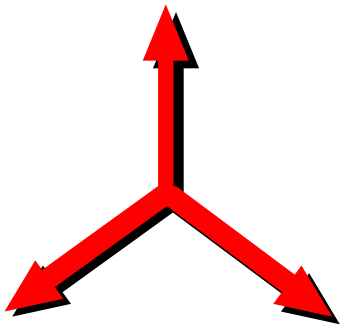
VERY LARGE ARRAY
Expansion Project



Interim Control & Monitor Processor
Hardware Specification

February 29, 2000

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1 Introduction.

An early phase of the Very Large Array (VLA) Expansion Project is the replacement of the aging Modcomp computers currently in use. The purpose of this document is to specify the hardware aspects of the Control & Monitor replacement processor (CMP) and its interface to the VLA system.

Since the CMP itself is comprised of Commercial Off The Shelf items, this document will focus on the interface and I/O signal characteristics between the CMP and the VLA system; the intent being to aid in the installation, debugging and future troubleshooting of this subsystem.

For a description of the current SLC to Modcomp interface refer to VLA Technical Report No. 44 "An Overview of the Monitor and Control System". For a detailed description of the SLC itself refer to VLA Technical Report No. 63, "The Serial Line Controller". For information on the new CMP hardware refer to the applicable documents described in the References section below.

1.1 Table of Contents

List of Figures

1.2 Definitions, Acronyms and Abbreviations used Throughout this Document

CMP	Control & Monitor Processor. A VME based single-board processor (MVME162-412) running VxWorks real-time OS that is replacing the existing computers.
Command Mode	The portion of the VLA Machine Cycle where the SLC accepts antenna control command words from one or both of the computers attached to it.
COTS	Commercial Off The Shelf (store-bought hardware).
DMA	Direct Memory Access. The ability of an I/O interface to get and put I/O data directly into and out of processor memory without requiring use of the processor itself.
Monitor Mode	The portion of the VLA Machine Cycle where the SLC collects monitor data from the Central and System Buffers and presents it to the computers.
SLC	Serial Line Controller. The NRAO built device that collects monitor data from, and sends command data to, the antenna array. The SLC resides between the CMP and the antenna array. The SLC will communicate with the CMP via the cable and connectors described in this document.
VLA Machine Cycle	19.2 times a second the system goes through the cycle of sending control information to, and receiving monitor information from the antennas in a half-duplex time-shared manner. This cycle is called the VLA Machine Cycle.
VLA	Very Large Array

1.3 References

MVME Embedded Controller Installation and Use, V162FXA/IH3, 1998, Motorola, Inc..

IP-Unidig-P User Manual, Revision 3, 8/2/99, SBS Greensprings Modular I/O.

VLA Technical Report No. 44, An Overview of the Monitor and Control System, March 1980, D.W. Weber.

VLA Technical Report No. 63, *The Serial Line Controller*, 12/11/86, David Weber

VLA Drawing No. F13720L46, Serial Line Controller Model B Logic Diagram.

VLA Drawing No. D13720L78, Serial Line Controller Model C Logic Diagram.

VLA Drawing No. D13720L01, Monty Interface Logic Diagram.

VLA Drawing No. D13720L60, Bacchus Logic Diagram.

VLA Drawing No. D13720W91, SLC - Modcomp Computer Cable Wire List.

2 VLA Control and Monitor System General Description

Command and Monitor Data are sent to and received from the VLA's 27 antennas at very distinct times in what is called the VLA Machine Cycle. The Control/Monitor data for each antenna are sent simultaneously, on individual RF carriers, over wave-guide using frequency multiplexing where each antenna occupies its own ‘band’.

Control, monitor and actual obsrervation data are passed to and from the antennas via three wave-guides (one for each arm of the array) in a half-duplex mode where transmitted command data and received monitor data ‘time-share’ the wave guide. This time-sharing is accomplished by allocating different times for control and monitor (transmit and receive) operations in the VLA Cycle. See Figure 2-1.

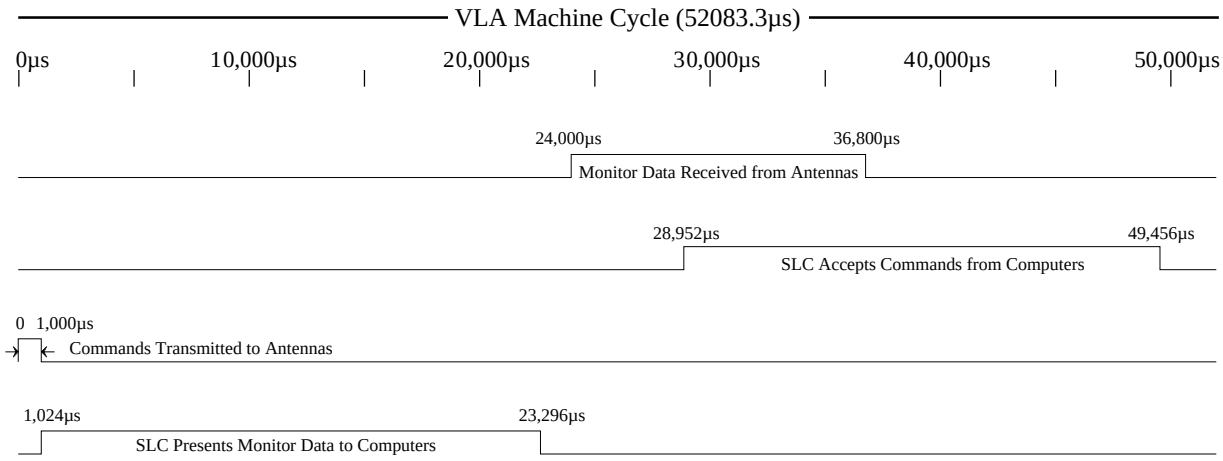


Figure 2-1. VLA Machine Cycle.

The VLA Cycles occur at a 19.2Hz rate which equates to a period of 52083µs per cycle. During time 28952µs to 49456µs of the previous cycle, command data is accepted from one or both of the control/monitor computers. Also on the previous cycle from 24000µs to 36800µs, monitor data is received from the antennas. At time 0µs to 1000µs of the subsequent cycle the command data previously received from the control/monitor computer(s) is transmitted to the antennas via the wave-guide. From 1024µs to 23296µs the previously received monitor data is sent to the control/monitor computers.

The Serial Line Controller is responsible for the timing of the control and monitor data transfers and therefore initiates all transfers to and from the CMP.

2.1 SLC General Description

The Serial Line Controller is a custom built device that provides the interface between the CMP and the antennas. For command operations the SLC essentially converts parallel I/O data from the CMP into serial data which is RF modulated and sent to the antennas. For monitor operations, the SLC coverts the demodulated serial data from the antennas into parallel I/O data for the computers. In addition to the serial/parallel conversions, the SLC provides parity insertion, error detection and antenna hardware addressing error detection.

The SLC is self-contained in a rack mounted chassis with its own internal power supply. The SLC chassis provides 32 rear panel connectors that interface to the 27 antennas (plus 5 for growth), eight connectors that may be connected to Data Taps to visually monitor message flow within the monitor and control system, a connector which provides a clock and other control signals and two computer interface connectors which provide 16-bit input, 16-bit output and associated handshaking signals to the CMP.

2.2 CMP General Description.

The Control and Monitor Processor (CMP) is a Motorola MVME-162FX Single Board Embedded Controller utilizing a Motorola 68LS040 microprocessor residing in a 6U VME chassis running VxWorks Real-Time OS. The 162 holds up to four Industry Pack (IP) Mezzanine Modules two of which will be used to provide input and output communications between the Serial Line Controller (SLC) and the CMP. The two IP modules used are the SBS Greensprings IP-UniDig-P 16-Bit Parallel I/O with handshaking.

One IP module will provide 16-bit Input from the SLC while the other will provide 16-bit Output to the SLC. The IP modules plug directly into the MVME-162 via standard IP Interface connectors. The MVME-162 in turn provides one 50-pin ribbon cable type connector for each of the four IP modules. 50-conductor ribbon cable or braided twisted-pair will exit the VME Chassis through slots provided on the front panel of the MVME-162.

See Appendix D for a diagram of the MVME162FX and its connector locations.

3 Detailed Description of CMP to SLC Interface.

The SLC can be interfaced to two computers. Monitor data is sent simultaneously to both computers while command data is received alternately from each of the two. VLA command and monitor data words are 48-bits in length; the parallel interface between the SLC and CMP however, is only 16-bits wide. For this reason, one 48-bit command/monitor data word must be transferred in three 16-bit segments.

The following subsections detail the data transfers and handshaking involved for sending command data and receiving monitor data. Logic diagrams are simplified to show only components necessary for the interface circuits being discussed; for the complete SLC logic diagrams see VLA Drawing numbers F13720L46 and D13720L78.

3.1 Command Data Transfer Operation

Command operations take place during the period 28952µs - 49456µs of the VLA Cycle. The SLC initiates the data transfers by querying each of the two computer interfaces alternately every 80 µs during this command cycle period. This means that one computer will be queried every 160µs. Figure 3.1-1 shows the timing for one computer interface; the identical handshaking occurs for the other interface offset by 80µs.

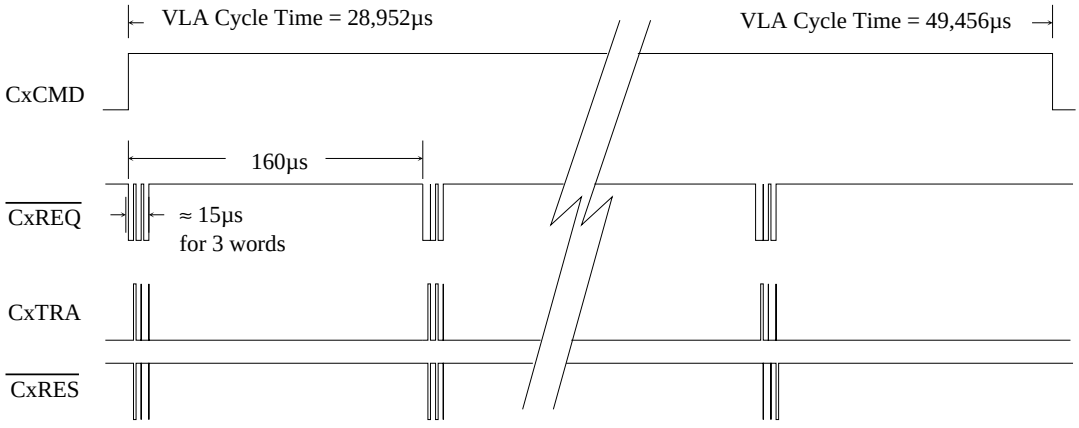
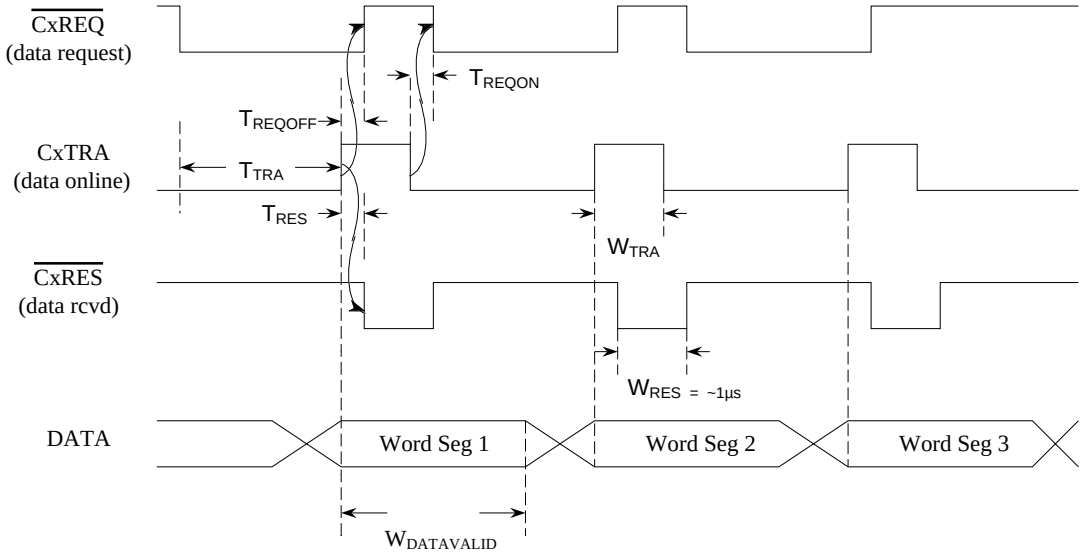


Figure 3.1-1. Command Cycle Timing.

The command word is 48-bits in length and is formed from three 16-bit segments generated by the computer. The three 16-bit segments are sent in a burst and must be completed within 80µs before the SLC initiates transfers from the other computer. Handshaking is accomplished by the SLC asserting CxREQ (Data Request) and the CMP responding CxTRA (Data Transferred) after placing the data on the output lines.



Parameter	From	To	Min	Typ	Max	Notes
T_{TRA}	CxREQ	CxTRA		Note 1		Note 1: All three word transfers must not exceed 80µs
W_{TRA}	CxTRA-ON	CxTRA-OFF	300ns	1µs	Note 1	
T_{REQOFF}	CxTRA-ON	CxREQ-OFF	200ns		400ns	
T_{REQON}	CxTRA-OFF	CxREQ-ON	200ns		400ns	
T_{RES}	CxTRA-ON	CxRES-ON	300ns		600ns	
$W_{DATAVALID}$			600ns		Note 1	

Figure 3.1-2. Handshaking Timing for Command Word Segment Transfers.

Refer to Figure 3.1-2. The three command word segment transfers occur as fast as the computer I/O interface (and line delays) will allow with the only speed 'governor' being a 300ns delay imposed in the SLC logic.

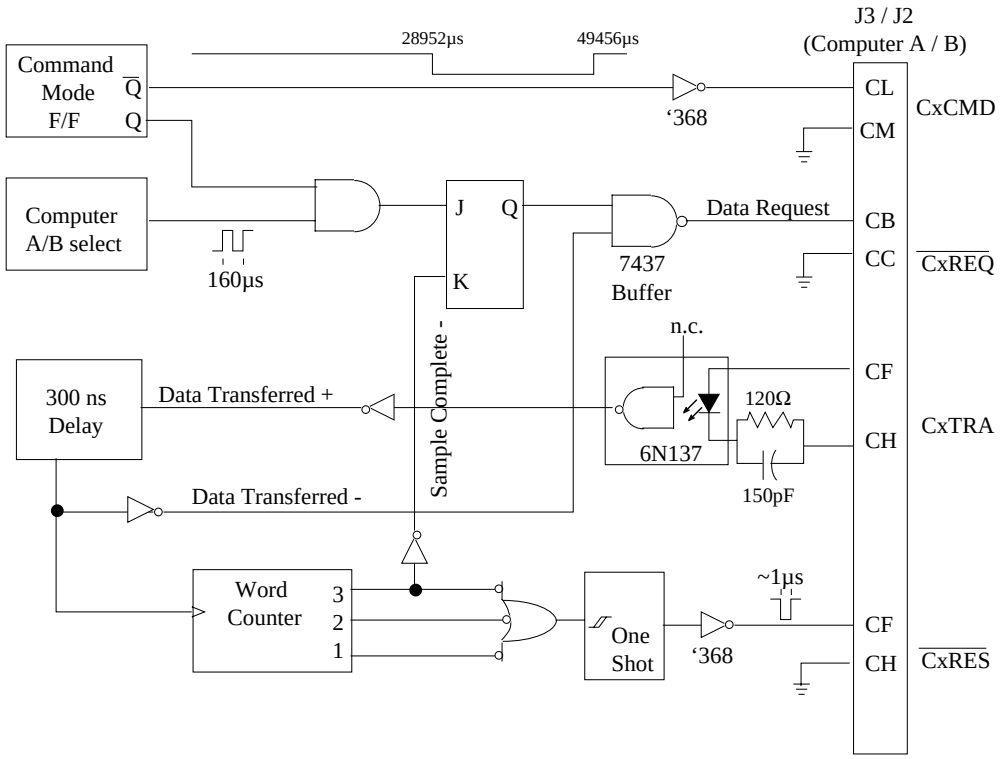


Figure 3.1-3. SLC Command Word Transfer Handshaking Logic.

Refer to Figure 3.1-3. The figure shows the handshaking logic for one computer interface, in reality there are two identical interfaces and the signal names reflect which is which. For discussion purposes signal names such as CACMD and CBCMD are referred to as CxCMD. Timing logic in the SLC enables the Command Mode signal CxCMD at time 28952µs via the Command Mode Flip/Flop. The Command Mode Flip/Flop also enables a divide by 80 circuit fed by a 1 MHz clock which in turn toggles the A/B Mode Flip/Flop to produce the Computer A Data Request and Computer B Data Request (CxREQ) signals alternatively every 80 µs. When the computer sees CxREQ it puts the first of three 16-bit command word segments on the output data lines and raises the Data Transferred (CxTRA) line. CxTRA causes the SLC to store the

data bits in a register and starts a 300ns delay timer. After the 300ns delay, Data Xfer (-) disables CxREQ which in turn causes the computer to disable CxTRA and readies the logic for the second segment of the 3-segment command word. The second and third segments are transferred the same way with the exception that at the completion of the third segment SAMPLE COMPLETE (-) disables further CxREQs until the next 160µs period.

The SLC inputs utilize 6N137 optoisolators (or equivalent) with the driven LED in series with a 120Ω resistor. The output drivers on the IP-UniDig-P module are MMPQ2329 (2N2329 transistors packaged in a quad surface-mount DIP package) with open collector outputs. These outputs are pulled up to 5VDC via a 220Ω resistor.

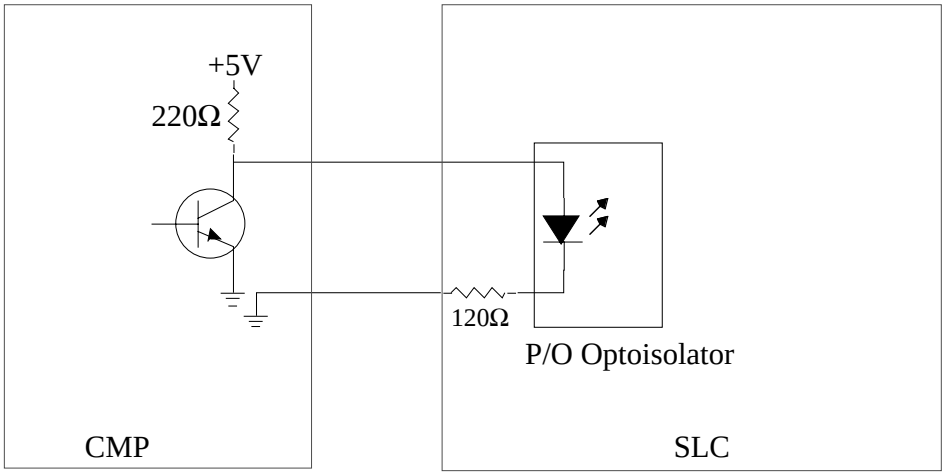


Figure 3.1-4. Typical Output Bit and Handshake line circuit.

Note: The IP-UniDig-P module ships from the factory with 1KΩ pull-up resistors in place in three 9-pin DIP sockets; these must be replaced with the 220Ω resistor mentioned in the text to ensure compatibility with the SLC optoisolators.

Handshaking for the SBS Greensprings IP-UniDig-P module is controlled by a Xilinx FPGA. Four handshake lines (Data Strobe, Data Acknowledge, Ready For Data and Data Available) can be programmed to operate in one of four modes. For transfers of command data from the CMP to the SLC, IP-UniDig-P Mode 0 will be used which uses the Ready For Data and Data Available lines. The CMP will pend on the Ready For Data line which is tied to the SLC

CxREQ line. When CxREQ goes active, the IP module will respond by placing a word of data on the output lines and activating Data Available which is connected to the SLC CxTRA signal. Though not used, CxRES is connected to the IP's Data Acknowledge line.

Observed transfer rates of one 16-bit word segment of control data from the CMP to SLC are [TBD].

3.2 SLC Monitor Data Transfer Operation

Monitor operations take place during the period 1024µs - 23296µs of the VLA Cycle. During this time the SLC transfers monitor data to the two computers concurrently at 58µs intervals.

Data collected from the antennas on the previous cycle are contained in buffers called Central Buffers. There are 31 Central Buffers, one associated with each antenna (only 27 are in use) and one System Buffer. Each buffer has six Data Sets associated with it and two monitor words are polled from each Data Set for a total of 32 x 6 x 2 = 384 monitor data words per VLA Cycle. The first monitor data word is polled and assembled during the 58µs time period starting at time 1024µs in the VLA Cycle; during the second 58µs period, this word is transferred to the computers while the SLC simultaneously polls and assembles the second monitor data word from the Central Buffers. Thus, while the SLC is sending word n to the computers, it is gathering word n+1 from the Central Buffers.

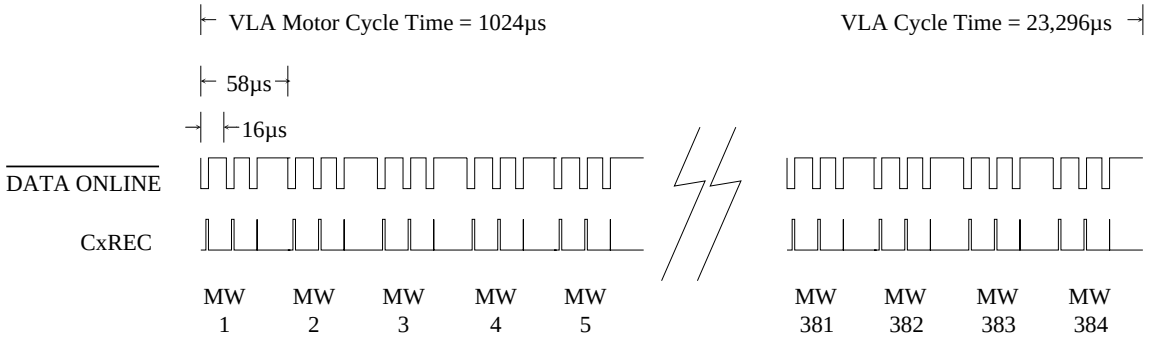
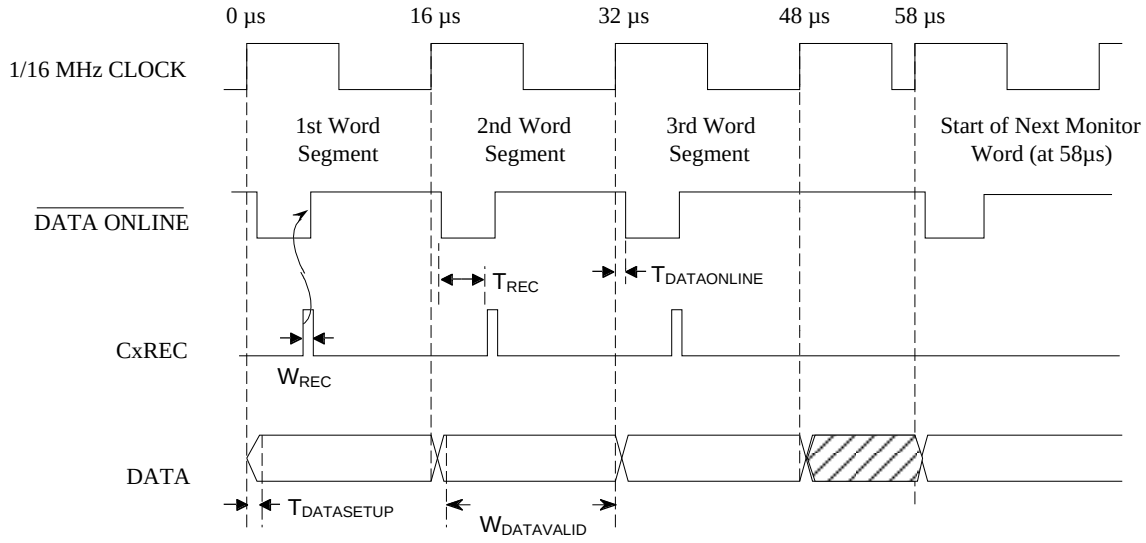


Figure 3.2-1. Monitor Cycle Timing.

Each monitor data word is 48 bits in length and is transferred to the computer in three 16-bit segments. Each 16-bit segment is placed on the data lines for 16µs only; the computer must accept the data within this allotted time or it will be lost. Three words are placed on the lines during each 58µs period.



Parameter	Min	Typ	Max	Notes
W_{REC}	25ns	1µs	Note 1	Note 1: WREC + TREC must not exceed 14µs
T_{REC}		Note 1		
$T_{DATASETUP}$		36ns	85ns*	* DATA ONLINE should not be used directly as a data latch since, under worst-case conditions, data may not be valid. A delay of at least 50ns should be used.
$T_{DATAONLINE}$		37µs*	108ns	
$W_{DATAVALID}$	15.9 µs			

Figure 3.2-2. Monitor Word Transfer Detailed Timing.

Even if the computer accepts the data faster than the 16µs allotted time, the next word will not be placed on the lines until the next 16µs period.

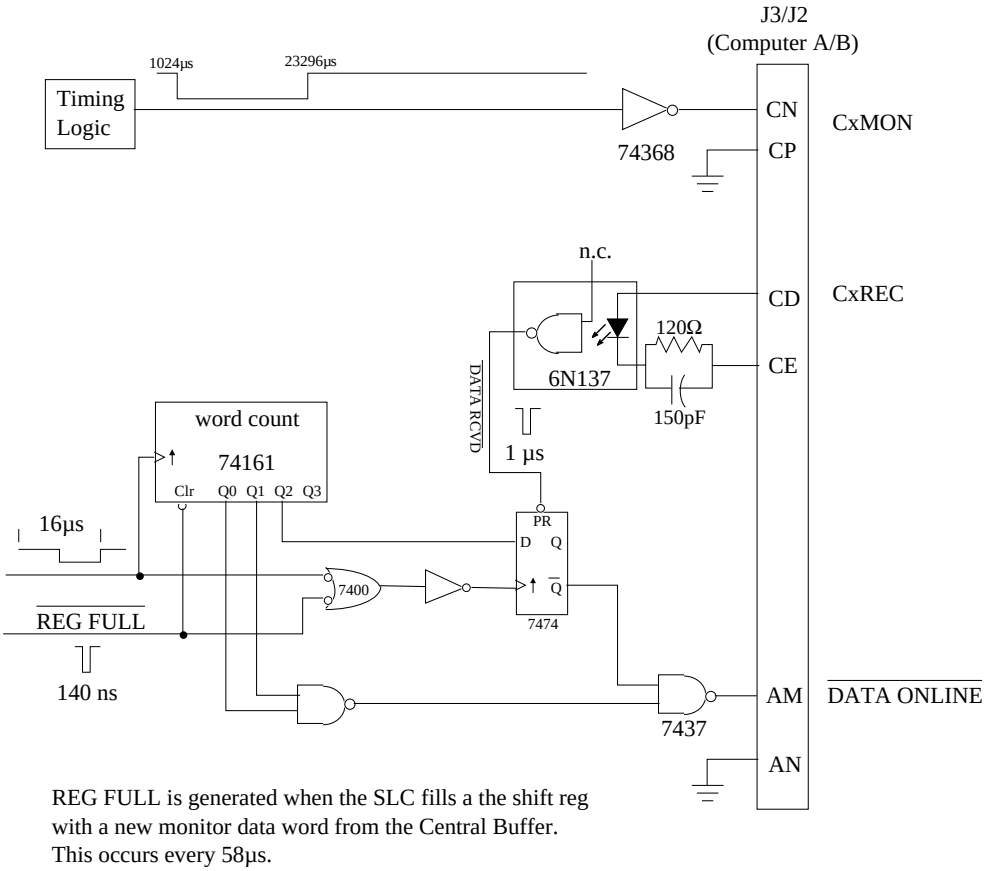


Figure 3.2-3. Monitor Word Transfer Handshaking Logic.

Refer to Figure 3.2-3. Timing logic in the SLC enables CxMON at time 1024 of the VLA Cycle. This TTL signal is active HIGH and is driven by a 74368 TTL Bus Driver. CxMON remains active for the duration of the monitor word transfer portion of the VLA Cycle. After the first monitor data word is assembled from the Central Buffer and loaded into the output register, a REGISTER FULL signal is applied to initialize the monitor word transfer handshaking logic to begin a new three-word count.

A 16µs clock sequences the word counter which enables half of the DATA ONLINE output gate for the first three 16µs counts. The other half of the DATA ONLINE gate is held enabled by a D-type flip-flop. When the computer has accepted the data, it replies with CxREC which presets the flip-flop and disables the DATA ONLINE gate. CxREC is a ≈ 1µs pulse generated by a one-shot in the Modcomp interface. With the next 16µs tick from the clock, the flip-flop again enables the DATA ONLINE gate and the cycle continues two more times (for a total of three) at which time the first half of the output gate is no longer enabled since the word count is greater than three. At the next 58µs interval, REGISTER FULL re-initializes the word count logic and the cycle repeats.

The IP-UniDig-P modules utilize AM26LS33A Differential Line Receivers for data bits and handshaking line inputs. One side of each receiver is tied to a 1.5 Volt reference level so the logic switching threshold is at 1.5VDC. Each receiver will handle up to +15V/-5V input voltage. The line receivers provide 50mV of hysterisis on the inputs.

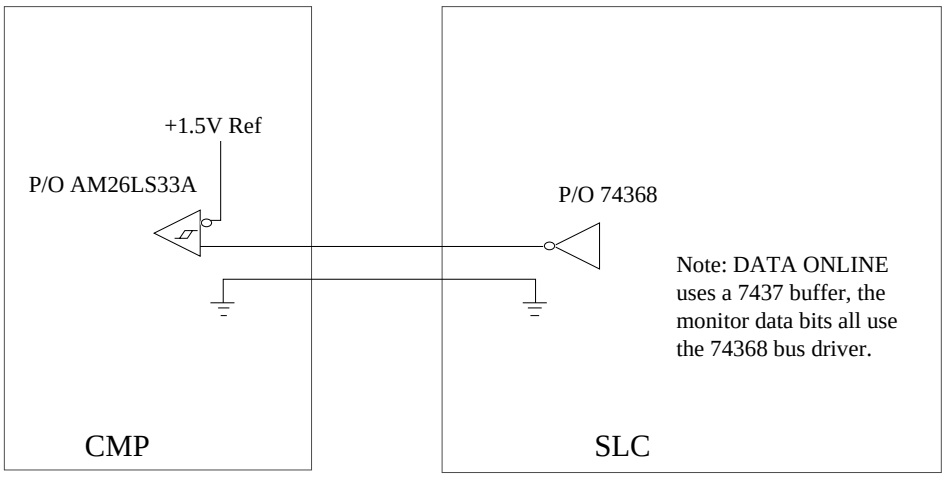


Figure 3.2-4. Typical Input Circuit for Monitor Data Bits and Handshaking Lines.

As stated earlier in the Command Cycle discussion, the IP-UniDig-P provides four different handshaking modes. Handshake Mode 2 will be utilized for monitor word transfers to the CMP. In this mode the IP's Data Available line will be connected to the SLC DATA ONLINE line. When DATA ONLINE goes active, the IP-UniDig-P will latch the incoming data and respond

with Data Acknowledge which is tied to the SLC CxREC line. Typical observed transfers rates for one 16-bit transfer of monitor data from the SLC to the CMP are [TBD].

3.3 SLC to CMP Interface Cable Description

The interface cable will consist of two 50-pin female ribbon cable type connectors (P1 and P2) on one end that will plug into the CMP; the other end will terminate in an ELCO 8016 series 90-pin connector (8016-90) which will be designated P3. The MVME162FX VME Processor board contains four 50-pin male ribbon cable type connectors with each one connected directly to its respective Industry Pack module. Since each IP-UniDig-P Industry Pack module can serve as an input or output device, any of the four IP module locations can serve as either Control or Monitor data transmitter or receiver. For specification purposes, IP Module A (IP_a) will be designated as the Control Data Output port and IP Module C (IP_c) will be designated as the Monitor Data Input port.

Using the above convention, P1 will be connected to J6 on the MVME162FX and P2 will be connected to J17. P3 of the interface cable may be connected to either J2 or J3 of the SLC where J3 is Computer 'A' and J2 is Computer 'B'.

The cable wiring will consist of two 50-conductor braided twisted pair cables each terminating in P1 or P2 at the CMP end and both terminating in P3 at the SLC end. The cable shall be no longer than 12 feet in length.

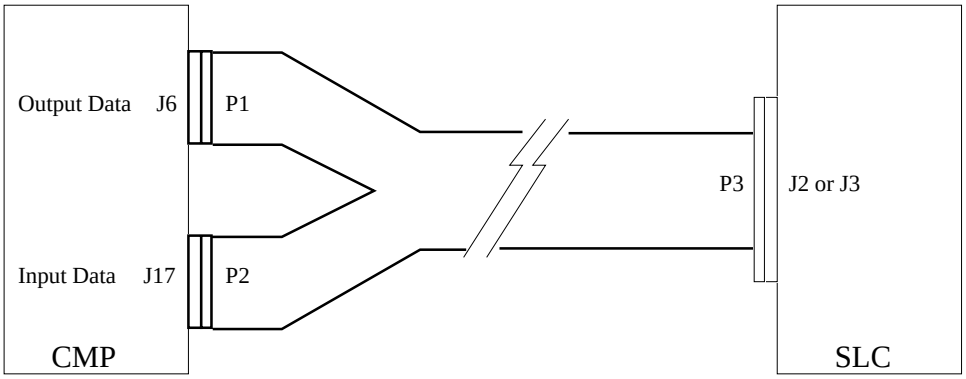


Figure 3.3-1. Interface Block Diagram.

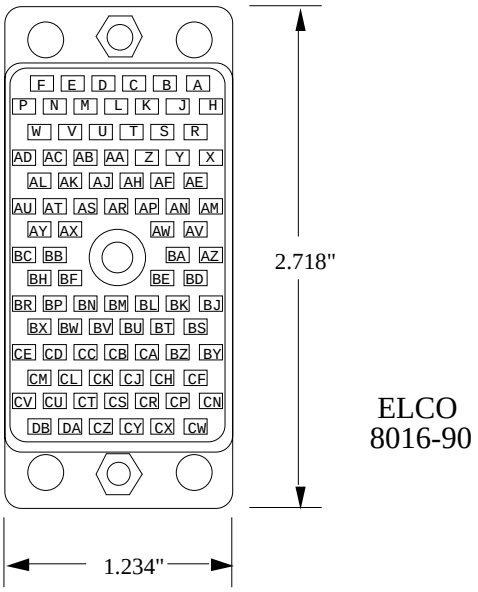


Figure 3.3-2. Looking into the pin-side of P3.

Appendix A. Wire Connection List

SLC Side Pin	SLC Signal Name	CMP Side Pin	CMP Signal Name	Remarks
P3-AK	CxB01	P1-01	OB-01	CMP Output Data Bit 01
P3-AL	CxB01-R	P1-02	OB-01-R	
P3-AH	CxB02	P1-03	OB-02	CMP Output Data Bit 02
P3-AJ	CxB02-R	P1-04	OB-02-R	
P3-AE	CxB03	P1-05	OB-03	CMP Output Data Bit 03
P3-AF	CxB03-R	P1-06	OB-03-R	
P3-AC	CxB04	P1-07	OB-04	CMP Output Data Bit 04
P3-AD	CxB04-R	P1-08	OB-04-R	
P3-AA	CxB05	P1-09	OB-05	CMP Output Data Bit 05
P3-AB	CxB05-R	P1-10	OB-05-R	
P3-Y	CxB06	P1-11	OB-06	CMP Output Data Bit 06
P3-Z	CxB06-R	P1-12	OB-06-R	
P3-R	CxB07	P1-13	OB-07	CMP Output Data Bit 07
P3-X	CxB07-R	P1-14	OB-07-R	
P3-S	CxB08	P1-15	OB-08	CMP Output Data Bit 08
P3-T	CxB08-R	P1-16	OB-08-R	
P3-U	CxB09	P1-17	OB-09	CMP Output Data Bit 09
P3-V	CxB09-R	P1-18	OB-08-R	
P3-P	CxB10	P1-19	OB-10	CMP Output Data Bit 10
P3-W	CxB10-R	P1-20	OB-10-R	
P3-M	CxB11	P1-21	OB-11	CMP Output Data Bit 11
P3-N	CxB11-R	P1-22	OB-11-R	
P3-K	CxB12	P1-23	OB-12	CMP Output Data Bit 12
P3-L	CxB12-R	P1-24	OB-12-R	
P3-H	CxB13	P1-25	OB-13	CMP Output Data Bit 13
P3-J	CxB13-R	P1-26	OB-13-R	
P3-E	CxB14	P1-27	OB-14	CMP Output Data Bit 14
P3-F	CxB14-R	P1-28	OB-14-R	
P3-C	CxB15	P1-29	OB-15	CMP Output Data Bit 15
P3-D	CxB15-R	P1-30	OB-15-R	
P3-A	CxB16	P1-31	OB-16	CMP Output Data Bit 16
P3-B	CxB16-R	P1-32	OB-16-R	
P3-CB	CxREQ	P1-41	Request For Data	CMP Output waits on this signal from SLC before sending output data word.
P3-CC	CxREQ-R	P1-42	RFD-R	
P3-CF	CxTRA	P1-39	Data Available	CMP activates this line when it has placed valid data on output lines.
P3-CH	CxTRA-R	P1-40	DA-R	
P3-CT	CxRES	P1-45	Data Strobe	(not used)
P3-CU	CxRES-R	P1-46	DS-R	

SLC Side Pin	SLC Signal Name	CMP Side Pin	CMP Signal Name	Remarks
P3-AP	IxB01	P2-01	IB-01	CMP Input Data Bit 01
P3-AR	IxB01-R	P2-02	IB-01-R	
P3-AS	IxB02	P2-03	IB-02	CMP Input Data Bit 02
P3-AT	IxB02-R	P2-04	IB-02-R	
P3-AV	IxB03	P2-05	IB-03	CMP Input Data Bit 03
P3-AW	IxB03-R	P2-06	IB-03-R	
P3-AX	IxB04	P2-07	IB-04	CMP Input Data Bit 04
P3-AY	IxB04-R	P2-08	IB-04-R	
P3-AZ	IxB05	P2-09	IB-05	CMP Input Data Bit 05
P3-BA	IxB05-R	P2-10	IB-05-R	
P3-BB	IxB06	P2-11	IB-06	CMP Input Data Bit 06
P3-BC	IxB06-R	P2-12	IB-06-R	
P3-BD	IxB07	P2-13	IB-07	CMP Input Data Bit 07
P3-BE	IxB07-R	P2-14	IB-07-R	
P3-BF	IxB08	P2-15	IB-08	CMP Input Data Bit 08
P3-BH	IxB08-R	P2-16	IB-08-R	
P3-BJ	IxB09	P2-17	IB-09	CMP Input Data Bit 09
P3-BK	IxB09-R	P2-18	IB-09-R	
P3-BL	IxB10	P2-19	IB-10	CMP Input Data Bit 10
P3-BM	IxB10-R	P2-20	IB-10-R	
P3-BN	IxB11	P2-21	IB-11	CMP Input Data Bit 11
P3-BP	IxB11-R	P2-22	IB-11-R	
P3-BR	IxB12	P2-23	IB-12	CMP Input Data Bit 12
P3-BX	IxB12-R	P2-24	IB-12-R	
P3-BV	IxB13	P2-25	IB-13	CMP Input Data Bit 13
P3-BW	IxB13-R	P2-26	IB-13-R	
P3-BT	IxB14	P2-27	IB-14	CMP Input Data Bit 14
P3-BU	IxB14-R	P2-28	IB-14-R	
P3-BS	IxB15	P2-29	IB-15	CMP Input Data Bit 15
P3-BY	IxB15-R	P2-30	IB-15-R	
P3-BZ	IxB16	P2-31	IB-16	CMP Input Data Bit 16
P3-CA	IxB16-R	P2-32	IB-16-R	
P3-AM	DATA ONLINE	P2-39	Data Available	Sent by SLC when valid monitor data is available for input to CMP.
P3-AN	DATA ONLINE-R	P2-40	Data Avail-R	
P3-CD	CxREC	P2-43	Data Acknowledge	Sent by CMP to acknowledge data received from SLC
P3-CE	CxREC-R	P2-44	Data Ack-R	

Appendix B. SLC Signal Description

The following summarizes the handshaking and data signal characteristics associated with the SLC. The SLC specifies the computer interface ('A' or 'B') in each signal-name which is denoted by a small 'x' here; for example, 'CxCMD' would actually be seen as either 'CACMD' or 'CBCMD'. Not all the signals described here are used in the SLC to CMP interface but they are described here nonetheless for information on what is available if needed.

SLC Signal Electrical Characteristics Table

Signal Name	Generated By	Remarks
CxCMD	SLC	Command Mode. Asserted by the SLC during the entire Command Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out.
CxMON	SLC	Monitor Mode. Asserted by the SLC during the entire Monitor Mode portion of the VLA Machine Cycle. SLC output; TTL; active HIGH; driven by a 74368 tri-state bus driver on a single fan-out (this connector).
CxREQ	SLC	Data Request. The SLC is requesting the CMP to place 16-bits of command data on the output data lines. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of three; 1) this signal, 2) the Test Connector (J1) and 3) the PRESET input of a 7474 'D'-type Flip-Flop.
CxRES	SLC	Data Received. The SLC acknowledges receipt of data from CMP interface. SLC output; TTL; active LOW; ~1μs pulse driven by a 74368 tri-state bus driver on a single fan-out.

CxTRA	CMP	Data Transferred. The CMP tells the SLC that it has placed a 16-bit command word segment on the output data lines. SLC current loop input; current required to be active ON; optically isolated input via a 6N137 Opto-isolator; typical switching delay of about 50 ns. See Optical Isolator note below.
DATA ONLINE	SLC	Data Online. The SLC has placed a monitor data word segment on the CMP interface's input lines. SLC output; TTL; active LOW; driven by a 7437 NAND Buffer with a fan-out of two; 1) this signal and 2) as a current sink for an LED on the SLC front panel Monitor Status Display - the current source is +5V through a 390Ω resistor.
CxREC	CMP	Data Received. The CMP acknowledges receipt of the monitor data word segment placed on its input lines by the SLC. SLC input; current loop input, input current required to be active ON; optically isolated via a 6N137 Opto-isolator; typical switching delay of about 50 ns. CxREC on the old (Modcomp) interface is a 1µs pulse generated from a one-shot. This pulse ends up at the PRESET pin of a 7474 flip-flop and is a pulse to ensure that the PRESET level is returned to inactive before the 16µs clock signal 'ticks' at this flip-flop (lest the clock be ignored). For this reason, it is important that CxREC arrive within 15µs to ensure the flip-flop is ready to receive the next clock. It is possible that the new interface need not generate a pulse and instead just reset CxREC when it sees DATA ONLINE go inactive. See Optical Isolator note below.
CxB01 - CxB16	CMP	Command Bits. Carry one 16-bit command word segment from the CMP interface to the SLC. SLC optically isolated inputs via a 6N137 Opto-isolator (see note on optical isolated SLC inputs below).
IxB01 - IxB16	SLC	Monitor Bits. Carry one 16-bit monitor word segment from the SLC to the CMP interface. SLC output; TTL active LOW driven by a 74368 tri-state bus driver with a single fan-out (this connector).

NOTE: The Optical Isolators on the input lines of the SLC employ a 120Ω current limiting resistor in series with the input diode. The 6N137 has a recommended operating current of 6.3 to 15 mA and a max of 20 mA. The SBS Greensprings IP-UniDig-P module utilizes open collector outputs with 1 KΩ pull up resistors as shipped from the factory. This combination of 1 KΩ plus the 120Ω series resistor will result in a current of only about 4.5 mA. The pull-up resistors on the IP modules are socketed SIP resistors which may be replaced with ones of a lessor value. A value of 220Ω will provide a current of (5.0V - 1.5 V(drop across the diode)) / (220Ω + 120Ω) = 3.5V / 3.4V = 10.3 mA.

Appendix C. IP-UniDig-P Industry Pack Module Specification

Each IP-UniDig-P provides a 16-bit parallel port with four programmable handshaking signals. The port may be configured for either input or output operations. When configured as an input device, all data lines utilize 26LS33 differential line receivers with one input of each receiver internally configured to provide a logic switching threshold of 1.5 volts. When configured as an output device, the outputs are driven by MMPQ2369 transistors with open collector outputs which are pulled up to +5V by 1KΩ resistors. The outputs are rated to sink 64 mA. The 1KΩ pull-up resistors are in socketed 9-pin SIPs which may be replaced with different values as will be required to interface with the optical isolator inputs of the SLC.

General

Size	Single High Industry Pack
Digital Interface	16 digital signal lines with double buffered inputs and outputs. 4 Handshake Lines. 8 MHz buffered IP Clock
Interface Level	Outputs: TTL Open Collector with 1KΩ pull up resistor standard, 64mA current sink. Inputs: Logic threshold of 1.5 V with 50 mV of hysteresis, voltage range +15V/-5V.
Handshake Modes	Mode 0: Ready For Data, Data Available Mode 1: Data Strobe, Data Acknowledge Mode 2: Ready For Data, Data Available, Data Acknowledge Mode 3: Data Available, Data Strobe Mode 4: Data Strobe
Software Interface	The 16 I/O lines are read or written with either word or byte accesses. There is an 8-bit Output Control Register and 16-bit Control and Status Register.

Initialization	300 Millisecond delay from reset. Forces all lines to a high impedance state. Clears the Control and Status Register and Output Control Register.
Access Mode	Byte or word in I/O Space.
DMA	Channel 0 supported.
Interrupts	Channel 0 supported.
Dimensions	Standard Single High Industry Pack width and length (1.8 x 3.9 inches).
Construction	Conformal Coated FR4 4 layer Printed Circuit. Surface mounted components.

Appendix D. MVME162FX Connector Locations.