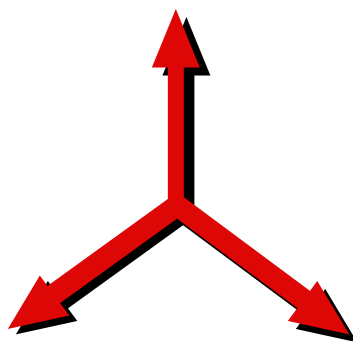


# EXPANDED VERY LARGE ARRAY



## Antenna Monitor & Control Subsystem Preliminary Requirements Specification

November 15, 2001

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Operated by Associated Universities, Inc.  
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## **1 Introduction and Purpose of this Document**

"The VLA Expansion Project will combine modern technologies with the sound design of the existing VLA to produce a tenfold increase in scientific capabilities." So the brochure says.

Expansion of the VLA is divided into two phases. Phase I will retrofit the existing 27 VLA antennas with new digital electronics, new wide band receiver systems and a modernized on-line control system. A new correlator with greatly increased performance characteristics will be incorporated as well as a fiber-optic data transmission link between it and the antennas. Phase II of the expansion will add eight new antennas located throughout the state of New Mexico and will interface to the existing inner VLBA antennas.

The NRAO scientific community has begun Phase I design by specifying precisely what the EVLA must do in terms of science. The next step is to specify how the system must be engineered to meet those scientific requirements. The purpose of this document is to specify what will be required of one component of the system - the Antenna Monitor and Control Subsystem.

## 1.1 Description and Scope of this Document

The science requirements of the EVLA are documented in EVLA Memo No. 15, "Scientific Requirements for the EVLA Real-Time System". The term 'Real-Time System' means the system of hardware and software that controls all aspects of the system during observation time as opposed to the systems that perform scheduling functions prior to or data archiving and processing afterwards.

Two components of the EVLA are operated in real-time during an observation, the array of antennas and the correlator. The Real-Time System (or On-line System as it is sometimes called) is therefore divided into two subsystems called the Antenna Monitor and Control Subsystem (AMCS) and the Correlator Monitor and Control Subsystem (CMCS). This document will focus on the Antenna Monitor and Control Subsystem.

The basic structure of the AMCS has been loosely defined in previous documents and oral discussions. The physical and functional aspects of the AMCS as it is known at this early stage are presented in chapter 2. Chapter 3 discusses the Interim Control and Monitor System (ICMS) that will control the VLA antennas prior to their conversion, one by one, into EVLA antenna. The descriptions in chapters 2 and 3 are for informational purposes only - to acquaint the reader with the system so as to better understand the requirements presented later. The descriptions in chapters 2 and 3 are not to be interpreted as requirements themselves. Chapter 4 presents the specific requirements for the development of the EVLA AMCS. The requirements are divided into three categories:

- 1) Engineering Requirements - those pertaining to how the system is built,
- 2) Functional Requirements - those describing what the system must be able to do and
- 3) Performance and Constraint Requirements - those that specify the 'how fast' or 'how many' type details.

Most of those distilled from the scientific requirements document fall into the latter of the three categories with some exception.

## 1.2 Definitions, Acronyms and Abbreviations used Throughout this Document

AMCS	Antenna Monitor and Control Subsystem. The component of the EVLA responsible for operating the array of antennas.
ASG	Array Support Group. A subgroup of the Computing Division of NRAO Socorro's Array Operations Center. The ASG is responsible for the development and maintenance of the VLA, VLBA and EVLA software systems.
CMCS	Correlator Monitor and Control Subsystem. The component of the EVLA responsible for operating the correlator.
Class	A term used in Object Oriented Design to define a virtual object. All behavior of the virtual object is wholly contained within the class definition of that object. All data and the functions that manipulate that data to specify the object's behavior are defined within the class. Classes are not executed in code, they are simply definitions from which objects are created. In the case of the EVLA, an Antenna Class will be developed to represent (in software) the physical antennas that make up the EVLA System.
CMP	Control & Monitor Processor. A VME based single-board processor (MVME162-412) running VxWorks real-time OS that will be used during the transition phase to control and monitor the old style VLA antennas in conjunction with the new EVLA antennas. The purpose of this is to allow all the antennas of the array to be kept in operation during the years it will take to convert them all into EVLA type antennas. The CMP is also known as the Interim Control and Monitor Processor (ICMP).
Correlator Backend	The output side of the correlator. The ASG is responsible for the computing system that will process, in real-time the data produced by the correlator.
COTS	Commercial Off The Shelf (store-bought hardware).

DMA	Direct Memory Access. The ability of an I/O interface to get and put data directly into and out of the memory used by a processor without requiring use of the processor itself.
EVLA	Expanded VLA.
Hybrid Array	During the several-year transition phase where individual VLA antennas are converted to EVLA types, the system will have to be operational with both types of antennas. It is called the Hybrid Array and will remain as such until the last VLA antenna is upgraded.
ICMP	See CMP.
msec	Milliseconds.
μsec	Microseconds.
NMA	New Mexico Array.
Object	A term used in Object Oriented Design to designate an instance of a class. An object is an actual segment of code in a program that provides the behavior previously defined by the class of which it is an instance of. In the EVLA an Antenna Object is the virtual antenna that the operational system 'sees'. There will be one Antenna Object for each physical antenna in the system.
Operational System	Sometimes referred to as Operation System. The system(s) that operate the EVLA array. During normal observations, the EVLA Operational Management System (OMS) will operate the system to perform science. During maintenance the operation system might be that of a technician's laptop computer used to control the system for testing and troubleshooting purposes.
SLC	Serial Line Controller. The NRAO built device that collects monitor data from, and sends command data to, the old-style VLA antenna array. The SLC resides between the CMP and the antenna array.

Subarray	A disjoint collection of antennas that operate independently of the other antennas in the VLA and NMA.
UTC	Universal Coordinated Time
VLA	Very Large Array.
VLA-LST	VLA Local Sidereal Time.
VLBA	Very Long Baseline Array.

### 1.3 References

EVLA Memo No. 15; "Scientific Requirements for the EVLA Real-Time System", September 26, 2000; John Benson and Frazer Owen, NRAO.

EVLA Project Book, Chapter 9, "EVLA Monitor and Control System", October 16, 2001, Wayne Koski, George Peck, William Sahr.

"EVLA Architecture and Design Snapshot #1", March 26, 2001, Bill Sahr.

"The VLA Expansion Project System Requirements", March 2, 2001, Bill Sahr, Steve Blachman.

EC-1 Microprocessor Data Sheet, Rev G, Copyright 2001, Synergetic Micro Systems, URL: <http://www.embeddedcomm.com>

"EVLA Interim Control & Monitor Processor Hardware Specification", February 29, 2000, Kevin Ryan.

**1.4 Table of Contents**

<b>1 Introduction and Purpose of this Document .....</b>	<b>2</b>
1.1 Description and Scope of this Document.....	2
1.2 Definitions, Acronyms and Abbreviations used Throughout this Document .....	3
1.3 References.....	6
1.4 Table of Contents .....	7
<b>2 Description of the EVLA Antenna Monitor and Control Subsystem .....</b>	<b>9</b>
2.1 The Module Interface Board (MIB) .....	10
2.2 The Antenna Control Computer.....	12
2.2.1 The Antenna Class .....	13
2.3 The Array Control Computer .....	14
<b>3 Description of the Interim Control and Monitor System.....</b>	<b>16</b>
<b>4 Preliminary Requirements of the EVLA Monitor and Control System. ....</b>	<b>18</b>
4.1 Engineering Requirements .....	19
4.1.1 General Design Goals .....	19
4.1.2 Milestones, Deliverables and Prevention of 'Feature Creep'.....	19
4.1.3 Documentation Requirements.....	20
4.1.4 Software Engineering Requirements .....	20
4.1.5 Hardware Engineering Requirements [should this be here?].....	21
4.1.6 Component Names and Naming Convention .....	22
4.2 Functional Requirements of the Monitor and Control Subsystem.....	23
4.2.1 Hybrid Array Operation {EVLA Memo 15, 3.1.1} .....	23
4.2.2 Built In Test (BIT), Failures, Errors, Warnings and Data Flagging.....	23
4.2.3 Hardware Software Interface (the MIB) .....	26
4.2.4 Interactive Observing {EVLA Memo 15, 3.1.3} .....	27
4.2.5 Subarrays {EVLA Memo 15, 3.2.6} .....	27
4.2.6 RFI Detection and Excision {EVLA Memo 15, 3.2.6} .....	27
4.3 Performance, Constraint and Physical Requirements of the AMCS.....	29
4.3.1 Time Frame {EVLA Memo 15, 3.2.3} .....	29
4.3.2 Operational System Requirements.....	29

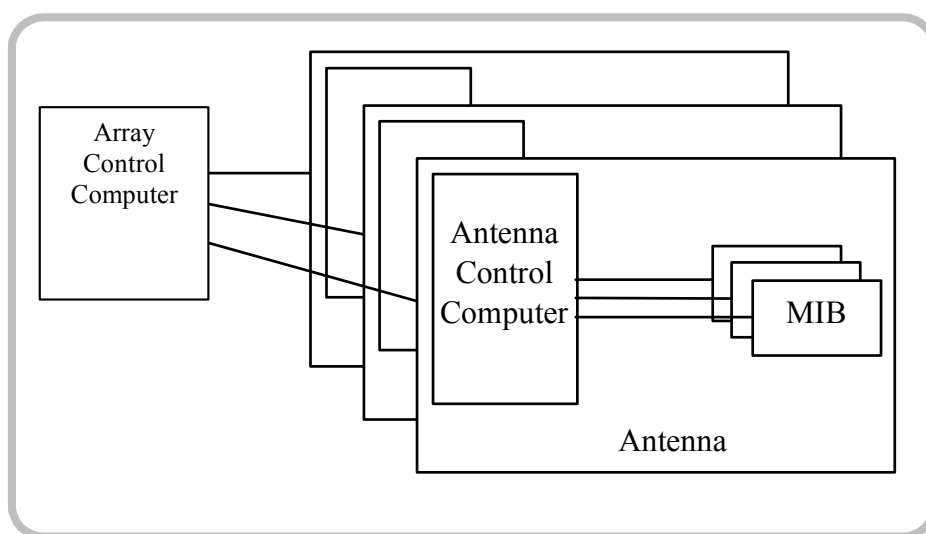
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4.3.3	Hardware Reconfiguration and Dynamic Corrections .....	29
4.3.4	Physical Requirements of the Antenna Control Computer .....	30
4.3.5	Physical Requirements of the Array Control Computer .....	30
<b>5</b>	<b>Design Considerations .....</b>	<b>31</b>
5.1	The Antenna Control Computer.....	32
5.2	The Array Control Computer .....	34



## 2 Description of the EVLA Antenna Monitor and Control Subsystem

The EVLA Monitor and Control Subsystem (AMCS) will consist of one Array Control Computer located in the Control Building at the existing VLA site, one or more Antenna Control Computers located either in the Control Building or in the antennas (in the case of the latter there will be one Antenna Control Computer per antenna), several micro-controllers per antenna that reside in the antennas and the networking hardware that connects them all.

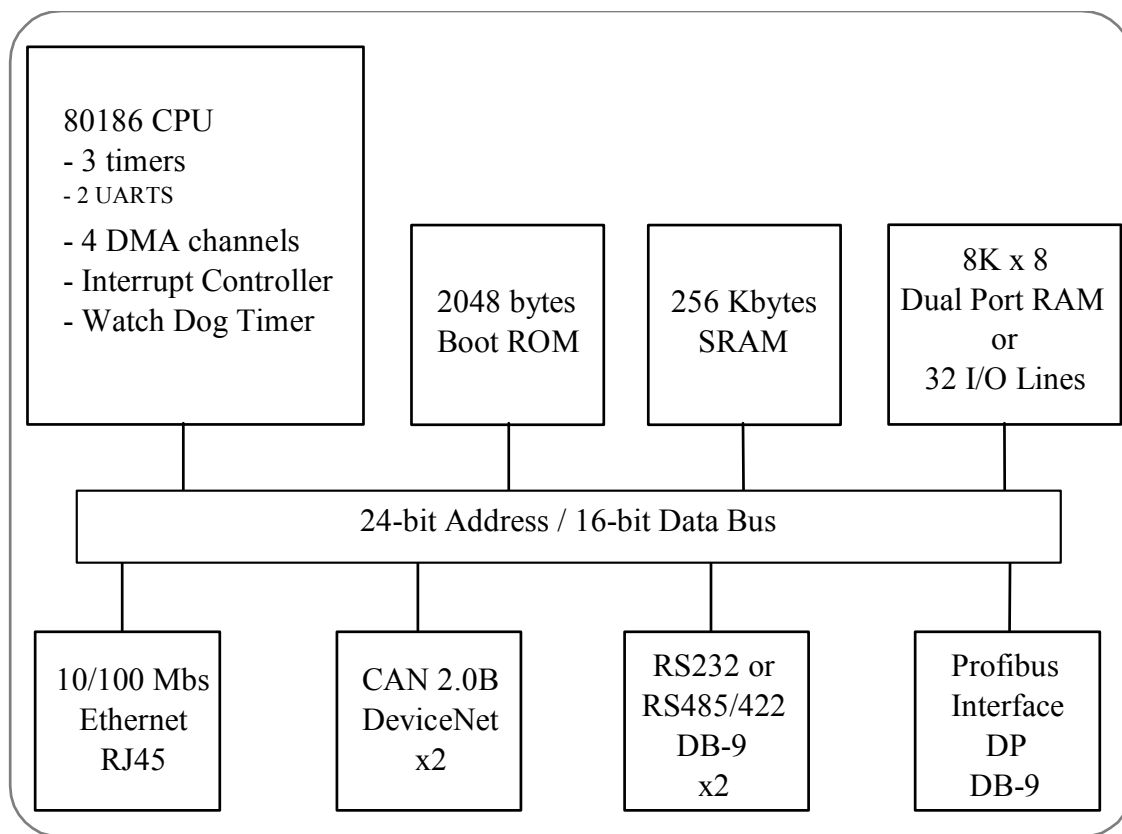


Whether the Antenna Control Computer resides in the antenna itself as shown above or resides in the Control Building, its functionality will remain about the same. The Module Interface Boards (MIB) operate specific antenna hardware, the Antenna Control Computers operate the MIBs and the Array Control Computer operates the Antenna Control Computers.

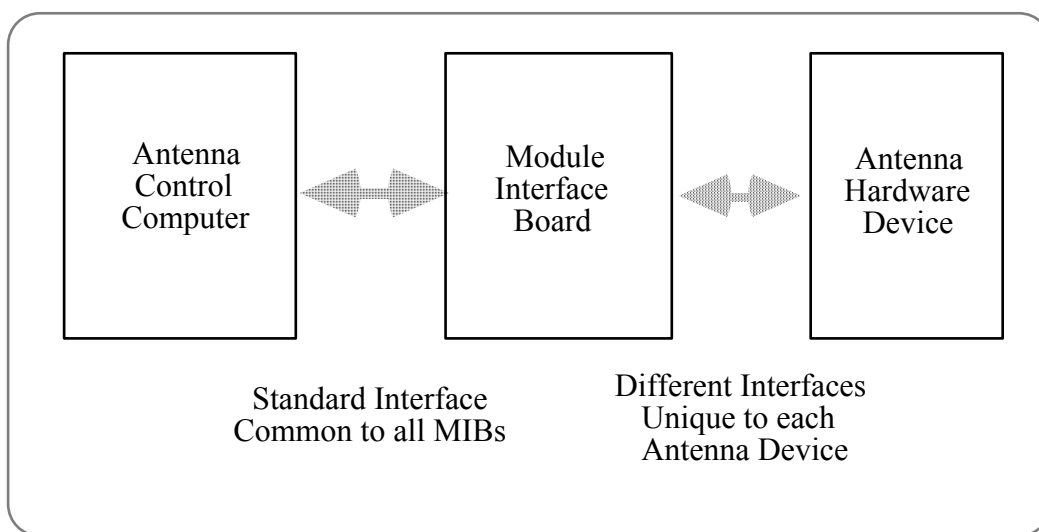
Each block in the diagram will be discussed in more detail in the following paragraphs.

## 2.1 The Module Interface Board (MIB)

The MIB will be a small self-contained microprocessor-based circuit board built by NRAO. As of this writing, the board will be built around the Synergetic EC-1 Communications System on Chip (SoC). The EC-1 is comprised of an Intel 80186 compatible microprocessor, 256K bytes of high-speed SRAM, 8Kx8 bytes of dual-port memory and a Serial Peripheral Interface (SPI) for communications to serial FLASH or other SPI compatible slave devices. The EC-1 supports two CAN channels, PROFIBUS, Ethernet, RS232, RS422 and RS 485 interfaces and protocols.



The MIB provides the interface between the Antenna Control Computer software and the antenna hardware. It will communicate with the Antenna Control Computer through the Ethernet port and with the antenna devices through one or more of its various other ports. This has the effect of converting the differing interface requirements of the various antenna devices into one interface type (Ethernet) for communications with the Antenna Control Computer.



It is not yet known how many MIBs will be used in the antenna or to what device(s) each will be connected. It is known however, that all devices in the antenna will be represented by one or more MIBs. For instance, one MIB may control both of the 1<sup>st</sup> LO Synthesizers or each synthesizer may be represented by its own MIB (or possibly by more than one MIB). The details of MIB placement and quantity have yet to be completed by the hardware engineering group.

The Module Interface Board effectively encapsulates the 'workings' of an antenna and provides a uniform physical and functional interface to the Antenna Control Computer. This encapsulation means, for instance, that the Antenna Control Computer program does not have to know *how* the antenna's azimuth position is changed, it simply just tells the MIB *where* to move it. This is important because it modularizes the system, keeping implementation details away from where they don't need to be. This means that hardware can be upgraded or modified with minimal affect on the software.

## **2.2 The Antenna Control Computer**

The Antenna Control Computer will most likely be a single board processor of either VME or CompactPCI form. It will not require large amounts of memory and processing power and will need few external interfaces other than Ethernet.

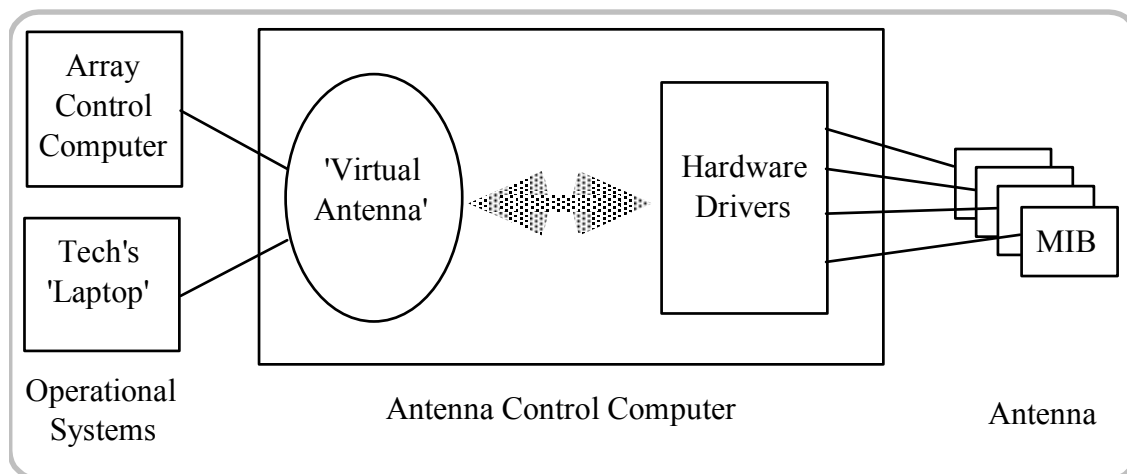
The Antenna Control Computer will either reside in the control building and interface to the antenna via optical fiber and network switches located in each antenna or will reside in the antenna itself and interface to the hardware in a more direct manner.

If the Antenna Control Computer resides in the Control Building, it will share one or more, many-slot, chassis with others of its own kind. If the computer resides in the antenna it will be housed in few-slot chassis with RFI shielding.

It is desired for the sake of decreasing RFI that optical cable be used for the Ethernet interface between the Antenna Control Computer and the Array Control Computer and between the Antenna Control Computer and the MIBs.

The Antenna Control Computer will use a Real-Time Operating System such as VxWorks or possibly RT Linux.

Functionally, the Antenna Control Computer will be an integral part of the EVLA antenna. It will be the interface to which all operational computers connect to operate the antenna; including the Array Controller Computer which will operate the array during normal observing, the technician's maintenance computers which will perform diagnosis, preventative and corrective maintenance functions and other systems that may control the antenna for special operations.



The Antenna Control Computer is the computer 'closest' to the antenna hardware itself. It presents a virtual representation of the antenna hardware to the rest of the AMCS and configures the antenna hardware to the state desired. It directly monitors and controls one antenna.

One of the main requirements of the EVLA AMCS is that it must be able to operate with different types of antennas (EVLA, VLBA, NMA). The Antenna Control Computer will provide a uniform representation of the antenna no matter what type of antenna it is controlling. This uniform representation is accomplished through the use of a software construct called the Antenna Class.

### 2.2.1 The Antenna Class

The purpose of the Antenna Control Computer is to transform the physical (hardware) antenna into a virtual (software) antenna that can be manipulated by various operational systems without them having to know the details involved at the hardware level. In effect, the antenna computer hides hardware implementation details from the operations system so that the operations systems can focus on *what* is being done instead of *how* it is being done. The functional interface will be accomplished through the use of a software based Antenna Class whose runtime instances, called Antenna Objects will each represent exactly one antenna.

The Antenna Class will be developed to represent the essence of an EVLA antenna. This will have the effect of generalizing the antenna interface that the operations systems will 'see' which, will in turn allow control of a hybrid system of VLA, EVLA, Pie Town VLBA, future New Mexico Array antennas and possibly 'unconnected' antennas such as other VLBA antennas from a single operations system. (Of course the latter VLBA examples will require that their station computers also implement the EVLA Antenna Class.)

In addition to standardizing control of many different antenna types, the Antenna Class will also provide system control by many different operational systems. It does this by, in effect, providing a standardized application interface (API) for applications wanting to operate the antennas. For instance, technicians will be able to operate the array (or individual antennas) to support maintenance activity. Scientists desiring to observe in a manner outside of the scope of the normal operational management system will be able to do so with their own control software. The Antenna Class relieves these various operational systems from having to duplicate antenna control and monitor functionality in their software.

The Antenna Class is also being designed to satisfy the scientific community's requirement that the system be able to utilize all current antennas during their transition from VLA to EVLA. The Interim Control and Monitor Processor will provide the functionality of the EVLA Antenna Control Computer to the antennas that are still of the VLA type by providing a similar Antenna Object (one for each remaining VLA antenna) to the EVLA operation system. In effect, the EVLA operation system will see 27 individual Antenna Objects without having to know which are EVLA and which are VLA.

## **2.3 The Array Control Computer**

The Array Control Computer will also likely be a single board processor with real-time operating system. It will definitely reside in the Control Building at the VLA site. It will interface to the Antenna Control Computers via high-speed (probably Gigabit) Ethernet over fiber-optic cable.

The Array Control Computer operates on groups of Antenna Objects thus forming the array of antennas. It will be responsible for carrying out the operation of the array during normal observation operation. It will convert the observe scripts (or their equivalent) into the actions needed to operate the array as a whole.

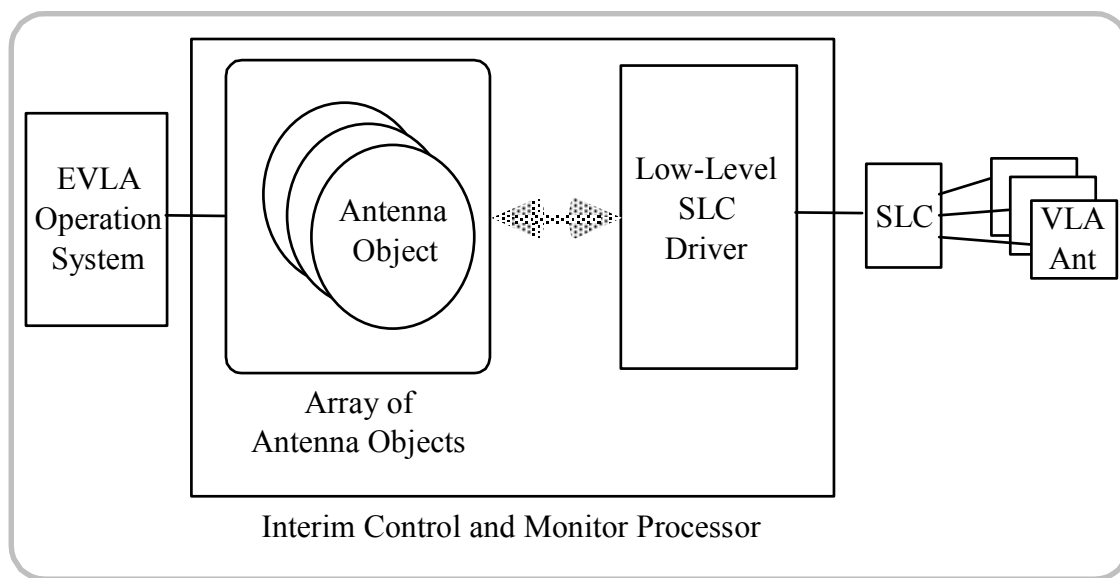
### 3 Description of the Interim Control and Monitor System

One of the requirements of building the EVLA is that system down time is kept to a minimum during its construction. The conversion of VLA antennas into EVLA types will be done one-by-one and will take several years to complete. It is desired that all 27 antennas be kept operational as a single array during this transition phase even though some will be old and others new. It is also desired that this 'hybrid array' be operated by the new EVLA operational system. Since the aging Modcomp Computers which operate the VLA today do not lend themselves well to the major software change necessary to make them work with the EVLA operational system, it was decided that a new computer system be built to provide this functionality. This new system is called the Interim Control and Monitor Processor (CMP).

Control of the VLA is done through a central processor scheme where one computer controls the whole array. Command data is sent out and monitor data is received in through a common piece of equipment called the Serial Line Controller (SLC). The SLC accepts commands targeted at individual antennas and broadcasts them to the whole array. The antenna for whom the command was directed acts upon it when received. The SLC also receives monitor data from all antennas and presents them to the operations computer.

The CMP will also interface to the SLC to provide the same low-level command sending and monitor data retrieving as the Modcomp computer does presently. In addition to this, the CMP will provide a high level interface - akin to Antenna Objects - that the EVLA operational system will 'see'. In so doing the EVLA operational system will control the VLA antennas much the same way it does the new EVLA antennas.





Development of the CMP is relatively far along, the SLC Driver section of the CMP software is nearly complete. Obviously the Antenna Object side of the software cannot be started until the Antenna Class has been defined. Also, more work has to be done on hardware to increase the robustness of communications with the SLC. Nonetheless, the CMP has been connected into the VLA in parallel with the Modcomp and has demonstrated its ability to observe monitor data and send command data at a low level (it has not actually operated the VLA for observing).

Physically, the CMP is nearly all COTS equipment. It consists of a Motorola MVME-162FX Single Board Embedded Controller that resides in one slot of a 6U VME chassis and runs under the VxWorks Real-Time OS. The 162 supports four Industry Pack (IP) mezzanine modules, 3 of which are used for communications with the SLC. The IP modules used are inexpensive general-purpose digital I/O devices. The only in-house item created for the CMP is the interface cable between it and the SLC. See the "EVLA Interim Control & Monitor Processor Hardware Specification" for a detailed description of the CMP hardware and its interface to the SLC.

A very important advantage that the CMP brings to EVLA development is that a large portion of the EVLA operational software will be able to be developed and tested on the existing VLA system before actual EVLA hardware is in place.

#### 4 Preliminary Requirements of the EVLA Monitor and Control System.

The following section provides the preliminary requirements of the EVLA AMCS; as such they will be fairly generic. As system design progresses, the number of individual requirements will grow while the scope of each will narrow.

As a rule, each and every requirement will contain one, and only one, *shall* statement. Additional amplifying information may accompany the *shall* statement but this information will not contain further requirements.

It is a goal that the fulfillment of each requirement will be satisfied by various testing methods at each level of system development. In other words, during the early stages of design, each requirement will be shown to be satisfied by a particular area or areas of the preliminary design. As development progresses, and the requirements become more specific, the level of design will become more specific to satisfy each.

Requirements are separated into three major areas:

- 1) Engineering Requirements describe the engineering process by which the system is created,
- 2) Functional Requirements describe what the system must do,
- 3) Performance, Constraint and Physical Requirements describe the manner in which it must be done. This includes such factors as data rates, minimum and maximum characteristics, limitations, physical requirements of the computer and networking hardware, etc..

Requirements from entities outside of ASG (e.g. the scientific community) will reference the document and paragraph from where they were extracted.

## **4.1 Engineering Requirements**

This section addresses the issues of how the system is designed and built. It specifies engineering practices that will be used to develop the system.

### **4.1.1 General Design Goals**

- 4.1.1.1 Flexibility. The system shall be designed to minimize software modifications needed to accommodate unforeseen observing requirements that may arise during the lifetime of the EVLA. {EVLA Memo 15, 3.1.2}.
- 4.1.1.2 Commercial Off The Shelf (COTS) hardware and software shall be utilized where feasible. This is a fairly subjective requirement, it is simply here to force engineering to consider buying before re-inventing.

### **4.1.2 Milestones, Deliverables and Prevention of 'Feature Creep'**

- 4.1.2.1 Each stage of development shall be well defined by pre-determined milestones. A development stage is usually marked by a review process; for example, when a requirements specification has been 'approved' the next stage would be that of developing a design that meets the requirements. The deliverable of the design stage is the design specification which is then reviewed and the process continues.
- 4.1.2.2 Each milestone shall be marked with associated deliverable(s). Examples of this are requirements and design specifications, performance and benchmark tests, etc..
- 4.1.2.3 Each milestone deliverable shall be reviewed and 'approved' and used as the basis of the next stage of development. This will help to avoid the problem of 'feature creep' where new functionality is added without review and without being documented.

### **4.1.3 Documentation Requirements**

- 4.1.3.1 Deliverables, such as design and requirements specifications shall be uniquely identified.
- 4.1.3.2 Deliverables shall be made available in a central repository available to all who are authorized access.

- 4.1.3.3 Once a deliverable document has been 'approved' (by whatever process) it shall be frozen.
- 4.1.3.4 Changes to a frozen document shall be accomplished only by the creation of a new document. This means that if a document is changed after it has been delivered, it must be identified by a new unique ID. This usually means applying a revision number to the original document.

#### **4.1.4 Software Engineering Requirements**

- 4.1.4.1 Software shall be compiled using the same compiler for common areas of code. This simply means that each engineer should compile like code using like compilers; for instance, all of the code running under VxWorks in the Antenna Control Computer must be compiled using the same version of gcc. This will normally not be a problem as most software development systems supply or specify which compiler to use.
- 4.1.4.2 ANSI C and C++ compilers shall be utilized where applicable.
- 4.1.4.3 Sun certified Java compilers shall be utilized where applicable.
- 4.1.4.4 The version of Java to be used shall be specified and used for all areas of Java development where possible. The reason 'where possible' is mentioned is to address areas where some OS's don't support the same versions of Java. This requirement is merely to promote thought about this while choosing the version of Java to be used.
- 4.1.4.5 C and C++ programming style shall adhere to ANSI standards.
- 4.1.4.6 Style sheets shall be developed for each type of language used.
- 4.1.4.7 Source code shall provide detailed functional description(s) of the module within the module itself.
- 4.1.4.8 Java source code shall utilize and comply with Javadoc standards.
- 4.1.4.9 A central repository for all deliverable software and related computer files shall be utilized.

- 4.1.4.10 All delivered human generated documents such as source code, HTML code, Makefiles, etc. shall be controlled under a Version Management system such as CVS or SCCS.
- 4.1.4.11 Software shall be designed to accommodate system growth. The EVLA will eventually utilize more antennas than the original 27; software should avoid the use of hard-coded limits for any areas that might see future change.
- 4.1.4.12 Software shall be designed with modularity in mind. The goal of this requirement is to mandate that the software be designed as robust and flexible as possible. Functionally divided areas of software should be as standalone as possible so that future changes to one will not cause adverse affects to others; this is called *loose coupling*. For an example of a system with tightly coupled modules see the VLBA's VLDIS system where dozens of global variables are used. One simple variable name or type change will cause probably 90% of the modules to fail compiling.

#### **4.1.5 Hardware Engineering Requirements [should this be here?]**

- 4.1.5.1 Circuit boards built by NRAO that are exposed to the environment shall be protected with a suitable fungus and corrosion protection coating such as MFP.
- 4.1.5.2 and so on with whatever Hardware Engineering wants to put here - if anything.

#### **4.1.6 Component Names and Naming Convention**

- 4.1.6.1 This requirement is presented only to stimulate discussion that should result in a concrete list of names for the various EVLA AMCS components that can be agreed upon (or at least acknowledged) by all. The names of the various components of the EVLA AMCS shall be as follows:
- Antenna Control Computer (ACC) - for the computer that controls an individual antenna.
  - Array Control Computer (???) - for the computer that controls the whole array.
  - Module Interface Board (MIB) - for the microcontroller that interfaces to the hardware devices and the Antenna Control Computer.
  - [TBD]

- 4.1.6.2 A naming convention(s) shall be adopted and agreed upon by both hardware and software personnel for identifying those hardware/software components common to both disciplines. This is different than the requirement above which simply names major block level components. This requirement is to force adoption of a naming practice that can be applied to all lower level items in the hardware/software system. For example a monitor point, such as Antenna 13's ACU's azimuth servo position might be named ANT\_13\_ACU\_AZ\_POS.

## 4.2 Functional Requirements of the Monitor and Control Subsystem

### 4.2.1 Hybrid Array Operation {EVLA Memo 15, 3.1.1}

- 4.2.1.1 The EVLA AMCS system shall support simultaneous operation of the old VLA antenna systems and the EVLA antennas during the transition phase.
- 4.2.1.2 Array down time shall be minimized as much as possible.
- 4.2.1.3 Operations using the old VLA shall be possible using the current OBSERVE/OBSERVE script files. [Why? It is intended that the CMP should operate the old array with the new observe system.]

### 4.2.2 Built In Test (BIT), Failures, Errors, Warnings and Data Flagging

- 4.2.2.1 A *failure* shall be defined as a condition where a portion of the system does not work. It is generally caused by a fault. A 5-volt power supply reading of zero volts will generate a failure.
- 4.2.2.2 A *warning* shall be defined as an 'un-normal' condition that is non-catastrophic to the operation of the system. It is generally caused by an out-of-tolerance condition. A 5-volt power supply reading of 4.7 volts might result in a warning.
- 4.2.2.3 An *error* shall be defined as a condition that is illegal or undefined that (would) result in data loss or an illegal equipment condition. [This needs work]
- 4.2.2.4 Failure, Error and Warning conditions shall be reported by a descriptive message. This doesn't preclude other methods of communicating the condition to the operator (such as a flashing icon).
- 4.2.2.5 Failure, Error and Warning messages shall indicate if they are a failure, error or warning.
- 4.2.2.6 Failure, Error and Warning messages shall convey the severity of the condition.

- 4.2.2.7 Failure, Error and Warning messages shall identify the consequences of the condition in terms of operational impact (data corruption, equipment safety, etc.).
- 4.2.2.8 Failure, Error and Warning messages shall identify the root cause of the condition.
- 4.2.2.9 Failure, Error and Warning messages shall suggest corrective action.
- 4.2.2.10 The Failure, Error and Warning Reporting system shall be designed so that only messages of a meaningful nature - that won't be ignored - are reported. This is another subjective area; the idea it is trying to convey is that we don't want a situation where an important alert is lost in the noise of an overwhelming number of trivial messages. The VLBA Checker screen is a good example of how it shouldn't be done.
- 4.2.2.11 Failure, Error and Warning messages shall apply, but not be limited, to the following areas:
- Loss of communications with a device or subsystem,
  - Device errors,
  - Out of range monitor points,
  - Invalid commands to a device,
  - Network failures,
  - Software based errors such as math errors, I/O errors, etc.
- 4.2.2.12 Built In Test (BIT) shall be incorporated. The extent of which is not known at this time. At the least it will be a 'health' status maintained by each MIB, but it could be periodic confidence tests initiated and performed by either the Array Control Computer or MIB.
- 4.2.2.13 Hardware shall be responsible for its own safe operation. This means that the hardware must be able to prevent itself from entering into a catastrophic condition even if commanded to so.
- 4.2.2.14 Hardware shall report an error condition if the software attempts to command it into a catastrophic condition.



- 4.2.2.15 Hardware shall report an error condition if it finds itself in a catastrophic condition.
- 4.2.2.16 Software shall be responsible for the reporting of out-of-range conditions.
- 4.2.2.17 Operations software shall have the ability of [or be responsible for?] setting its own tolerance ranges. This is not to mean that range checking (against the specified tolerances) will not be carried out in the Antenna Control Computer, only that the Antenna Control Computer will not specify the tolerances. The reason for this is that different types of antenna operations are possible (normal observing, maintenance testing, etc.) and each should be able to specify their own tolerances.
- 4.2.2.18 The AMCS shall support the retrieval of Flagging Data by EVLA operators and astronomers. {EVLA Memo 15, 3.2.10}.
- 4.2.2.19 Flagging data shall be constructed by the AMCS mainly from monitor data. {EVLA Memo 15, 3.2.10}.
- 4.2.2.20 Data shall be flagged when pointing errors exceed a specified threshold. {EVLA Memo 15, 3.2.10}.
- 4.2.2.21 Data shall be flagged when local oscillators are not locked. {EVLA Memo 15, 3.2.10}.
- 4.2.2.22 Data shall be flagged when shadowing occurs. {EVLA Memo 15, 3.2.10}.

### 4.2.3 Hardware Software Interface (the MIB)

These requirements are aimed at providing a standard for communicating data between the software and the antenna hardware. They are a little more specific for this stage of development because they are known from past experience. It is also generally known that the communications to the hardware will be via a standardized, in-house built, micro-controller called the Module Interface Board (MIB). The term hardware is not restricted to just the MIB (it can also mean the device it is connected to) but the term MIB does refer to the MIB specifically.

- 4.2.3.1 The MIB shall have the concept of time. The details of this will be decided later as we know more about the MIB itself. It would be desirable to have TOD to about the millisecond accuracy.
- 4.2.3.2 Monitor data shall be time stamped. It is not yet known who will do this, but it will be one of two places: the Antenna Control Computer or the MIB.
- 4.2.3.3 There shall be no special diagnostic ports, located in the antenna, that could provide monitor and control information not available to the rest of the AMCS. This is not to preclude test points, indicator lights, panel gauges and etc. that would normally be in and around equipment. It simply means that any monitor and control data conveyed by the MIB must be available to the whole AMCS.
- 4.2.3.4 All communication between the software and hardware shall be via the MIB.  
[are we sure?]
- 4.2.3.5 Every Control Point shall be readable. In other words, the last value written to it can be read back from it at any time.
- 4.2.3.6 Every Monitor Point shall be read only.

- 4.2.3.7 Every Monitor Point reading shall reflect the actual state of the device being monitored as opposed to merely an echo of the last command sent. This is not requiring that the actual value of a device parameter be available - in some cases this would not be to our best advantage. Such is the case of an LO where it is of more value to know simply whether or not it is locked to the commanded reference frequency as opposed to knowing the actual frequency of the LO itself. In that case, a simple lock status would reflect the 'actual state' of the device.
- 4.2.3.8 Since Monitor Points reflect the actual state of the hardware, they shall not be resettable by software. This does not mean that software cannot issue a device reset which will cause the device to reset itself - it means that software is not allowed to change the contents of a monitor point which then may no longer reflect the actual state of the hardware.
- 4.2.3.9 A Monitor Point shall have an indicator of its health. This means that no ambiguity can exist as to whether a value is truly zero or if the device is not present.
- 4.2.3.10 Every Control Point shall have a corresponding Monitor Point. This simply means that every device that can be controlled must also be able to be monitored.
- 4.2.4 Interactive Observing** {EVLA Memo 15, 3.1.3}
- 4.2.4.1 The Monitor and Control Subsystem shall provide required data and receive EVLA control parameters from the interactive control and data displays (over the internet). [This may need refinement]
- 4.2.4.2 The AMCS shall provide required data and imaging control parameters to the on-line imaging pipeline.
- 4.2.5 Subarrays** {EVLA Memo 15, 3.2.6}
- 4.2.5.1 Two levels of subarraying shall be supported by the AMCS: 1) where the VLA operations staff will assign antennas to specific observing programs and 2) where the observing programs may freely schedule their antennas into subarrays.

#### **4.2.6 RFI Detection and Excision {EVLA Memo 15, 3.2.6}**

There are no concrete plans yet for an RFI Detection and Excision system but it is agreed that such a system is highly desirable if not needed. The following requirement is in place simply to remind us that the system should be designed to accommodate a future observer/operator RFI alert system.

- 4.2.5.1 The system shall accommodate the control and monitoring of a separate RFI monitoring radiometer if such a system is built in the future.

### **4.3 Performance, Constraint and Physical Requirements of the AMCS**

#### **4.3.1 Time Frame {EVLA Memo 15, 3.2.3}**

- 4.3.1.1 UTC and VLA LST shall be used in all interfaces involving humans. .
- 4.3.1.2 Dynamic scheduling tools shall use VLA LST.
- 4.3.1.3 Scan stop time in the observing control scripts (or their EVLA equivalent) shall be in VLA LST.
- 4.3.1.4 UTC and VLA LST should both be available on the interactive control and display screens.
- 4.3.1.5 Control scripts shall use only UTC time tags.
- 4.3.1.6 Archived data shall use only UTC time tags.

#### **4.3.2 Operational System Requirements**

These requirements specify what is needed by the AMCS from the Operational System in order for AMCS to meet its own performance requirements of the Scientific Community.

- 4.3.2.1 The operational system shall supply source position with a precision of 10 microarcseconds. {EVLA Memo 15, 3.2.5}.
- 4.3.2.2 Antenna position and axis offsets shall be known to a geodetic level of accuracy. {EVLA Memo 15, 3.2.5}.

#### **4.3.3 Hardware Reconfiguration and Dynamic Corrections**

- 4.3.3.1 The AMCS shall support frequency switching within a receiver's band at the rate of 1 second. {EVLA Memo 15, 3.2.1}.
- 4.3.3.2 The time it takes for hardware to initiate a frequency change within a receiver's band after the scheduled time of the change shall not exceed 100 microseconds. {EVLA Memo 15, 3.2.1}.

- 4.3.3.3 The time it takes for the hardware to complete a frequency change within the receiver's band shall be limited only by the LO settling time. {EVLA Memo 15, 3.2.1}.
- 4.3.3.4 The AMCS shall support 'nodding' source switching at the rate of 10 seconds. {EVLA Memo 15, 3.2.1}.
- 4.3.3.5 The time it takes for hardware to initiate a nodding source change after the scheduled time of the change shall not exceed 100 microseconds. {EVLA Memo 15, 3.2.1}.
- 4.3.3.6 The time it takes for the antenna to complete a nodding source change shall be limited only by the serving settling time. {EVLA Memo 15, 3.2.1}.
- 4.3.3.7 The CALC program calculates local azimuth and elevation angles as part of its normal operation. To keep the antenna pointed to a sub-arcsecond level of accuracy, the pointing servos shall be updated with new az/el's at least every 50 milliseconds. {EVLA Memo 15, 3.2.7}.
- 4.3.3.8 Antenna Focus shall be corrected in real-time. {EVLA Memo 15, 3.2.11}.

#### **4.3.4 Physical Requirements of the Antenna Control Computer**

Little is known at this time about the physical attributes of the Antenna Control Computer because it has not been decided. It is also not known, at this point, where the computer will be physically located and how many; although it is known that it will be one of three configurations:

- 1) A few computers operating many antennas located in the Control Building.
- 2) One computer per antenna located in the Control Building.
- 3) One computer per antenna located in the antennas.

The computers themselves will most likely be VME or CompactPCI single board processors utilizing the PowerPC architecture based on its superior real-time performance over the Pentium architecture, in areas such as interrupt latency times. Past experience has shown FLASH RAM to be a desirable feature as it allows persistent retention of operating system software and possibly application software over power outages yet can be rewritten in the field much easier than EEPROM or other ROM devices.

The Antenna Control Computers will not need their own hard drives nor large amounts of RAM. The preceding of course is based upon a one-for-one correspondence of processor to antenna; if one or a few processors control all of the antennas than more systems resources will be required for each processor.

If the processors are to reside in the antenna, than a suitable RFI shielding will have to be utilized. As many antenna electronic components are digital in nature with faster and faster switching speeds, RFI shielding applies to many areas of antenna electronics not just the control computer.

#### **4.3.5 Physical Requirements of the Array Control Computer**

[TBD}

## 5 Design Considerations

### 5.1 The Antenna Control Computer

There has been some debate over whether the Antenna Control Computers should reside in the Control Building or in the antennas themselves. The arguments for a few centrally located processors include reduced cost because less processors are needed, the processors don't have to be 'weather-proof' and the chassis will not have to be RFI shielded like it would if it were located in the antenna.

It is of the author's opinion that the Antenna Control Computers should reside inside the antennas. The reasoning is presented here.

First, if the Antenna Control Computer is located in the Control Building, managed switches will have to reside in the antenna in its place to route the Ethernet interface to the MIBs. The cost of these switches may well approach that of a 'low power' single board processor and associated multiport Ethernet interface hardware - this is being researched now. Since managed switches also contain microprocessors and switching logic, they too will have to meet RFI shielding and weather-proofing requirements; in fact, there will be many such electronic devices in the antenna (like the MIBs) that are microprocessor based and will have the same concerns.

Second, if the Antenna Control Computer is located in the antenna, the following advantages will be realized.

Flexibility. If the antenna computer is tightly coupled to the antenna itself it has a greater range of options for communicating with the hardware. Granted, the majority of hardware devices will interface via the MIB over Ethernet however, it is likely that other devices using other interface types such as RS-232 may be desired; this is not physically possible if the antenna controller resides in the control building.



Modularity. An Antenna Control Computer that is physically part of the antenna will allow the antenna to be a wholly self-contained instrument capable of operation from a wide variety of sources. Three such sources of control have been defined in the requirements above; 1) normal observing system, 2) special observing systems and 3) the technician's 'laptop' maintenance system. An integrated control computer and antenna will provide a single well-defined interface that all operation processes can connect to whether they are inside the antenna itself, at the control building or across the country.

The few, centrally located, computers model has already resulted in confusion about the 'technician's laptop' maintenance computer with regard to where and how it will interface to a particular antenna and what will be required of it to operate an antenna for maintenance purposes. If the ACC is located in the Control Building, and if the technician wants to operate the antenna locally then his laptop will have to assume the duties of the Antenna Control Computer in addition to his specialized operational software in order to stimulate the antenna. This duplication of functionality is disadvantageous and will lead to confusion in areas such as antenna performance testing. ("Is the antenna acting this way because there is something wrong with it, or because there is something different between the control software in the technician's laptop and that of the Antenna Control Computer").

Maintenance. An integrated antenna and controller will allow an antenna to be easily taken off-line and operated differently than the others without affecting the operation of the others. This may not be the case where one computer is responsible for controlling many antennas. Failure of an independently controlled antenna means only that antenna is affected; one computer controlling many antennas presents another single-point failure area that can affect many antennas.

With these thoughts in mind, we should carefully weigh the long-term cost, maintenance and performance implications of designing the system around up-front monetary costs alone.

## 5.2 The Array Control Computer

Little has been said about the Array Control Computer throughout this document. The reason for this is that, during the course of writing this document, a general negative feeling has arisen as to the actual *need* of an Array Control Computer - at least in the real-time sense. It is possible that the Array Control Computer will turn out to be nothing more than a system to translate observe scripts into vectors (one for each antenna) of Antenna Objects where each Antenna Object represents the state of an antenna at a particular moment in time. This possibly does not have to be done in real-time and certainly will not require a dedicated computer. Of course there are other aspects of operating the array such as monitor data archiving, system monitoring, etc., that must be considered, but it is not obvious (at least at this stage of development) that a dedicated Array Control Computer is needed.

## **EVLA Antenna Monitor & Control Subsystem Preliminary Requirements Specification**

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