

From bsahr Fri Dec 22 11:56:47 2000
To: jbenson, jjackson, ghunt, bwaters, ksowinski
Subject: Re: a naive question
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----- Begin Included Message -----

From Brent.Carlson@hia.nrc.ca Thu Nov 2 16:00 MST 2000
Date: Thu, 02 Nov 2000 14:59:00 -0800
From: B Carlson <Brent.Carlson@hia.nrc.ca>
Organization: National Research Council of Canada
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To: Bill Sahr <bsahr@zia.aoc.NRAO.EDU>
Subject: Re: a naive question
References: <200011022212.PAA00577@mnemosyne.aoc.nrao.edu>
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Hi Bill:

Some answers to your questions...

> For a while now there has been a question in the back of my mind
> concerning the correlator backend...
>
> In very simplistic terms, my question is, where is the "throttle" on
> the correlator backend ?

The hardware and LTA integration time is completely controlled by the "DUMPTRIG" signal coming from the Station Boards (refer to Memo# 001). When a dump is to occur, a hardware signal goes to the correlator chip and it dumps the data into its buffer registers and sets some sort of interrupt or flag to the "Hi-speed Readout/LTA controller" (an FPGA that is acting like a dumbed-down, but very fast CPU). This controller reads the data out and stuffs it into LTA RAM: this "stuffing" is one of starting a new accumulation bin, adding to an existing accumulation bin, or adding/starting accumulation into a phase bin. A timestamp from the hardware "TIMECODE" signal is also saved with the data (if appropriate at the time). Each correlator chip will essentially have a specific region of LTA RAM where its data gets deposited (actually, many "chunks" within its region so ample buffer space is available) and then the readout controller will set some semaphore in RAM when data is ready...the PPMC or PC processor's job is to essentially poll the LTA RAM looking for these semaphores and then to read out data that is ready. If the readout controller runs out of RAM to deposit some correlator chip's data into, then an overflow condition occurs and, in my opinion, no more data from that correlator chip gets dumped until its region of memory gets read out and semaphores are cleared.

This is a very hardware oriented mechanism that, I believe, is required to meet the performance requirements of the system. Because of the clock rate, it will be necessary to dump data from all correlator chips about every ~8 msec even if

the LTA accumulation time is much longer. Also, the astronomers want very high speed dumping for pulsar phase binning, and in some cases high speed sustained dumping...and there is the requirement to design the correlator to be essentially bottleneck free so that it is only the back-end computing that limits performance. (There may, in fact, have to be more than one readout controller on a Baseline Board, because sub-millisecond pulsar phase binning appears to be a requirement :-)).

So, after all that, to answer your question, the "throttle" is set by some programmable timer on the Station Board that generates DUMPTRIG. The correlator chip is able to select whether it dumps data based on DUMPTRIG from the X or Y station. This does limit the flexibility some because it is station-based dumping, but no one could come up with a reason why it wouldn't be ok.

> As an initial spec, we are aiming to take data
> from the correlator at a rate of only 20 to 25 Mbytes per second. So,
> what synchronizes the readout of the data from the LTAs with the writes
> of data to the LTAs ?

I think that if a PPMC card is used, interrupts can be generated by the Hi-speed readout controller to the CPU that a semaphore is set and that it is time to read data. Or, the CPU could just be constantly polling the semaphores looking for data that is ready.

> How does whatever is responsible for initiating
> a read know that a new data set is ready ?

Semaphores set by the readout controller. There could be a separate hi-speed RAM just for semaphores since using DDR SDRAM is optimized for block transfers and it should just be "chunked out" for data.

> What prevents that data
> set from being overwritten by the next set of results before the readout
> process has completed ?

Semaphores and the readout controller as mentioned above.

> What happens to the data that could not be written
> to the LTAs because an earlier data set is still being readout ?

It gets discarded...downstream processing will know this by looking at timestamps.

> Is it a
> question of how the correlator is configured at the station boards and
> baseline boards ?

Yes, the station board configuration of the DUMPTRIG timer as mentioned above and the baseline board configuration where each correlator chip can be configured to dump on an X station or Y station DUMPTRIG (or some derivative thereof).

> Are there signals in the memory access controllers ?

The memory access controller is just to make the LTA (DDR) SDRAM (Double Data Rate Synchronous Dynamic RAM) look like dual-port RAM to the PPMC and readout controller. We can't use actual dual-port RAM because it currently is not large enough to meet the minimum ~2 Gbyte memory capacity for the LTA to support the

required 1024 phase bins. To get this much memory for a decent cost is going to require using the same memory device as mass produced PCs use.

Hope these provide satisfactory answers to your questions. Peter and I will be coming to Socorro in December for the NSF site visit so we should have lots of time for informal discussions.

Regards,
Brent.

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