Dump Control, Delay Models

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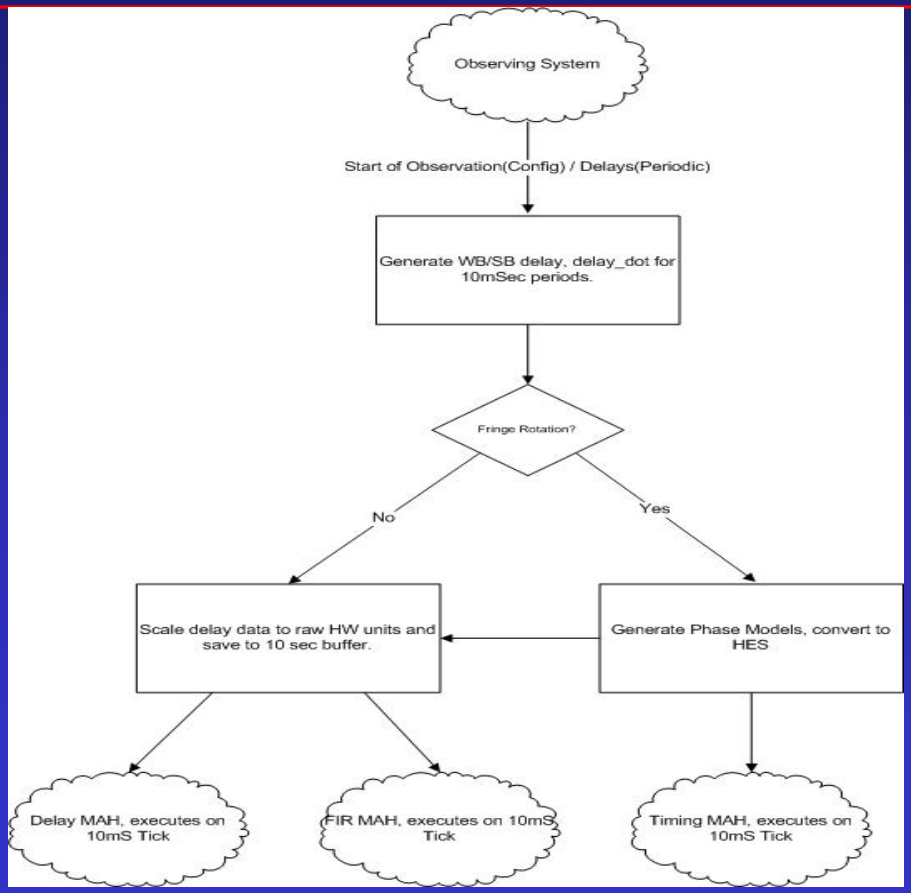
Dumptrig, Delay Models

- General
  - Implemented as user mode processes running on station board CMIB
  - Real-time component implemented in the Module Access Handler

Delay model generation

- Generates models for wideband and sub band delays
- Inputs are start of observation (config) and periodic (delay) data
- Calculates 10 seconds worth of delay/phase data
- Transforms delay polynomials into raw HW units
- Data time tagged for execution synchronous with 10 mS tick

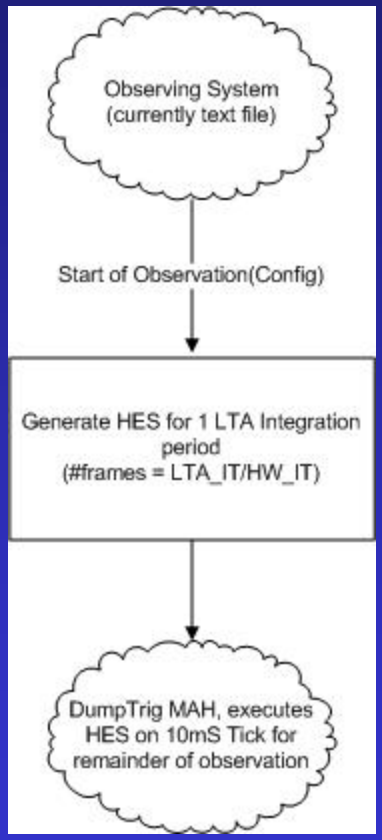
Delay model generation



Dump Control

- Creates Hardware Executable (HES) defining dump sequences for BB/SB pairs
- Inputs are start of observation data, currently derived from text files
- Generates HES for one LTA integration period (except burst mode)
- Currently implemented modes are Normal, Recirculation, and Burst
- Limited testing performed, verified HES executed w/o CRC errors.

Dump Control



Dumptrig, Delay Models

- Future Challenges
  - Replace configuration text files (dumptrig) with data from Observing System
  - Pulsar binning, Recirculation w/ Pulsar binning
  - Testing through back end
  - Succession planning

Questions?