NRC · CNRC

Expanded
Very Large Array

Software Requirements for the Testing of Prototype Correlator

Sonja Vrcic

NRC · CNRC

Purpose

- Basic setup and requirements for each stage
  - Control software: how is the correlator configured and controlled ?
  - Interfaces: what input does the correlator require, and what output must it produce ?
  - Is software integration required ?
  - Organization & storage of data & metadata:
    - which data must be kept;
    - data formats;
    - data assemblers;
    - archives;
    - data output rates.
  - Examination of data & metadata (analysis programs)
- Are we tacking all the major pieces ?
- Are there major missing bits ?

NRC · CNRC

- This presentation is based on the NRAO document:

"WIDAR Prototype Correlator, Schedules, Testbeds, Software" Version 3.0

Author: Bill Sahr

As requested, diagrams from the document are provided here for review, although WIDAR test plan has been modified.

NRC · CNRC

Software Requirements For the Stage 2 Acceptance Testing in DRAO Q1 2008

- Station Board and Baseline Board will be independently tested.
- At this phase test environment is rather low-level and manual.
- Control software:
  - CMIB software (Device Drivers, Module Access Handlers, Data Streaming). Some upgrades are needed, most notably for new RXP FPGAs on Baseline Board.
  - GUIs developed for Stage 1 testing. Some upgrades are needed, most notably for new RXP FPGAs on Baseline Board.
  - Power monitor & control (CPCC) HW and SW is not needed at this time.
- Input:
  - External input data is not needed, on-board test pattern generators will be used.
  - Externally generated (real-time) models are not needed, models will be prepared and loaded together with Test Vector.
- Output:
  - Output is stored in files and examined/analyzed by utility programs developed for Stage 1 (RTDD, Intelligent Diff, utility programs that capture BLB output).

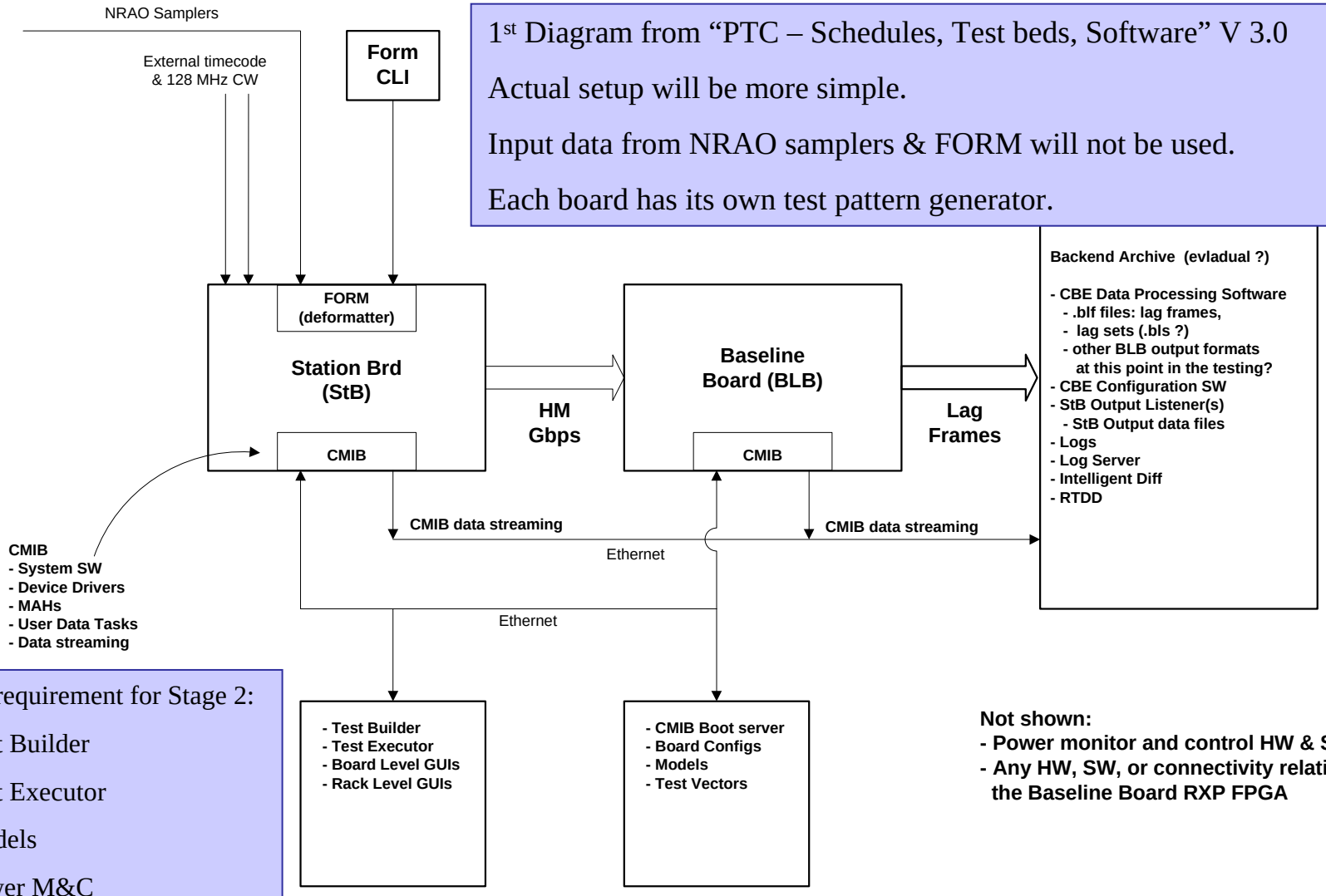
Stage 2 Acceptance Testing - Q1 2008

1st Diagram from "PTC – Schedules, Test beds, Software" V 3.0

Actual setup will be more simple.

Input data from NRAO samplers & FORM will not be used.

Each board has its own test pattern generator.



Not requirement for Stage 2:

- Test Builder
- Test Executor
- Models
- Power M&C

Not shown:
- **Power monitor and control HW & SW**
- **Any HW, SW, or connectivity relating to the Baseline Board RXP FPGA**

NRC · CNRC

Further Software Development

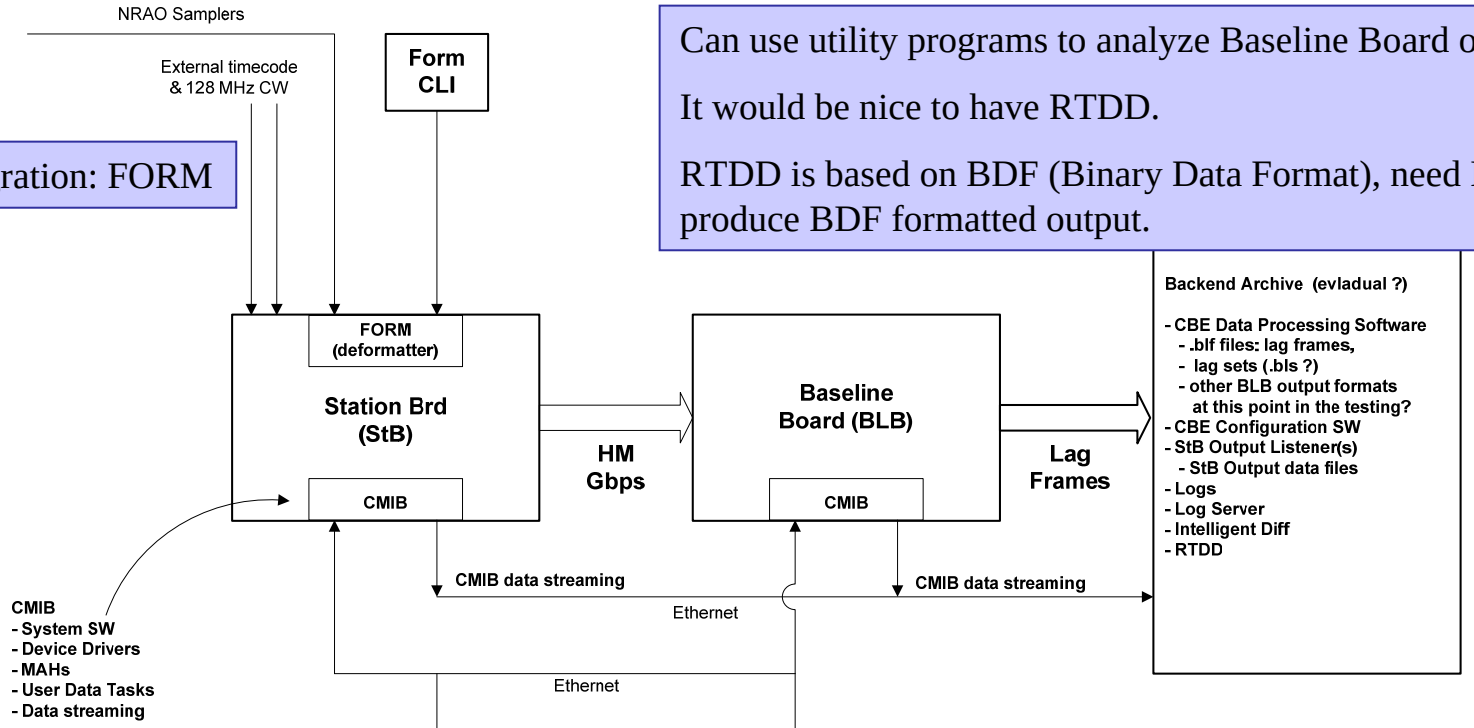
- In parallel with testing of Stage 2 boards, software for the Station Board and Baseline Board needs to add more and more functionality in preparation for the full integration and on-the-sky testing.
- For example, real-time software such as:
    - Delay tracking
    - DUMPTRIG generation
    - PHASEMOD generation

NRC · CNRC

Single Baseline Hardware at VLA (End Q1 2008)

- If stage 2 if successfully completed, single baseline hardware will be sent to VLA to begin **early on-the-sky testing**.
- The setup for this phase will be (more-or-less) as shown in the Bill's diagram for stage 2 acceptance.
- Fiber Optic Receiver Module (FORM) must be integrated into system. Note that FORM interface is not / and will not be integrated into WIDAR Monitor & Control. FORM is part of Antenna System and will be controlled by Antenna Monitor & Control System.
- Station Board must be able to
  - process externally generated delay models.
  - generate DUMPTRIG
- Basic MCCC functionality will also be needed to forward models to CMIB.
- Small number of boards can be configured using board GUIs, i.e. Test Builder & Executor are not essential (not required).
- Power Monitor & Control is required (basic functionality).
- Utility programs & RTDD can be used to analyze output.
- Requirements for archive & data analysis – to be defined.

Diagram: Single Baseline H/W at VLA – End Q1 2008



Integration: FORM

Can use utility programs to analyze Baseline Board output.

It would be nice to have RTDD.

RTDD is based on BDF (Binary Data Format), need Backend to produce BDF formatted output.

Test Builder & Executor still not essential.

Can use board GUIs.

Power M&C is required.

Not shown:
- **Power monitor and control HW & SW**
- **Any HW, SW, or connectivity relating to the Baseline Board RXP FPGA**

Not shown in this diagram:

Models received from Antenna M&C

NRC · CNRC

Stage 3 Testing: 14 Station Boards and 14 Baseline Boards (Q2 2008)

At this time an automated testing environment will be needed.

- GUI based **Test Builder** that will allow user to create a Test Case which consists of configuration for:
  - Station Board (STB)
  - Baseline Board (BLB)
  - STB and BLB Output Data Listeners, including names/paths for output files,
  - Intelligent Diff including set of "golden files", etc.

- A **Test Case** is an XML file which may contain pointers to (i.e. names of) other XML files which contain configuration for individual components (e.g. boards).

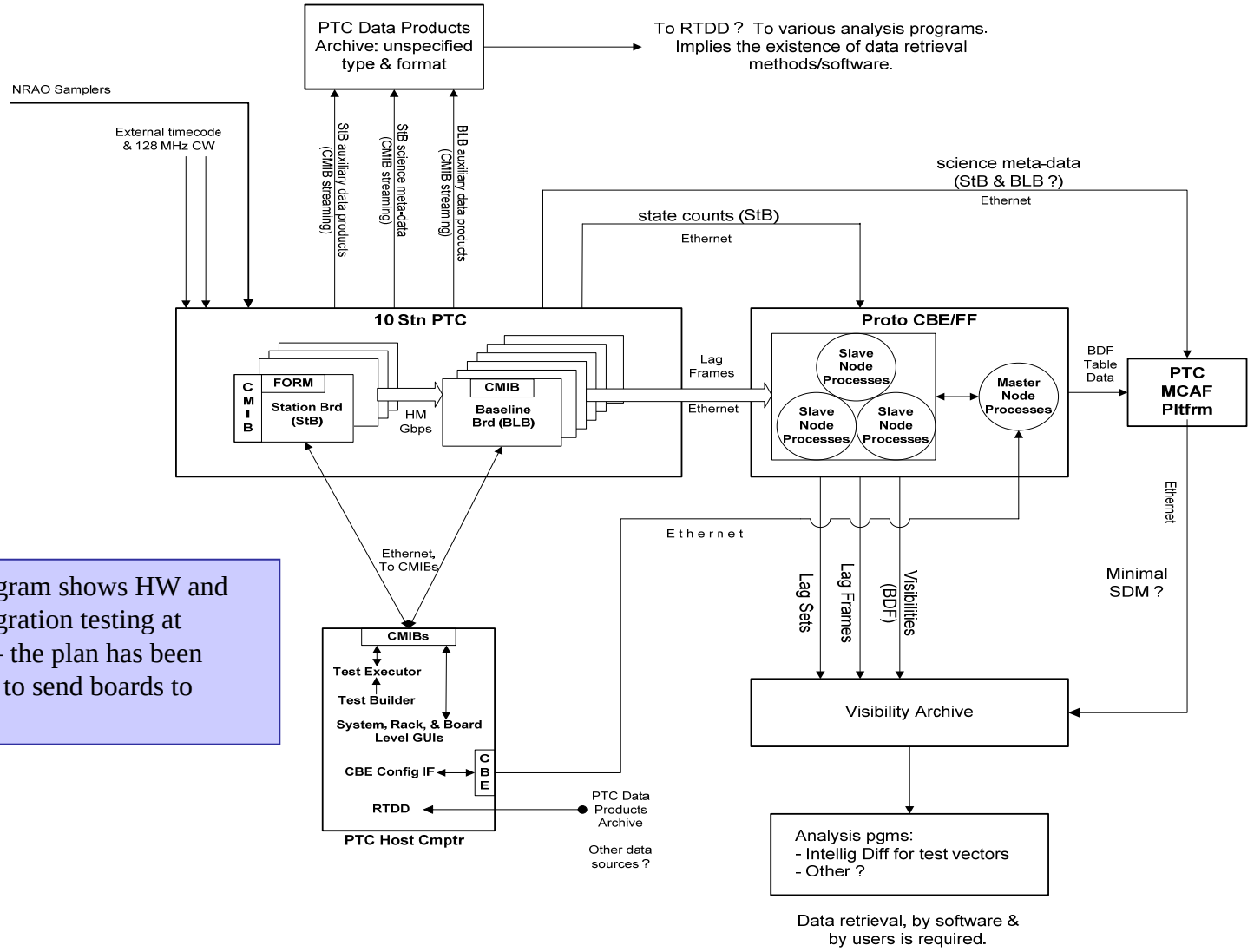
- GUI based **Test Executor** that will use Test Cases as input. Test Executor allows user to specify:
  - List of Test Cases
  - Start time
  - Duration for individual Test Cases
  - How many times to repeat test, etc.

NRC · CNRC

Test Setup for Stage 3

- Except for the additional software requirements (i.e. test automation) the setup for Stage 3 is the similar as for Stage 2.
- At this time Station Board should be able to generate input for Baseline Board (see early OTS).

Diagram from "PTC – Schedules, Test beds, Software" V 3.0



This diagram shows HW and SW integration testing at DRAO – the plan has been changed to send boards to VLA.

NRC · CNRC

Critical OTS Testing (VLA)

- According to the current (expedited schedule) critical OTS testing would start in mid August 2008.
- The setup at VLA will consist of 10 Station Boards and 12 Baseline Boards.

Monitor & Control:

- Test Builder & Executor will be used for execution of critical hardware tests. By this time Test Builder & Executor should be fully implemented.
- Correlator Backend M&C should be integrated by this time.
- It would be nice to have rack & system level GUIs to provide overall view of the system.

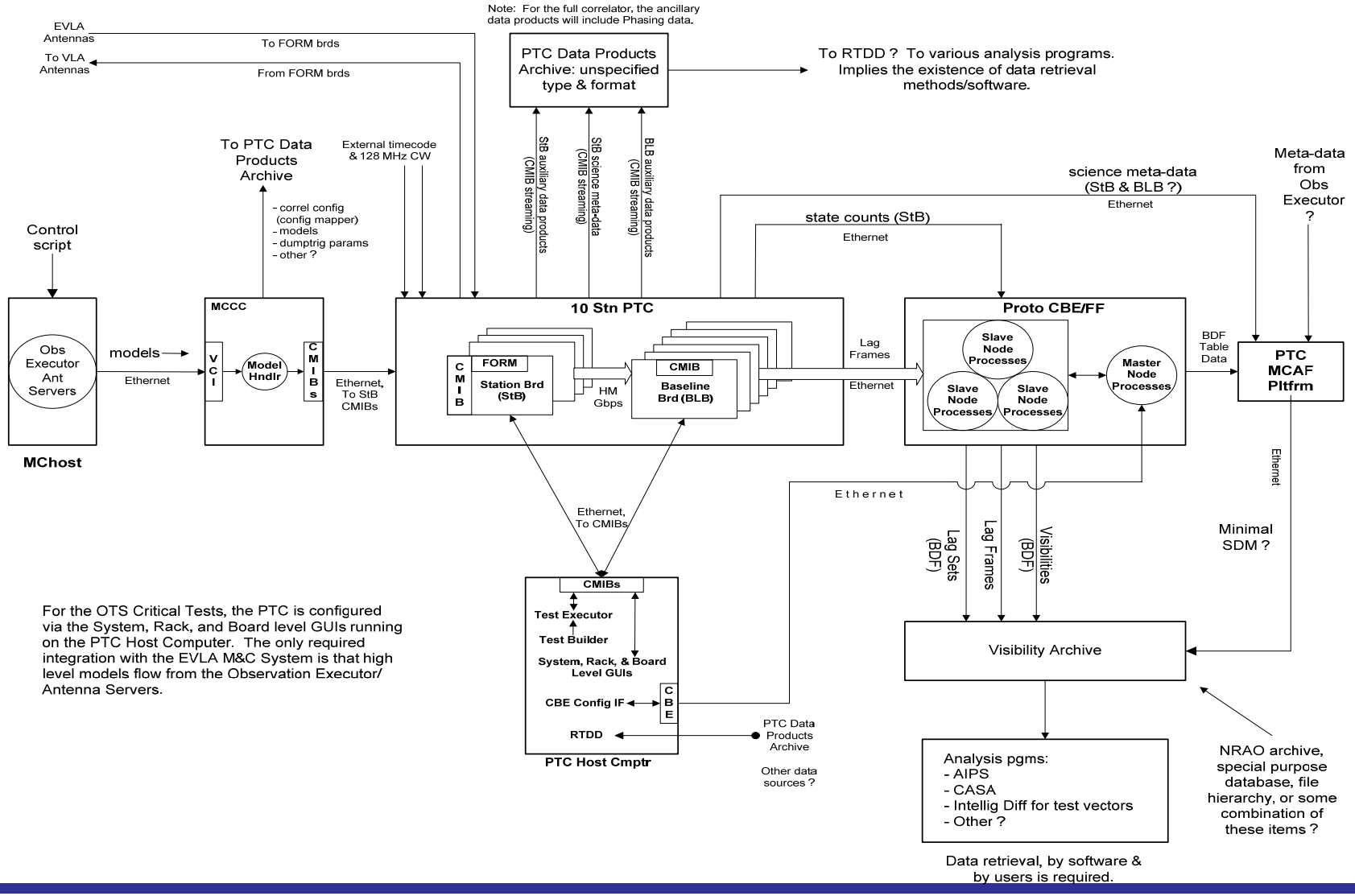
Input:

- Observed data from EVLA antennas (via FORM)
- Delay models from Antenna Monitor & Control

Output:

- Requirements to be defined.

On-The-Sky Critical Testing
Diagram from "PTC – Schedules, Test beds, Software" V 3.0



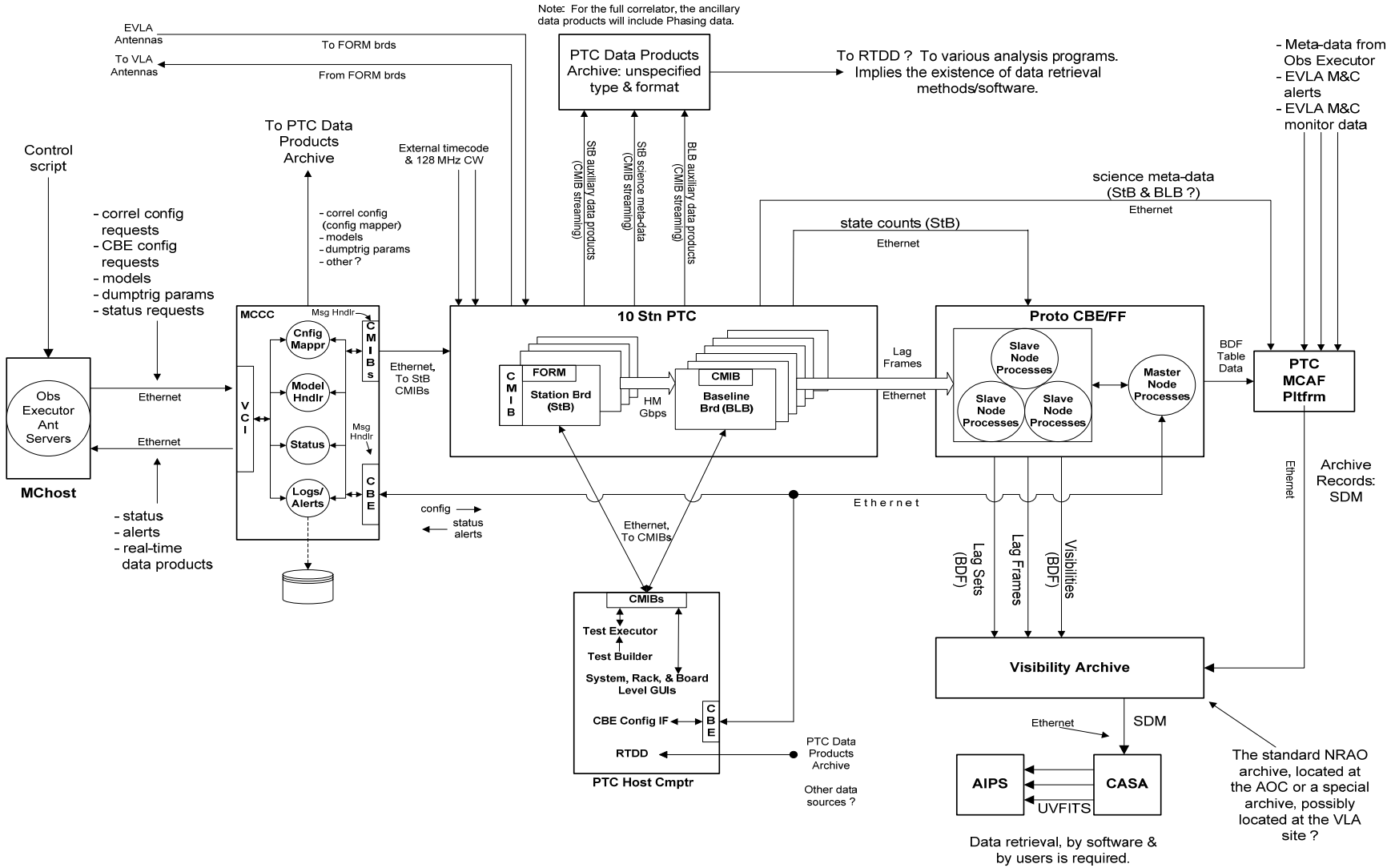
For the OTS Critical Tests, the PTC is configured via the System, Rack, and Board level GUIs running on the PTC Host Computer. The only required integration with the EVLA M&C System is that high level models flow from the Observation Executor/ Antenna Servers.

NRC · CNRC

Software Integration

- It is expected that after the critical hardware testing, the prototype correlator will be available for software integration testing.
- It would be probably better to call this phase system integration.
- WIDAR team should be concentrating first on configuration and status reporting, to provide controlled environment.
- It is expected that interface between various subsystems may start earlier, for example, interface between Observation Executor and Configuration Mapper (VCI) may be start earlier, and does not need to include hardware. The same applies for interface between Configuration Mapper and WIDAR CMIB software.
- A tool that would provide good hi-level view of the correlator configuration would be very useful.

Software Integration, Limited Observing (Q4 2008)



NRC · CNRC

Summary

- Basic setup and requirements for each stage:
  - Control software: how is the correlator configured and controlled ?
  - Interfaces: what input does the correlator require, and what output must it produce ?
  - Is software integration required ?
  - Organization & storage of data & metadata:
    - which data must be kept;
    - data formats; data assemblers; archives; data output rates.
  - Examination of data & metadata (analysis programs)
- Are we tacking all the major pieces ?Are there major missing bits ?

- Requirements for WIDAR software are well known.
- Most unknowns are in the area of output data organization, storage and analysis.