NRC · CNRC

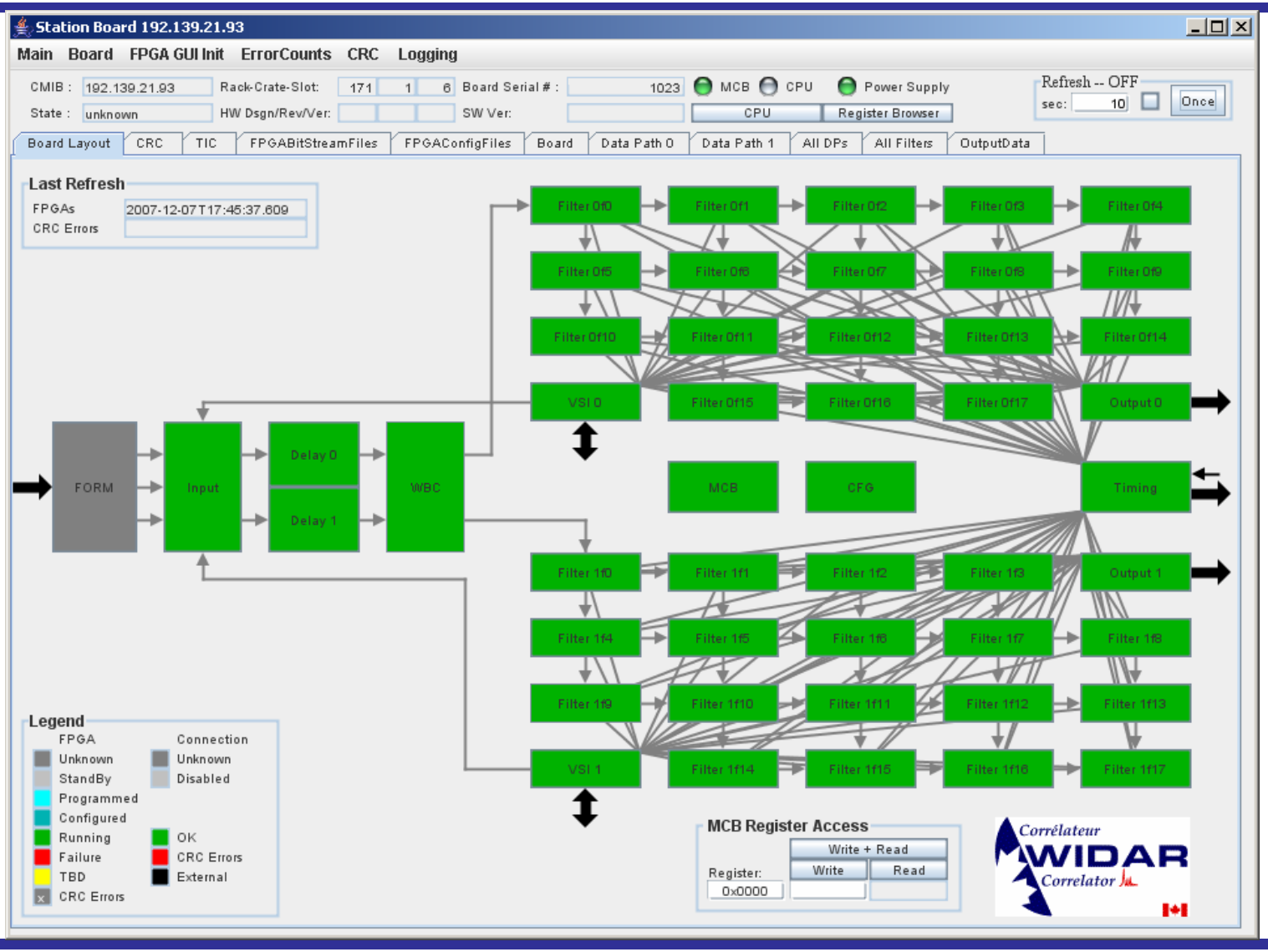
Expanded Very Large Array

Station Board

Outline

- Station Board Review
- Station Board Status
- Delay Module Status
- Filter FPGA Status
- FORM Status
- CMIB Status
- GUI Status
- RTDD Status
- IDIFF Status
- Testing Status
- Testing Schedule

Review


Station Board 192.139.21.93
Main Board FPGA GUI Init ErrorCounts CRC Logging
CMIB : 192.139.21.93
Rack-Crate-Slot: 171 1 6
Board Serial # : 1023
MCB CPU Power Supply
State : unknown
HW Dsgn/Rev/Ver:
SW Ver:
CPU
Register Browser
Refresh -- OFF
sec: 10
Once
Board Layout CRC TIC FPGABitStreamFiles FPGAConfigFiles Board Data Path 0 Data Path 1 All DPs All Filters OutputData
Last Refresh
FPGAs 2007-12-07T17:45:37.609
CRC Errors
Filter 0f0 Filter 0f1 Filter 0f2 Filter 0f3 Filter 0f4
Filter 0f5 Filter 0f6 Filter 0f7 Filter 0f8 Filter 0f9
Filter 0f10 Filter 0f11 Filter 0f12 Filter 0f13 Filter 0f14
VSI 0 Filter 0f15 Filter 0f16 Filter 0f17 Output 0
FORM Input Delay 0 Delay 1 WBC
MCB CFG Timing
Filter 1f0 Filter 1f1 Filter 1f2 Filter 1f3 Output 1
Filter 1f4 Filter 1f5 Filter 1f6 Filter 1f7 Filter 1f8
Filter 1f9 Filter 1f10 Filter 1f11 Filter 1f12 Filter 1f13
VSI 1 Filter 1f14 Filter 1f15 Filter 1f16 Filter 1f17
Legend
FPGA
Unknown
StandBy
Programmed
Configured
Running
Failure
TBD
CRC Errors
Connection
Unknown
Disabled
OK
CRC Errors
External
MCB Register Access
Write + Read
Register:
Write
Read
0x0000
Corrélateur
WIDAR
Correlator

Station Board Status

- Tests needed to proceed with the new board completed
- Two new boards are being manufactured now
  - Quoted delivery is 11 January 2008
- VSI FPGAs will be installed on one board at DRAO
  - Both types have to be tested.
- Board Testing should take one week if nothing is wrong
  - Uses CRC and TIC measurements, FIR comparisons, ...
  - The board without the VSI FPGAs needs external PPSCODE
- JTAG test development could take another week or two
  - Need to decide whether Delay Module is installed for test.
- The next 14 boards could be done with or without JTAG
  - Could be delivered by 01 April 2008

Delay Module Status

- Old Delay Module works but too expensive
  - Functional tests complete for ‘4’-bit samples
- New Delay Module undergoing tests now
  - First tests to decide when to manufacture 32 more
  - Only address lines untested
- May need to move termination resistors away from FPGA
  - Needed to allow replacement of faulty FPGA => re-spin
- Need to be complete at same time as the 14 Station Boards
  - End of March 2008

Filter FPGA Status

- Data output agrees with simulation (using radar mode)
  - All stages tested
  - All measurements tested
  - Delay, side-band flipper, RFI excisor, re-quantizer tested
  - 8-bit, mixer, fractional bit not yet tested
- All 36 give the same results when configured the same
  - They do this for hours
- Not too sure how stage scaling will be done OTS
  - Does sampler have AGC?
  - Dynamic? CMIB?

FORM Status

- FORM interface with Station Board works well.
- ICD needs small updates.
- OTS requires FORM firmware and software updates along with testing in NM.

CMIB Status

- Performing well - a few minor things left.
- Will require some work for new PCB.
  - Timing FPGA PPSCODE (embedded delays)
  - Timing FPGA DUMPTRIG (expansion to 16 generators)
  - MCB (more ADC values)
- Testing Delay Module Test Vector Models
  - For testing prototype system well before OTS
- Testing actual polynomial models
  - before OTS testing
  - Probably does not need to involve hardware

GUI status

- Performs well
- Nearly complete for testing purposes
  - Ability to save a board configuration needs minor fixes
- Ability to run a single test may be built in
  - Pre-cursor to Test Executor

RTDD Status

- Real Time Data Display by Dave Del Rizzo
- The RTDD receives all output tables and performs well.
- Some minor changes are needed and more testing is required.

IDIFF Status

- Will be used soon in its current form
  - Can manually edit files to remove non matching records for now
  - Can all attributes be requested now?
- Will require Intelligent diff that compares records with the same observation time for testing of multiple boards
  - Maybe end of April 2008

Testing Status

- Of 90 hardware functions to be tested (TVP)
  - 67 (75%) are complete
  - 12 (13%) are nearly complete
  - 11 (12%) have not been tested

- Of 42 software functions to be tested (TVP)
  - 6 (14%) are complete
  - 19 (45%) are nearly complete
  - 17 (41%) have not been tested

Testing Schedule

- Continue functional testing of old boards
  - Until new boards arrive – middle of January 2008
- Test new boards for PCB errors to give go-ahead for 14 more
  - Possibly complete JTAG test for 14 new boards
  - End of January 2008
- Functional testing of new boards
  - Complete by end of March 2008
- Begin testing of 14 new boards when they arrive.
  - Basic tests
  - Develop canned tests
  - Eventually needs Test Executor - middle of April 2008

Summary

- Delay Module manufacture go-ahead
- JTAG test vectors for new board
- Complete hardware-CMIB/GUI testing
- Add single test ability to GUI
- Complete hardware functional tests
- Complete Timing FPGA changes
- 14 board manufacture go-ahead
- Complete FORM interface to Station Board
- Complete RTDD repairs and testing
- Delay Module Test Vector execution tests
- Polynomial models execution tests
- Intelligent Diff with time-tag comparison
- 14 board with new Delay Module testing
- Test Executor
- Begin prototype system testing