EVLA Corr Schedule & Risk Issues

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NRC · CNRC

Outline

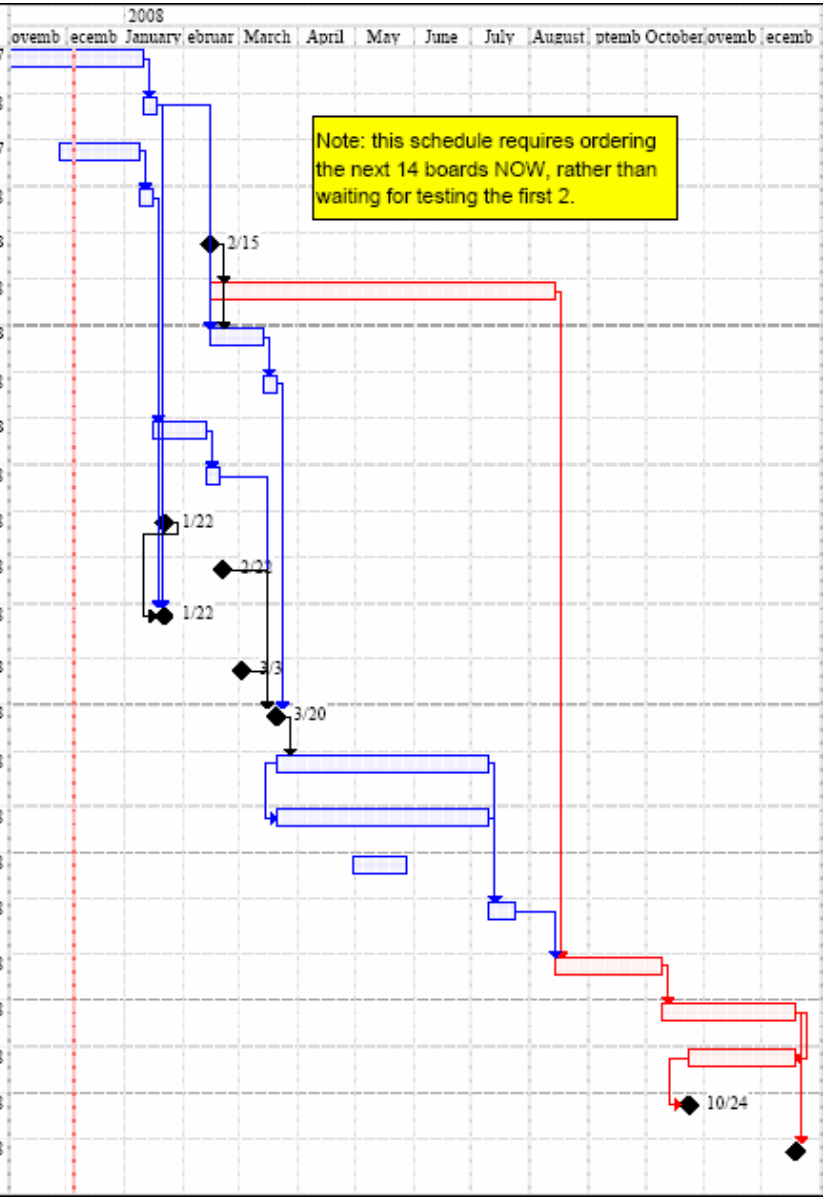
1. Schedule Options.
2. Trading risk for schedule.
3. Screening for prototypes & production.
4. Software in near term.
5. On-the-Sky tests.

Wildest Dreams Hardware Schedule

- No prototype reliability test or laboratory system integration.
- No production burn-in in Penticton.
- Expedited Station & Baseline Boards for delivery direct to VLA site.
  - Factory assembles complete board, including all daughter boards.
  - Production shipment direct from factory after quick functional test.
  - No JTAG on prototypes.
- No reliability testing on first 1200 chips (decision already made).
- Only hardware considered in this schedule analysis; software not included.
- Assumes no Re-spins.
- Remarks
  - Single baseline hardware arrives at VLA site in Jan/08.
    - How does this help?
    - Is there a risk that it could actually slow things down?
      - Support from Penticton required.
  - Obvious long-term risk impact to hardware.
  - Little sense of thoroughness.
    - Much more responsibility on NRAO.
  - NRAO takes care of all software?

Wildest Dreams Hardware Schedule

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, no JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton	Fri 1/11/08
3	Stage 2 Station Boards; qty=2; proto fabrication, no JTAG test	Wed 11/28/07
4	Stage 2 Station Boards; qty=2; functional test @ Penticton	Wed 1/9/08
5	1200 corr chips available at mfg (iSine delivery milestone)	Fri 2/15/08
6	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
7	Stage 3 Baseline Boards; qty=14; fabrication	Fri 2/15/08
8	Stage 3 Baseline Boards; qty=14; functional test @ Penticton	Fri 3/14/08
9	Stage 3 Station Boards; qty=14; fabrication	Wed 1/16/08
10	Stage 3 Station Boards; qty=14; functional test @ Penticton	Wed 2/13/08
11	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
12	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
13	**Single Baseline Tests Start: first H/W (2xSB + 1xBB) arrives a**	Tue 1/22/08
14	Next set of racks (2 SRs, 2 BRs, min) arrive at VLA	Mon 3/3/08
15	**8 more SBs, 10 BBs arrive at VLA; start full OTS testing**	Thu 3/20/08
16	**OTS testing at VLA (duration???)**	Fri 3/21/08
17	Functional test development; JTAG; full production tooling, long lead-time ordering	Fri 3/21/08
18	Final racks delivered and installed at VLA	Wed 4/30/08
19	**Critical Design Review (CDR)**	Fri 7/11/08
20	Full production: PCB fab	Fri 8/15/08
21	Full production: assy+test	Fri 10/10/08
22	Functionally tested boards delivered to VLA	Fri 10/24/08
23	Control Rack, CPUs, CBE etc install complete	Fri 10/24/08
24	**All H/W delivery to VLA complete**	Thu 12/18/08

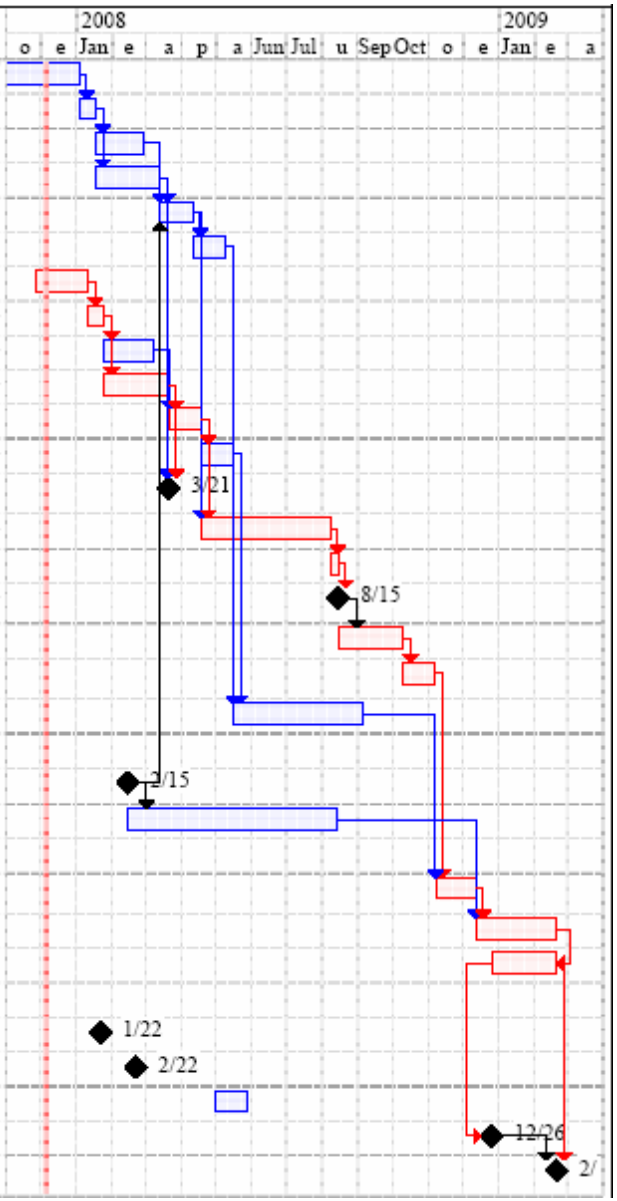


Very Optimistic Hardware Schedule

- Full prototype reliability test and laboratory system integration.
- No production burn-in in Penticton.
- Expedited Station & Baseline Boards for delivery.
  - 6 week turn on assembled boards.
- No reliability testing on first 1200 chips (decision already made).
- Only hardware considered in this schedule analysis; software not included.
- Assumes no Re-spins.
- Remarks
  - Single baseline hardware arrives at VLA site in Apr/08.
    - Useful? Supportable?

Very Optimistic Hardware Schedule

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, c/w JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/4/08
3	Stage 3 Baseline Board; qty=14 PCB fab, 6 week turn	Fri 1/18/08
4	Stage 2 Baseline Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/18/08
5	Stage 3 Baseline Board; qty=14; assembly	Fri 3/14/08
6	Stage 3 Baseline Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/11/08
7	Stage 2 Station Boards; qty=2; proto fabrication	Wed 11/28/07
8	Stage 2 Station Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/11/08
9	Stage 3 Station Board; qty=14 PCB fab, 6 week turn	Fri 1/25/08
10	Stage 2 Station Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/25/08
11	Stage 3 Station Board; qty=14; assembly	Fri 3/21/08
12	Stage 3 Station Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/18/08
13	**Single baseline H/W could be sent to VLA to begin early OTS testing**	Fri 3/21/08
14	System integration and test @ Penticton (duration????)	Fri 4/18/08
15	10 Station Boards, 12 Baseline Boards ship to VLA	Fri 8/8/08
16	**Begin full OTS testing; 10 stations, 1536 MHz/poln, at VLA**	Fri 8/15/08
17	Critical OTS testing for production go-ahead (duration???)	Fri 8/15/08
18	**Critical Design Review**	Fri 10/10/08
19	Production tooling: functional test setup, order long-lead time parts	Fri 5/16/08
20		
21	**Production corr chips delivered from iSine (how firm???)**	Fri 2/15/08
22	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
23		
24	**Start full production: Production PCB fab, all PCBs, 6 week turn**	Fri 11/7/08
25	Full production and functional test	Fri 12/12/08
26	Functionally tested H/W boards delivered to VLA site	Fri 12/26/08
27		
28	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
29	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
30	Final racks delivered and installed at VLA	Thu 5/1/08
31	Control Rack, CPUs, CBE etc install complete	Fri 12/26/08
32	**All H/W delivery to VLA complete**	Fri 2/20/09

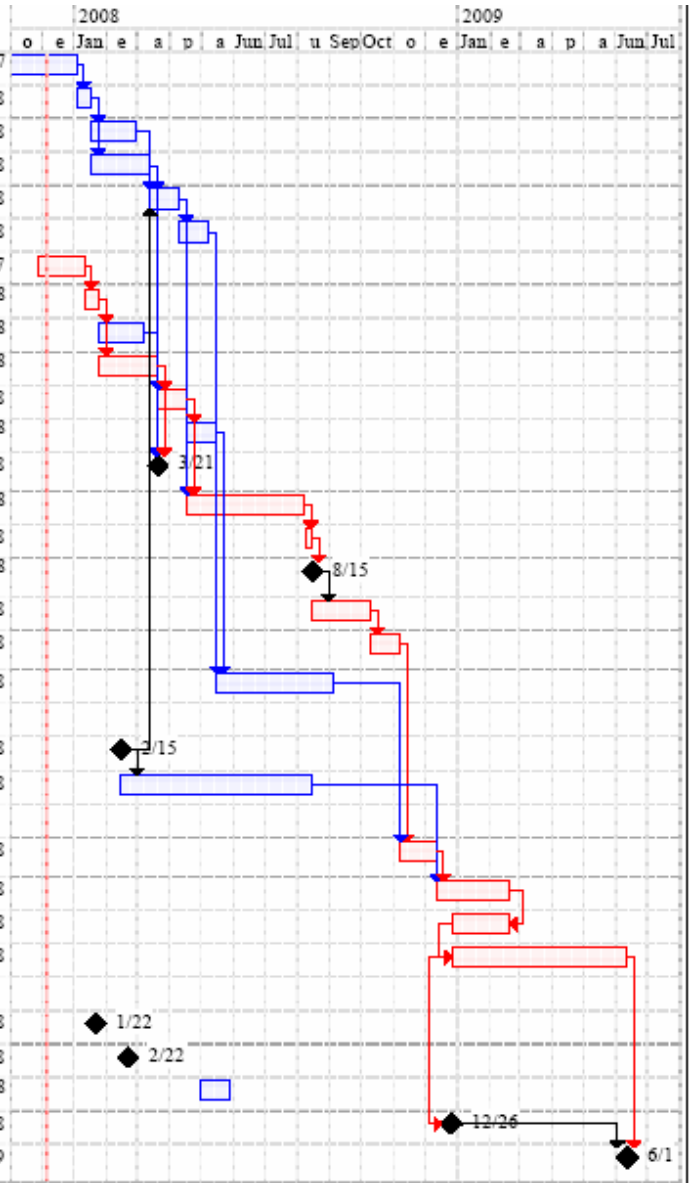


Fairly Optimistic Hardware Schedule

- Full prototype reliability test and laboratory system integration.
- Production burn-in in Penticton (two large boards per day).
- Expedited Station & Baseline Boards for delivery.
  - 6 week turn on assembled boards (saves 2 weeks).
- No reliability testing on first 1200 chips (decision already made).
- Only hardware considered in this schedule analysis; software not included.
- Assumes no Re-spins.
- This schedule fits approximately with the “Optimistic Long Term Schedule” on the web.
- 3.5 months for system integration and test in Penticton.
- OTS starts mid-Aug/08.

Fairly Optimistic Hardware Schedule

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, c/w JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/4/08
3	Stage 3 Baseline Board; qty=14 PCB fab, 6 week turn	Fri 1/18/08
4	Stage 2 Baseline Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/18/08
5	Stage 3 Baseline Board; qty=14; assembly	Fri 3/14/08
6	Stage 3 Baseline Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/11/08
7	Stage 2 Station Boards; qty=2; proto fabrication	Wed 11/28/07
8	Stage 2 Station Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/11/08
9	Stage 3 Station Board; qty=14 PCB fab, 6 week turn	Fri 1/25/08
10	Stage 2 Station Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/25/08
11	Stage 3 Station Board; qty=14; assembly	Fri 3/21/08
12	Stage 3 Station Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/18/08
13	**Single baseline H/W could be sent to VLA to begin early OTS testing**	Fri 3/21/08
14	System integration and test @ Penticton (duration????)	Fri 4/18/08
15	10 Station Boards, 12 Baseline Boards ship to VLA	Fri 8/8/08
16	**Begin full OTS testing; 10 stations, 1536 MHz/poln, at VLA**	Fri 8/15/08
17	Critical OTS testing for production go-ahead (duration???)	Fri 8/15/08
18	**Critical Design Review**	Fri 10/10/08
19	Production tooling: functional test setup, order long-lead time parts	Fri 5/16/08
20		
21	**Production corr chips delivered from iSine (how firm???)**	Fri 2/15/08
22	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
23		
24	**Start full production: Production PCB fab, all PCBs, 6 week turn**	Fri 11/7/08
25	Full production, JTAG, partial assembly at BMS	Fri 12/12/08
26	Production boards ship to Penticton.	Fri 12/26/08
27	Burn-in test H/W boards and deliver to VLA site (average of 2 large boards per day--faster???)	Fri 12/26/08
28		
29	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
30	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
31	Final racks delivered and installed at VLA	Thu 5/1/08
32	Control Rack, CPUs, CBE etc install complete	Fri 12/26/08
33	**All H/W delivery to VLA complete**	Fri 6/12/09



Optimistic Long-Term Schedule

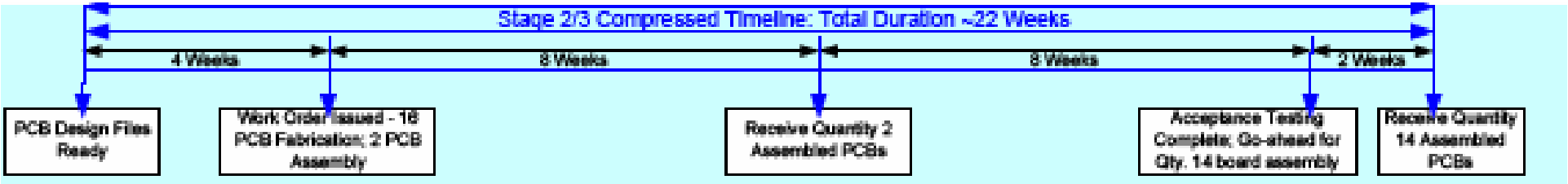
- Currently on the web.
- Approximately the same as the “Fairly Optimistic Hardware Schedule”.
  - Fairly Optimistic Hardware Schedule contains more recent analysis.
- No single-baseline hardware stage.
- OTS starts Oct 14/08.
- Change of 1Q since 30Aug schedule (July 18/08).

Optimistic Long-Term Schedule

Optimal Schedule

ID	Task Name	Start
5	Stage 2 Prototype Redesign, Fabrication, & Assembly (2 PCB)	Mon 28/05/07
6	Stage 2 Prototype Fabrication Acceptance Testing	Fri 18/01/08
7	Stage 2 Accepted; Go-ahead Stage 3 (Fab & Assy - 8 PCB)	Fri 01/02/08
8	Hardware/Software Integration Testing	Tue 20/05/08
9	Critical Design Review	Mon 15/09/08
10	Hardware for OTS Testing Sent to VLA	Tue 16/09/08
11	On-The-Sky Testing	Tue 14/10/08
12	High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site	Mon 03/03/08
13	Racks Delivered to and Installed at VLA Site	Tue 18/03/08
14	Limited Production Hardware Could Be Sent to VLA	Tue 16/09/08
15	Limited (10-Antenna) Observing	Mon 30/03/09
16	Stage 4 Production Hardware	Tue 27/01/09
17	Final Full Production Test & Burn-in in Penticton	Tue 12/05/09
18	Full Board Installation & Testing @ VLA	Tue 11/08/09
19	Commissioning - Turn off old correlator	Tue 13/07/10
21	Test Builder and Executor	Mon 03/09/07
22	MCCC Software	Mon 03/07/06
23	CPCC Software	Mon 17/11/08
24	Correlator Backend Software (V1.0 Test, V2.0)	Thu 30/11/06
25	CMIB Production Software	Mon 21/05/07

** This schedule is the current estimated view of the project with a compressed Stage 2/3 PCB build scenario.
** Long Term Schedule Modifications (from previous edition - 30Aug2007):
----- *Schedule formatted to only display incomplete tasks.*
----- Task 3: Stage 2 Prototype Redesign, Fabrication, & Assembly (2 PCB) has had it's name changed to reflect current build scenario and it's duration extended by 6 weeks.
----- *Task 6: Stage 2 Prototype Fabrication Acceptance Testing has had it's name changed to reflect current build scenario and it's duration extended by 2 weeks.*
----- Task 7: Stage 2 Accepted; Go-ahead Stage 3 (Fab & Assy - 8 PCB) has had it's name changed to reflect current build scenario and it's duration extended by 12 weeks (mostly due to addition of PCB Fabrication Go-ahead which occurs much sooner than Assembly Go-ahead, therefore the duration of the task is extended, but it starts much earlier).
----- *Task 12: High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site has had it's start date pushed out by 11 weeks to represent the current estimated delivery date.*
----- *Task 13: Racks Delivered to and Installed at VLA Site has had it's dependency on Task 12 (High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site) deleted.*
----- *Task 20: Prototype Software has been marked as complete.*
----- *Task 21: Test Build and Executor has been added to the schedule.*
----- *Task 23: CPCC Software has been set dependent on Task 21 (Test Builder and Executor).*



Comparisons of Similar Schedules

Task	Aug 30 Compressed Schedule	Dec 09 Compressed Schedule	Fairly Optimistic Hardware Schedule
Stage 2 Prototype Redesign, Fabrication (16 PCBs) , & Assembly (2 PCBs)	28May2007 – 11Dec2007	Xxx – 08Feb2008	Xxx – 10Jan2008
Stage 2 Prototype Acceptance Testing	05Dec2007 – 05Feb2008	18Jan2008 – 07Apr2008	11Jan2008-20Jan2008
Stage 2 Boards Accepted, Assemble the remaining 14 StBs & BLBs	30Jan2008 – 21Feb2008	02Feb2008 – 15May2008	13Mar2008 – 13Apr2008
HW/SW Integration Testing @ DRAO	22Feb2008 – 19Jun2008	20May2008 – 15Sep2008	18Apr2008 – 08Aug2008
WIDAR Correlator Critical Design Review	19Jun2008	15Sep2008	10Oct2008
HW (the PTC) for OTS Testing to VLA	20Jun2008 – 17Jul2008	16Sep2008 – 13Oct2008	08Aug – 15Aug2008
On-The-Sky (OTS) Critical Tests of the EVLA PTC	18Jul2008 – 30Oct2008	14Oct2008 – xxx	15Aug2008 – xxx

Schedule Speed-up Measures

- Parts Acquisition
  - Always has been well under control.
  - Now weekly procurement meetings.
    - Double checking exercise: Has schedule been recovered?
  - Buy long lead-time components in advance.
    - Note: BreconRidge sources most electronic components.
    - Major components already purchased (all FPGA's and delay RAM by end of Feb.)
- Skip component and board tests:
  - No reliability screen of first 1200 chips.
  - No production screen of correlator chips.
  - No burn-in of populated boards.
    - Only quick factory-based functional test of boards.
  - No JTAG tests of early prototypes.
  - No full test of correlator racks before shipping.

Schedule Speed-up Measures (cont'd)

- Ship single-baseline correlator with minimal testing.
- Minimize or eliminate OTS tests.
- Expedite bare-board fabrication.
- Overtime provisions where necessary.
- Hiring additional assemblers at DRAO for rack and cable assembly.
  - Being done, but not on critical path anyway.
- Adopt H/W-only schedule – just enough S/W to show H/W operational.

Summary: Proto & Production Corr. Chip-Screening

- 20-year reliability requirement.
- Company qualifications are important in this case.
  - Carried out by a company with a demonstrable track record
  - Even to the point of demonstrations in court of law.
- Carry out industry recognized screening tests.
  - Widely used by the telecom industry for similar lifetimes.
  - Requires investment in testing equipment.
  - Verify reliability of process, package, die.
  - Actual details of tests are proprietary at this time.
  - Carry out destructive testing on a small sample of devices.
  - Root Cause Failure Analysis
  - Design production testing that finds infant-mortality cases, but does not affect lifetime.
- Carry out functional tests on production chips.
  - DRAO stand-alone pass-fail functional tester (10-15 sec).
- Elapsed Time for full production screen: 17 weeks.

Summary: Prototype & Production Board-Screening*

- All tests on 2nd (Beta) Prototype Boards.
- Tests marked (P) on production boards.

1. Functional Test (P)
2. Signal integrity examinations, voltage checks, at all sites.
3. Board temperatures (thermal image) (P).
4. ESS (incrementally for Beta Prototypes to examine effects on boards).
   a) Thermal shock; unpowered; 0-80C, 2 cycles. (P)
   b) Functional test repeat (P)
   c) Thermal shock lifetime test; 0-80C, 10 cycles.
   d) Functional test repeat
5. Powered high temperature test, 160 hr, T_j = 100C. (P)
6. Powered ΔT, 1 hour cycle, 0-50C, 160 hr. (P)

- * See TVP Document A25010N0006 (Carlson) for details.

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Immutable Schedule Dependencies

- Lab testing
  - Length of time not well known.
    - Note that 1st protos already well tested.
- Parts acquisition
  - Delivery almost never on time.
    - Only remedy is squeaky wheel.
- Correlator Chip Delivery
  - Feb 15 currently.
  - Seeing is believing; scan-tested chips are better.
  - Only part clearly on the critical path.

What Can Go Wrong?

- Unknowable time for system integration and testing in Penticton.
- Parts delivery – even small parts.
  - Weekly procurement meetings.
  - Suppliers never on time.
- Shipping delays or disasters.
- Schedule recovery efforts that make the schedule worse.
- Bugs in testing
  - Software and FPGA code
    - slows things down.
  - Hardware
    - Could require re-spin of boards.
- System-level Issues
  - Unexpected computer bottle-necks.
    - E.g. model delivery
  - Serious ground loop problem.
  - Air conditioning.
  - Hidden fault in an interface (e.g. FORM board, Ethernet connections).

Most Serious Risks

- Shipping losses or delays
  - Shock, water, misdirection, border agents.
- Revised Baseline Boards do not work.
  - Re-design; re-spin of boards.
- Correlator Chips poor quality.
  - Detected during testing.
    - Re-spin of chips.
  - Detected after mounting on boards.
    - Re-spin of baseline boards.
- Loss of employees.
  - Risk is now mostly retired.
- "Horseshoe Nail" problem.
  - Lack of small common item holds up production.
- Fabricator (BreconRidge) problems.
  - Bare-board sub-contractor as well.

Most Serious Risks (cont'd)

- Funds do not come through for FY08/09; 90/10.
- Chip Fabricator or Packager fails.

Correlator System Testing Summary

- Stage 1/2: Prototyping and testing.
- Stage 3 Prototype testing
  - 16SB/16BB in racks will form “testable unit sub-systems”, loaded in a way that is very similar to final rack configuration.
  - Subjected to as many tests as possible in lab environment.
  - When complete, the OTS system will be shipped to Socorro.
- On-the-Sky (OTS) – 10-antenna.
  - Principal DRAO purpose is to verify hardware in-system.
  - Check for HST-style bloopers.
  - Long integration times available.
    - Already done for correlator chips.
- Production Testing
  - Both correlator chips and finished circuit boards will be subjected to temperature cycling and subsequent testing/burn-in before leaving DRAO.
  - Methodology is worked out, but precise details are not.
  - Testing hardware and equipment has been purchased or developed.

Software Required Near Term

- CMIB
  - All MAH's (Penticton Tests = PT)
  - Start/Stop Test function on CMIB that synchronizes MAH's. (PT)
  - Model generation, reading, and delay-vector generator. (On-the-sky Tests = OTS)
  - Board startup and BIST. (PT)
- FORM board firmware and MIB S/W.
  - SB-FORM interface firmware (PT)
  - MIB control. (OTS)
- Test Executor and all GUI's.
  - Needed for set of 14 boards. (PT)
  - Planned to be ready by end of March/08.
- RTDD (display software).
  - Needed mainly for Station Board. (PT)
  - Some testing has already been done in Penticton.
    - Bugs to be fixed (see JIRA).
- Intelligent diff. (PT)

On-the-Sky Testing

- Primary purpose – DRAO led (Critical OTS Tests).
  - Verify Hardware so that production phase can proceed.
  - Long integration times available.
  - Check for HST-style bloopers.
- Secondary Purpose – NRAO led.
  - Integration of a “small” system with EVLA software.
  - Testing of such, and further checks of software through-put.
- Tertiary Purpose – NRAO led.
  - Test wide-band observing.
  - Develop wide-band calibration techniques.
- Quaternary Purpose – NRAO led.
  - Look at wide-band RFI environment.
  - Develop evasion/expurgation measures.
- Quinary Purpose – NRAO led.
  - Carry out early observations where possible.

Critical OTS Tests

- Nature of decision
  - ***Is the fault that you just detected possibly attributable to the H/W and not FW or SW?***
  - Most testing will have been done in Penticton.
  - Most bugs will not be the correlator.
  - But … if there is a correlator bug, it will be exist forever.
  - Answer is real-time monitoring of the OTS tests.
- Michael/Brent's list (4 months?)
  - Basic setup/connectivity checks
  - Delay tracking
  - Noise switching
  - First fringes
  - Strong source, known flux density (check corr'n coeff)
  - Deep integration on mostly blank field (corr offsets and other systematics)
  - Deep spectral line integration (bandpass stability)
  - Recirculation on narrow line(s)
  - Sub-band stitching (comes "for free")

Michael R's Questions

- How realistic is the schedule?
- When do we know whether we are on the compressed or expanded schedule?
  - Can we add a decision date to the schedule?
- Are there other "gotchas" waiting to happen?
- Should we relax testing to speed up delivery?
  - If so, does this affect the number of spares required?
- Are there other ways to speed up delivery?
- What is the impact on Software Requirements.

End