NRC · CNRC

Expanded Very Large Array

Baseline Board and Chips

B. Carlson

NRC · CNRC

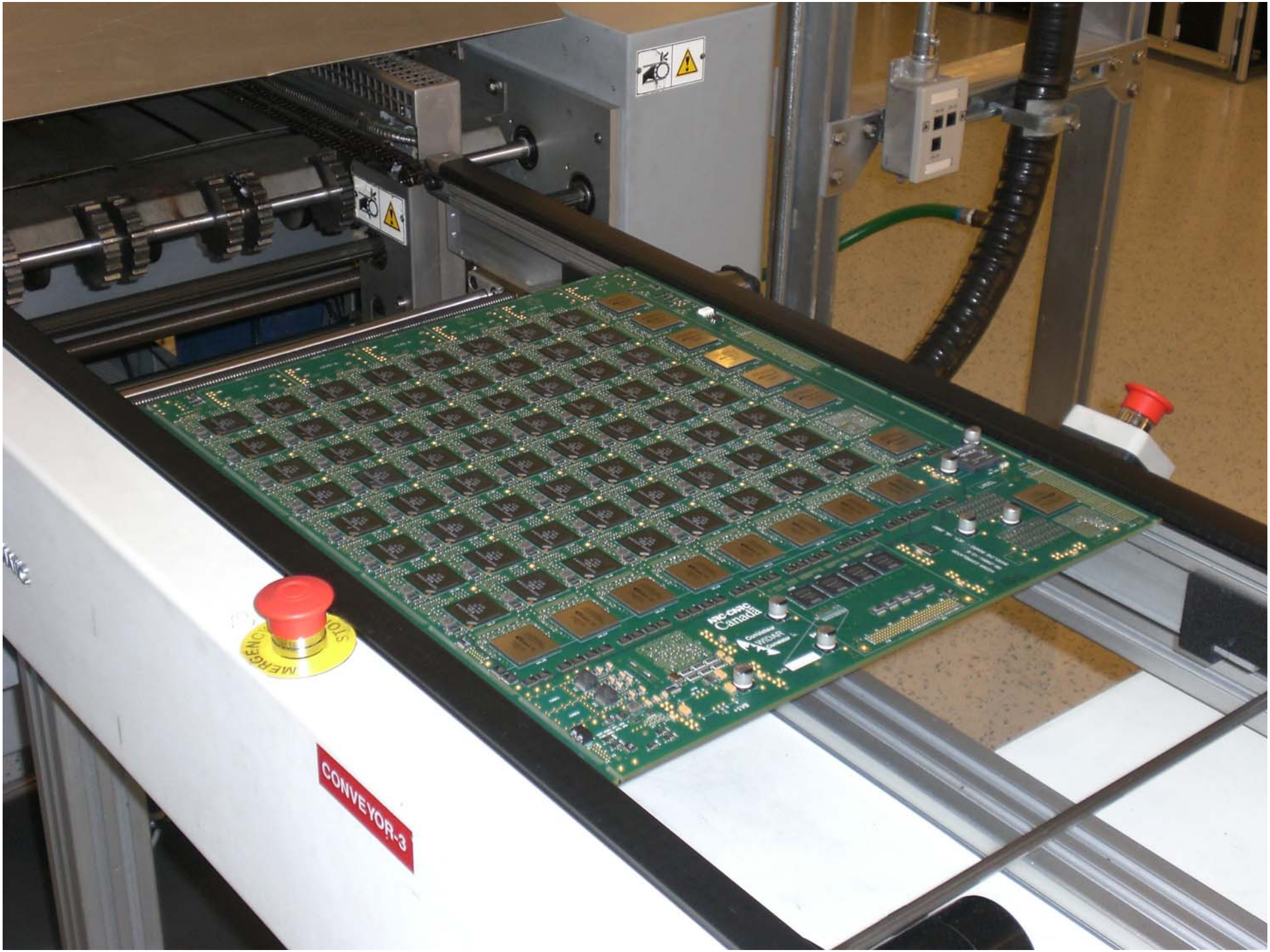
Outline

- Design status and schedule.
- Production status and schedule.
- Testing status and schedule.
- Delivery schedule to VLA/eMERLIN.
- Outstanding issues/risks.

NRC · CNRC

Design status and schedule

- Board:
  - PCB fab first 2 done…some problems.
  - SMT done (1st board). SMT 2nd board, ~week Dec. 12.
  - Expect delivery of 1 board ~Jan 7/08 if all tests (X-ray, FP, JTAG) pass…only partial "quickie" JTAG test.
  - This is the first fully corr-chip loaded board test with input section changes for new connectivity scheme.
  - Next board towards end Jan, need to do full JTAG test/dev (21 days).
  - Schedule for test and construction of next 14:
    - Most aggressive: available mid/late March in Penticton.
    - Otherwise, mid-April if no delays or major problems found.
    - Otherwise….?


CONVEYOR-3

NRC · CNRC

Design status and schedule

- BB chips:
  - **RXP FPGA**: Input section, on-chip testvectors (test mode) DDR in/out, X-bar, output section…RTL implemented and tested, working on gate-level sim to verify DDR I/O timing. Uses ~40% of chip.
    - Phasing logic: full reg description in RFS…start implementation after X-bar Board FPGA…probably ready for OTS testing in late summer/fall.
  - **Recirc FPGA**: All changes for external/internal recirc finished and tested. Have not tested 7-bit mode with recirc in H/W yet.
  - **Corr chip**: Passed CDR…validation testing complete. Production chip delivery expected Feb. 15/08. First 1200 chips func test in Penticton for 14-brd assy. Rest of chips undergo qual testing/screening, ready Aug/08.

NRC · CNRC

Design status and schedule

- BB chips:
  - **LTA FPGA**: design changes to support 2X RAM, and 1C12 device, finished, tested (RTL and gate-level). Ready for H/W testing.
  - **GigE FPGA**: Only pinout changes to support new board and lines from RXP chip. Still need to implement Phased-data synchronizer/packetizer. Will be a few registers added (sync detect, dest. MAC/IP etc.). Want to test with SFP with no autoneg…tried it but the GigE FPGA is transmitting BREAKLINKs(why??)
    - How much testing to do on 10 GigE option? Have XFP and receiver card…need minimum FPGA code to test link…at least look at S.I.

NRC · CNRC

Production status and schedule

- Most aggressive/optimistic: start full production Aug. 08, finish end 08.
- Next most aggressive/optimistic: start full production November 08, finish Feb. 09.
- Full testing (protos/prod) Penticton: start full production November 08, finish Jun 09.

IT ALL DEPENDS ON AMOUNT/SUCCESS OF TESTING.

NRC · CNRC

Testing status and schedule

- Start 1st board test ~Jan. 7/08.
- Scenarios:
  - 1 week test, if successful, give go-ahead for next 14…but have to wait for corr chips anyway.
  - 2 week test, if successful, give go-ahead for PCB fab of next 14, mid-Mar/08, go-ahead for assembly…get boards ~mid April…start sys integration and test in Penticton…finish mid-Aug/08…OTS start.

IT ALL DEPENDS ON AMOUNT/SUCCESS OF TESTING.

NRC · CNRC

Delivery schedule to VLA/eM

- Most aggressive: earliest single-baseline H/W: 3rd week Jan/08, if functional tests pass, no rel testing. Full OTS starts mid-March (eM).

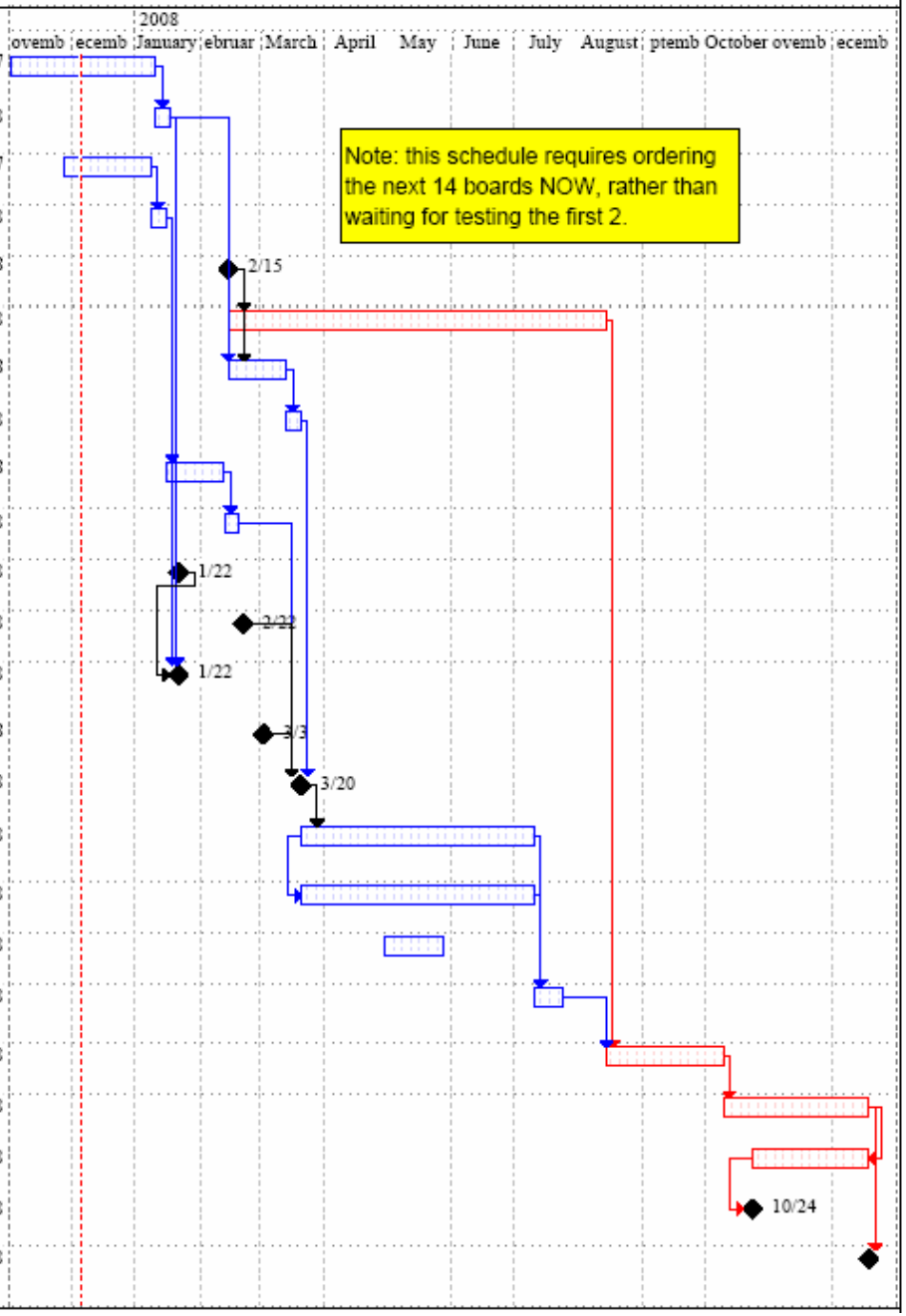
- Next most-agr: could deliver single-baseline H/W mid-March. Full OTS mid August (eM).

- Full production H/W: end 08, Feb/09, or Jun/09.

IT ALL DEPENDS ON AMOUNT/SUCCESS OF TESTING.

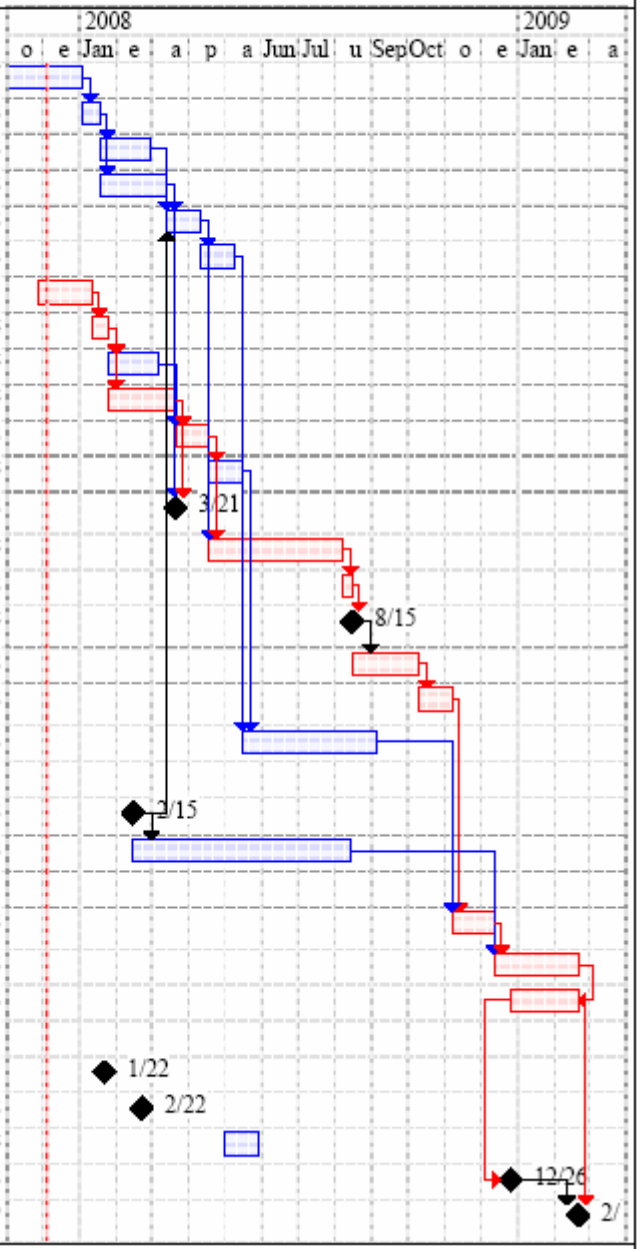
PRELIMINARY--FOR DISCUSSION ONLY: Expedited proto (no rel test); expedited production (no burn-in), H/W driven BEST CASE schedule

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, no JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton	Fri 1/11/08
3	Stage 2 Station Boards; qty=2; proto fabrication, no JTAG test	Wed 11/28/07
4	Stage 2 Station Boards; qty=2; functional test @ Penticton	Wed 1/9/08
5	1200 corr chips available at mfg (iSine delivery milestone)	Fri 2/15/08
6	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
7	Stage 3 Baseline Boards; qty=14; fabrication	Fri 2/15/08
8	Stage 3 Baseline Boards; qty=14; functional test @ Penticton	Fri 3/14/08
9	Stage 3 Station Boards; qty=14; fabrication	Wed 1/16/08
10	Stage 3 Station Boards; qty=14; functional test @ Penticton	Wed 2/13/08
11	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
12	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
13	**Single Baseline Tests Start: first H/W (2xSB + 1xBB) arrives a**	Tue 1/22/08
14	Next set of racks (2 SRs, 2 BRs, min) arrive at VLA	Mon 3/3/08
15	**8 more SBs, 10 BBs arrive at VLA; start full OTS testing**	Thu 3/20/08
16	**OTS testing at VLA (duration???)**	Fri 3/21/08
17	Functional test development; JTAG; full production tooling, long lead-time ordering	Fri 3/21/08
18	Final racks delivered and installed at VLA	Wed 4/30/08
19	**Critical Design Review (CDR)**	Fri 7/11/08
20	Full production: PCB fab	Fri 8/15/08
21	Full production: assy+test	Fri 10/10/08
22	Functionally tested boards delivered to VLA	Fri 10/24/08
23	Control Rack, CPUs, CBE etc install complete	Fri 10/24/08
24	**All H/W delivery to VLA complete**	Thu 12/18/08



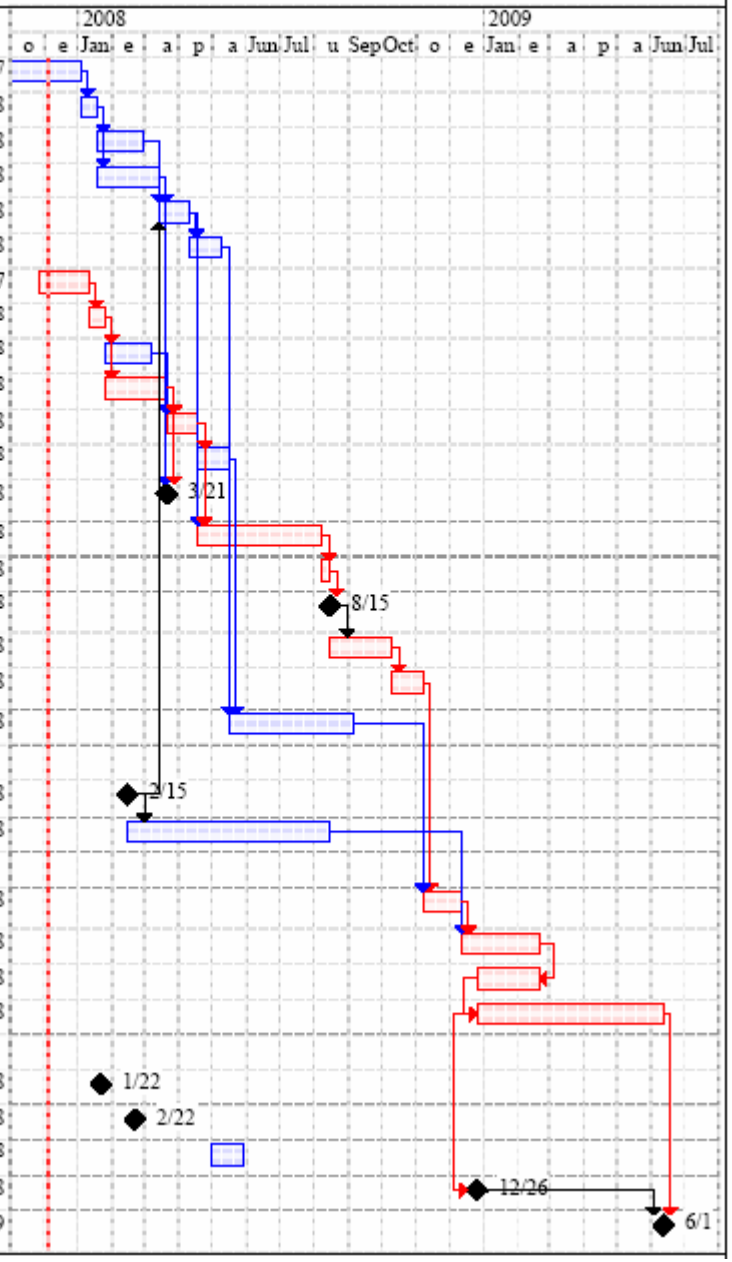
PRELIMINARY--FOR DISCUSSION ONLY: Full prototype reliability test and laboratory sys integration; expedited production (no burn-in), BEST CASE schedule; Expedited St. Brd and Bas. Brd. delivery. No rel testing on first 1200 corr chips.

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, c/w JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/4/08
3	Stage 3 Baseline Board; qty=14 PCB fab, 6 week turn	Fri 1/18/08
4	Stage 2 Baseline Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/18/08
5	Stage 3 Baseline Board; qty=14; assembly	Fri 3/14/08
6	Stage 3 Baseline Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/11/08
7	Stage 2 Station Boards; qty=2; proto fabrication	Wed 11/28/07
8	Stage 2 Station Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/11/08
9	Stage 3 Station Board; qty=14 PCB fab, 6 week turn	Fri 1/25/08
10	Stage 2 Station Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/25/08
11	Stage 3 Station Board; qty=14; assembly	Fri 3/21/08
12	Stage 3 Station Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/18/08
13	**Single baseline H/W could be sent to VLA to begin early OTS testing**	Fri 3/21/08
14	System integration and test @ Penticton (duration????)	Fri 4/18/08
15	10 Station Boards, 12 Baseline Boards ship to VLA	Fri 8/8/08
16	**Begin full OTS testing; 10 stations, 1536 MHz/poln, at VLA**	Fri 8/15/08
17	Critical OTS testing for production go-ahead (duration???)	Fri 8/15/08
18	**Critical Design Review**	Fri 10/10/08
19	Production tooling: functional test setup, order long-lead time parts	Fri 5/16/08
20		
21	**Production corr chips delivered from iSine (how firm???)**	Fri 2/15/08
22	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
23		
24	**Start full production: Production PCB fab, all PCBs, 6 week turn**	Fri 11/7/08
25	Full production and functional test	Fri 12/12/08
26	Functionally tested H/W boards delivered to VLA site	Fri 12/26/08
27		
28	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
29	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
30	Final racks delivered and installed at VLA	Thu 5/1/08
31	Control Rack, CPUs, CBE etc install complete	Fri 12/26/08
32	**All H/W delivery to VLA complete**	Fri 2/20/09



PRELIMINARY--FOR DISCUSSION ONLY: Full prototype reliability test and laboratory sys integration; production burn-in in Penticton, BEST CASE schedule; Expedited St. Brd and Bas. Brd. delivery. No rel testing on first 1200 corr chips.

ID	Task Name	Start
1	Stage 2 Baseline Boards; qty=2; proto fabrication, c/w JTAG test	Fri 11/2/07
2	Stage 2 Baseline Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/4/08
3	Stage 3 Baseline Board; qty=14 PCB fab, 6 week turn	Fri 1/18/08
4	Stage 2 Baseline Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/18/08
5	Stage 3 Baseline Board; qty=14; assembly	Fri 3/14/08
6	Stage 3 Baseline Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/11/08
7	Stage 2 Station Boards; qty=2; proto fabrication	Wed 11/28/07
8	Stage 2 Station Board; qty=2; functional test @ Penticton; pre-qual for Stage 3 PCB fab	Fri 1/11/08
9	Stage 3 Station Board; qty=14 PCB fab, 6 week turn	Fri 1/25/08
10	Stage 2 Station Board; qty=2; full reliability/functionality testing (duration???)	Fri 1/25/08
11	Stage 3 Station Board; qty=14; assembly	Fri 3/21/08
12	Stage 3 Station Board; qty=14; full reliability/functionality testing (duration???)	Fri 4/18/08
13	**Single baseline H/W could be sent to VLA to begin early OTS testing**	Fri 3/21/08
14	System integration and test @ Penticton (duration????)	Fri 4/18/08
15	10 Station Boards, 12 Baseline Boards ship to VLA	Fri 8/8/08
16	**Begin full OTS testing; 10 stations, 1536 MHz/poln, at VLA**	Fri 8/15/08
17	Critical OTS testing for production go-ahead (duration???)	Fri 8/15/08
18	**Critical Design Review**	Fri 10/10/08
19	Production tooling: functional test setup, order long-lead time parts	Fri 5/16/08
20		
21	**Production corr chips delivered from iSine (how firm???)**	Fri 2/15/08
22	Production corr chip qualification and screen testing (need to verify duration)	Fri 2/15/08
23		
24	**Start full production: Production PCB fab, all PCBs, 6 week turn**	Fri 11/7/08
25	Full production, JTAG, partial assembly at BMS	Fri 12/12/08
26	Production boards ship to Penticton.	Fri 12/26/08
27	Burn-in test H/W boards and deliver to VLA site (average of 2 large boards per day--faster???)	Fri 12/26/08
28		
29	First Station rack arrives at VLA (for single baseline test)	Tue 1/22/08
30	128 sets of rack-to-rack cables arrive at VLA	Fri 2/22/08
31	Final racks delivered and installed at VLA	Thu 5/1/08
32	Control Rack, CPUs, CBE etc install complete	Fri 12/26/08
33	**All H/W delivery to VLA complete**	Fri 6/12/09



NRC · CNRC

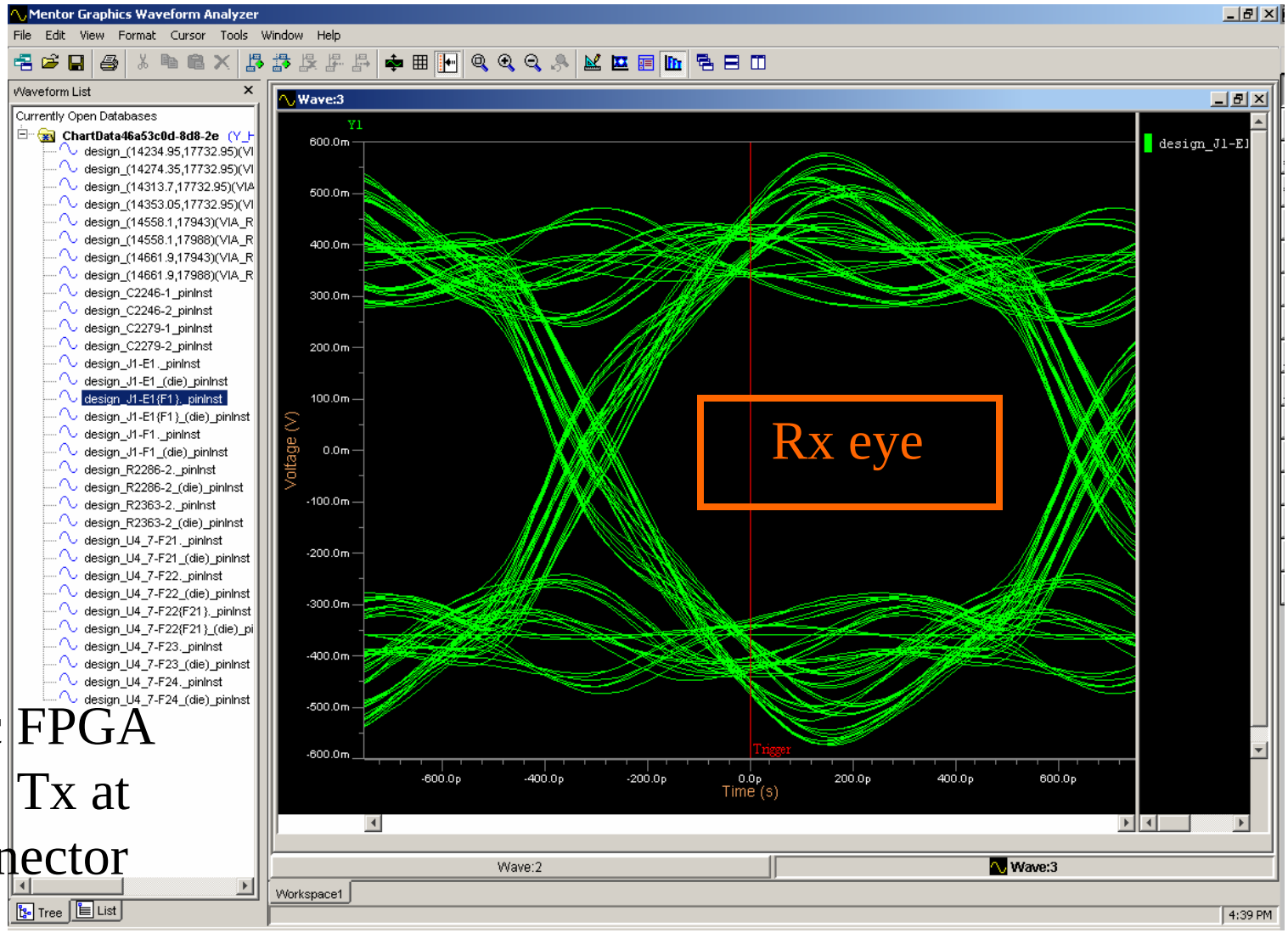
Outstanding H/W issues

- RXP phasing logic implementation/test.
- Debugging/testing (some FPGA bugs for current proto need to be chased down). Probe testing all chip sites for S.I. checks.
- Settling on rel testing procedure…requires incremental test and verify with the 14.
- Thermal heat-spreader plate for back of board? Effectiveness of thermal interface material?
- TESTING. TESTING. TESTING. H/W--S/W integration/debugging.
- Final assy/test in Penticton or at BMS?

NRC · CNRC

Risks

- RXP FPGA can't handle all of the 1 Gbps I/O; RXP-RXP DDR
  - Low; spoken to Altera; no firm reason to believe this will be a problem, but never tested a chip with this many 1 Gbps I/O before.
- Y Recirc output to next board X input.
  - Plan to use "Patch Board" PCB rather than cable. Hypertransport rather than LVDS (higher amplitude).
  - Use high-performance PCB material (IS415: Dk=3.7; LC=0.013). Will run multi-board sim tests before build to verify.
  - Y Recirc Tx/Rx connection for I/O capability (expansion)…additional source jitter. Can remove connection if necessary…surface traces. Re-spin PCB with 0201 connections.
  - Could use cable if necessary for performance…more $, less intrinsic reliability.
- First time that entire corr chip matrix populated…
  - All sites are carbon-copies of tested sites on first board.
  - Risk is considered low, but unknown until tested.



Recirc FPGA LVDS Tx at Y connector

NRC · CNRC

Summary

- Design status and schedule.
- Production status and schedule.
- Testing status and schedule.
- Delivery schedule to VLA/eMERLIN.
- Outstanding issues.