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Expanded Very Large Array

# OTS Testing of Prototype Correlator

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# Outline

- Overview.
- Test plan
- S/W requirements.

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# Overview

- The H/W and prototype test S/W will have been checked out to a high degree of confidence before this test.

- The primary goal of this test (from our perspective) is to provide the final assurance that the H/W "works" before committing to further full production.
  - Although, Corr Chip production must proceed before this test.

- Test plan A25010N0005 – 34 prioritized tests + 10 astronomer-determined tests.

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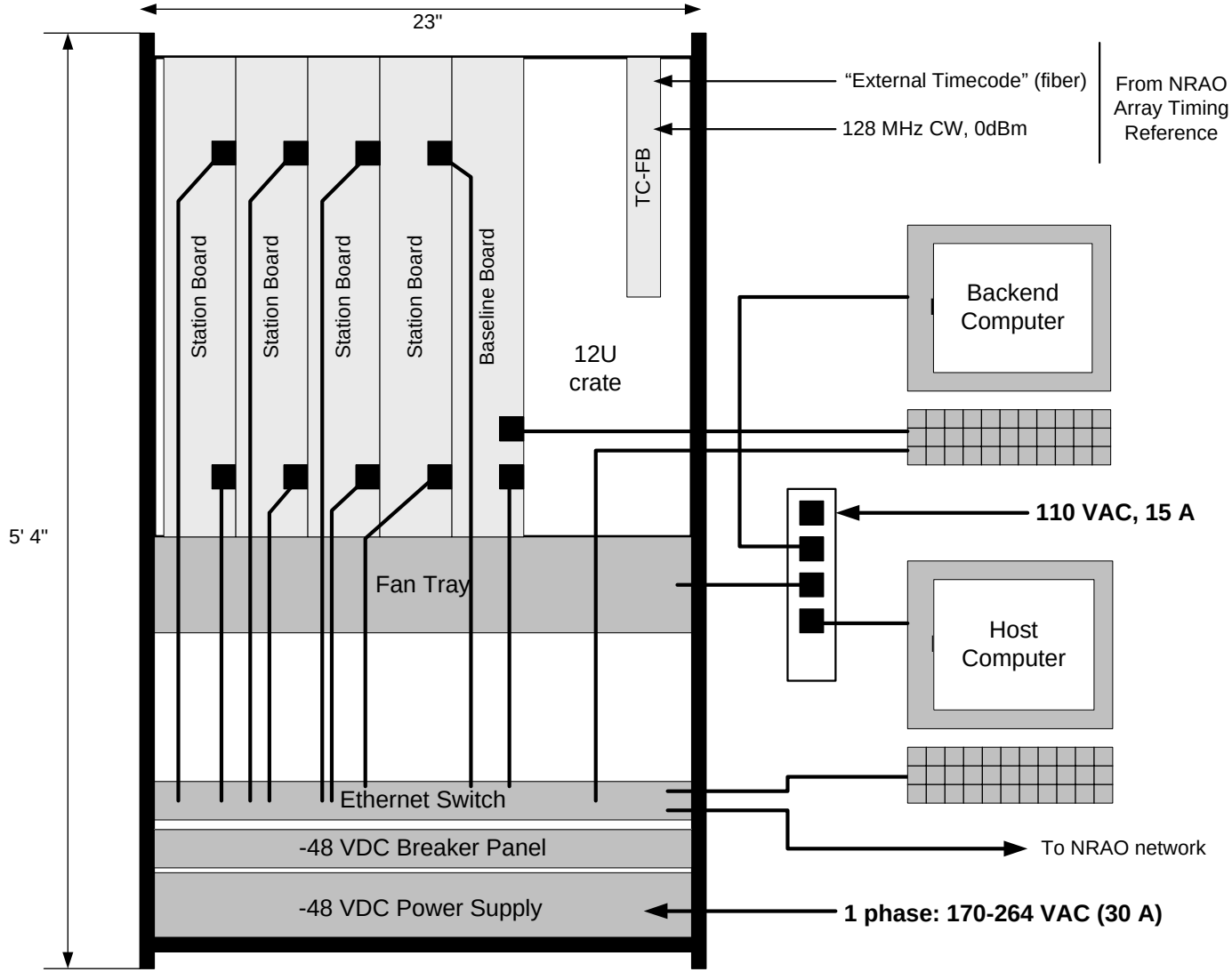
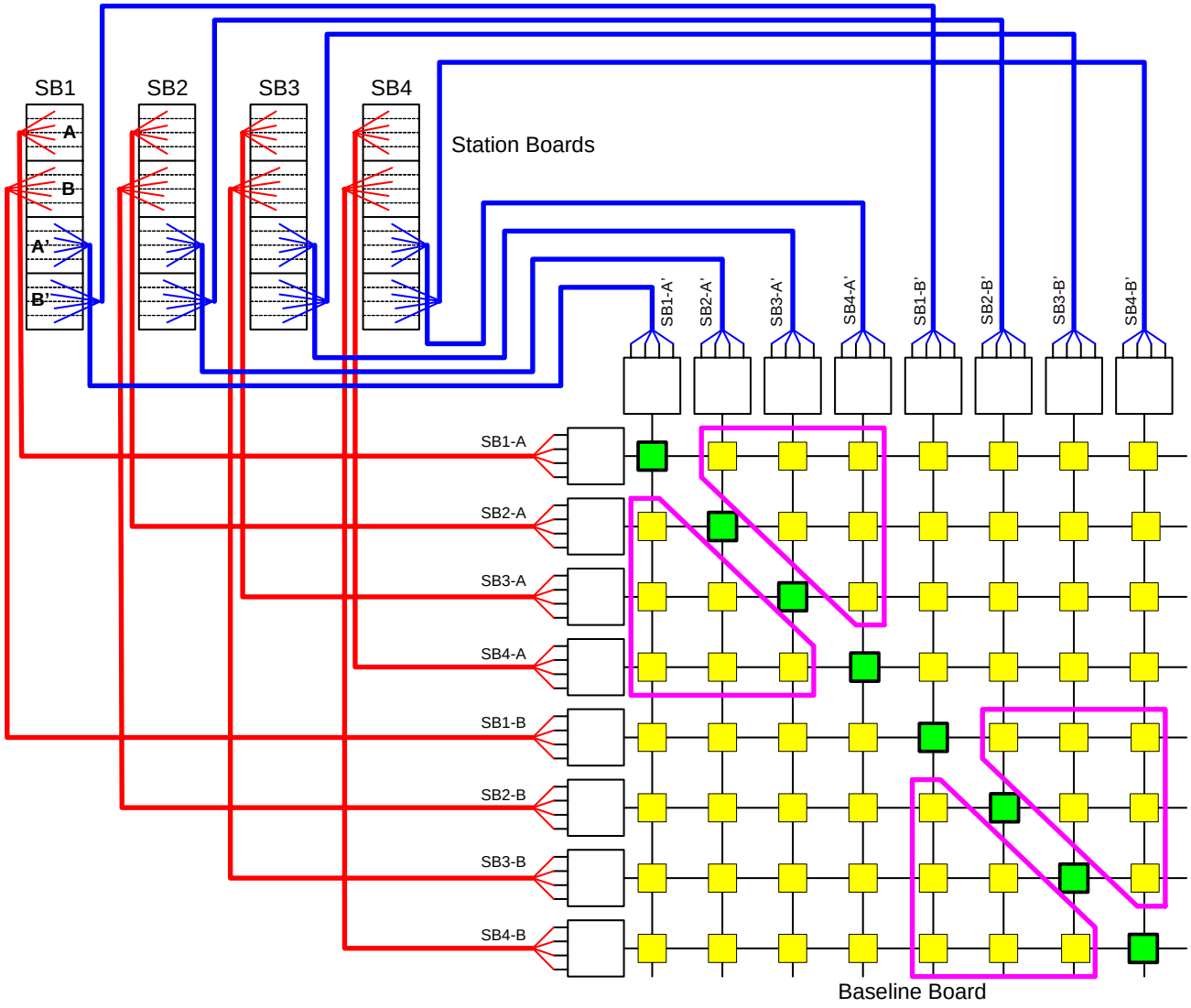
# Test Plan

- 4 Station Boards.
- 1 Baseline Board.
- 1 FB-TC.
- Computers for GUIs and CBE.


23"
5' 4"
"External Timecode" (fiber)
128 MHz CW, 0dBm
From NRAO Array Timing Reference
TC-FB
Station Board
Station Board
Station Board
Station Board
Baseline Board
12U crate
Backend Computer
110 VAC, 15 A
Fan Tray
Host Computer
Ethernet Switch
To NRAO network
-48 VDC Breaker Panel
-48 VDC Power Supply
1 phase: 170-264 VAC (30 A)


Canada


SB1
SB2
SB3
SB4
A
B
A'
B'
Station Boards
SB1-A'
SB2-A'
SB3-A'
SB4-A'
SB1-B'
SB2-B'
SB3-B'
SB4-B'
SB1-A
SB2-A
SB3-A
SB4-A
SB1-B
SB2-B
SB3-B
SB4-B
Baseline Board

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# S/W Requirements

- Outlined in OTS test plan A25010N0005 and in Sonja's A25204N0001.
  - Board and chip GUIs for configuration/status.
  - Top-level and rack-level GUIs to set configs and determine status.
  - Real-time wideband delay tracking…on SB CMIB, getting models from "Model Server".
  - Real-time phase model generation…calculated from delay models on the SB CMIB.
  - Real-time dump control…SB CMIB.
  - SB and CBE…save data products for analysis/image processing.
    - Phase and amplitude closure tests.
    - Continuum and spectral-line imaging/dynamic range tests.