

# Current state of hardware development/delivery

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## Outline

- Board status.
  - Baseline Board.
  - Station Board.
  - Fanout Board.
  - Etc.
  
- System-level design/purchasing.

## Board Status

- Baseline Board:
  - Mechanical sample received ~September 21<sup>st</sup>. Useful for physically checking mating with bits of metal and test bed.
  - Electrical prototype received October 24<sup>th</sup>. Testing starting...
  - Corr chip protos waiting since June...need basic first tests to pass before getting the rest of the 200 protos packaged.
  - Test vector generator FPGA+GUI (on old Timecode Board) ready to roll.

## Board Status

- Station Board
  - Mechanical and electrical boards should arrive ~end of 1<sup>st</sup> week November.
  - All FPGA design complete and gate-level simulated.
  - Heatsink and stiffener bar are ready and waiting.
- New Fanout Board
  - Should ship to us by mid-November.
  - Contains FPGA to re-time hi-speed signals to avoid destructive jitter accumulation.
  - Also used for “External Timecode” distribution for correlator, by installing optional fiber and SMA connectors.
  - Both the hi-speed fanout and timecode distribution FPGAs are built and gate-level simulated.

## Board Status

- New Common Backplane
  - Work order issued ~Oct. 18<sup>th</sup>.
  - Probably show up in mid Dec/Jan.
  - Still can use old one for test bed testing.
  
- Delay Module
  - Original designed board received...wait for Station Board to test.
  - New design (cheaper FPGA, DDR SDRAM) underway.
  - Probably here in ~March/April/07.

## Board Status

- PCMC
  - Current board “works”...no further prototyping anticipated...minor change for board-type ID...but still have to test ADC functions.
- RPMIB
  - Development after Correlator Chip test board.
  - Simple, low-speed; diodes, resistors, opto-couplers, wire terminals.
- Correlator Chip test board
  - PAR almost complete. FPGA design+test complete; c/w 30 test cases.
  - 5 will be made.
  - Probably Feb/March delivery
  - Required for production quantity testing of Correlator Chips.

## Board Status

- Correlator chip
  - Priority is to test the correlator chip (according to test plan), so we can give the go-ahead for production. Production qty ~12 weeks ARO, but if the past is any indication, it will likely take longer.
  - Successful test requires fully-loaded Baseline Board...for now we have only ~10 packaged chips...get the rest of the 200 chips packaged once tests indicate there are no packaging problems (I/Os work).

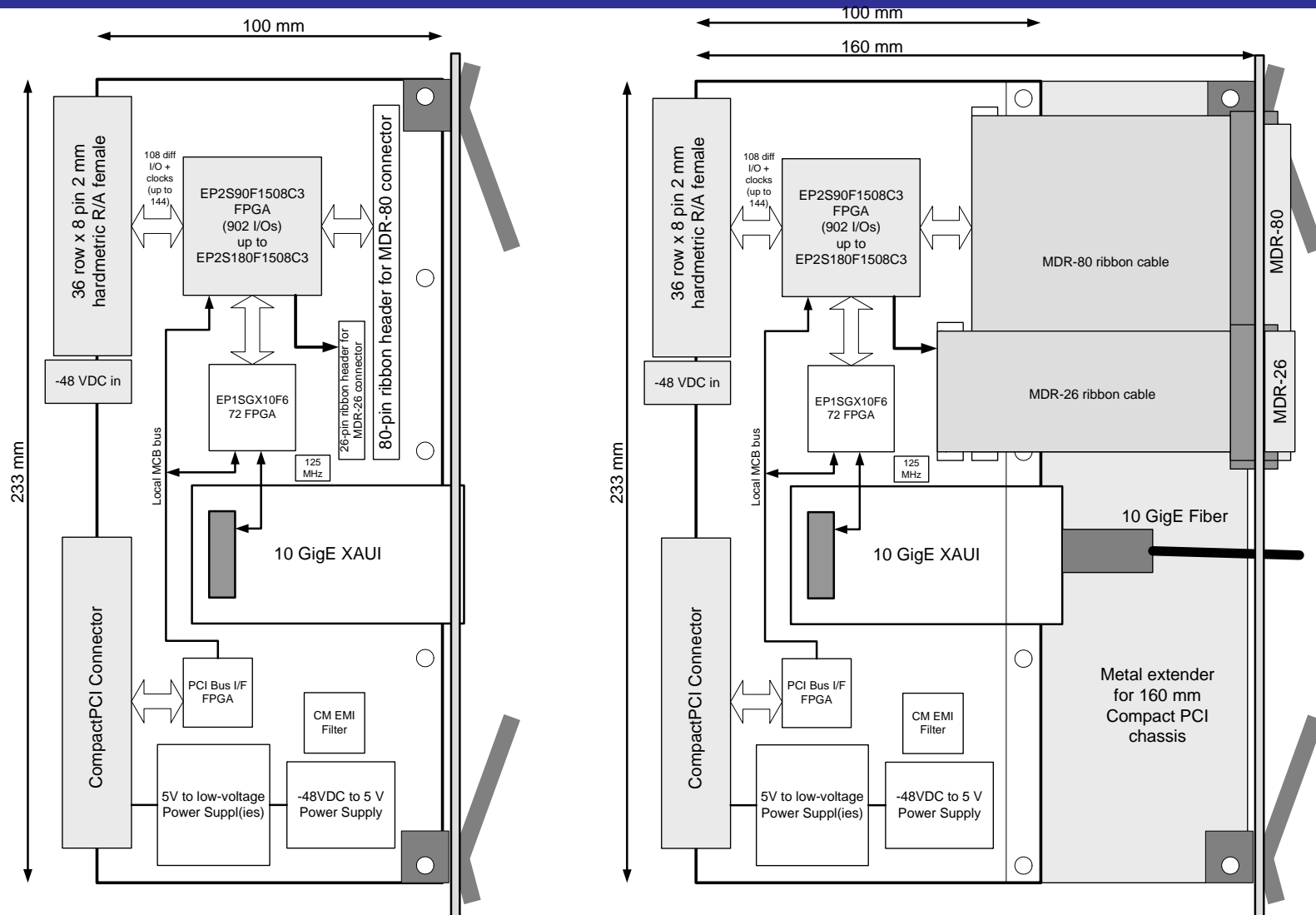
## Board Status

- Terminator Board
  - Required for incremental testing wherein not all Baseline Boards are installed in a rack (unterminated Fanout Board outputs feedback and “wreck” other signal channels).
  - Develop after RPMIB.
  - Small board with 36-row hm 2 mm connector and resistors...short development time.
  - Qty TBD (maybe ~20).



## Board Status

- Phasing Board
  - Still refining design concept...RFS review held Oct 18/06.
  - New RFS available...Jan/07? Depends on Baseline Board testing.
  - Good chunk of FPGA design required before starting board layout.
  - Probably start board layout mid 07...depending on Baseline Board testing.



## System-level design/purchasing

- -48 VDC power plant contract signed very soon. Probably delivered in Jan/07. (Currently held up on “federal employment equity requirements”).
- Meritec cable contract development underway...DRAFT Contract in Meritec’s hands. 12 weeks to prototype cables after contract signing.
  - All major DRAFT cabling installation plans released.
  - Still need to refine quantities or add quantities for Phasing Board.
  - Will order production quantity cables after successful end-to-end test...12 weeks ARO.

## System-level design/purchasing

- Rack mechanical and electrical specs doc V1.0 released.
- System BOM under development
  - Based on rack elec/mech specs doc and system network diagram.
  - Purchasing is combination of COTS RFP thru PWGSC, and purchasing out of DRAO.
- Sub-racks and rack cooling mechanics SolidWorks models and drawings undergoing final development.
  - RFP/PWGSC purchase required due to cost...evaluation and production stage.

## System-level design/purchasing

- Goal is to have all components in place for rack assembly by ~July 2007.
  - Racks.
  - Sub-racks.
  - Rack fan metal bits (duct, fan carrier, carriage assembly).
  - Common Backplanes.
  - High-speed Meritec cable + strain relief.
  - Wire, crimp terminals, screws, breaker panel, breakers, DIN rail, RPMIBs.
- Aim to complete assembly and test of racks by end of 2007.
  - Have lined-up at least one additional rack assembly person...may need another. Estimate 2 person weeks to assemble + test each rack.

## System-level design/purchasing

- Production inter-rack Meritec cable should be delivered to DRAO by July 2007 (requires successful end-to-end test).
  - We need to kit and label all cables before shipment to VLA in ~early fall of 2007.
  - Installation at VLA site requires NRAO personnel. NRC to provide engineering assistance if requested.



