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Expanded Very Large Array

EVLA Correlator Prototype and OTS Testing

B. Carlson

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Outline

- Initial prototype testing.
  - Test setups.
  - Test equipment.
- Prototype system testing.
- On-the-Sky (OTS) testing.
  - Review of DRAFT test plan.
- Schedule.

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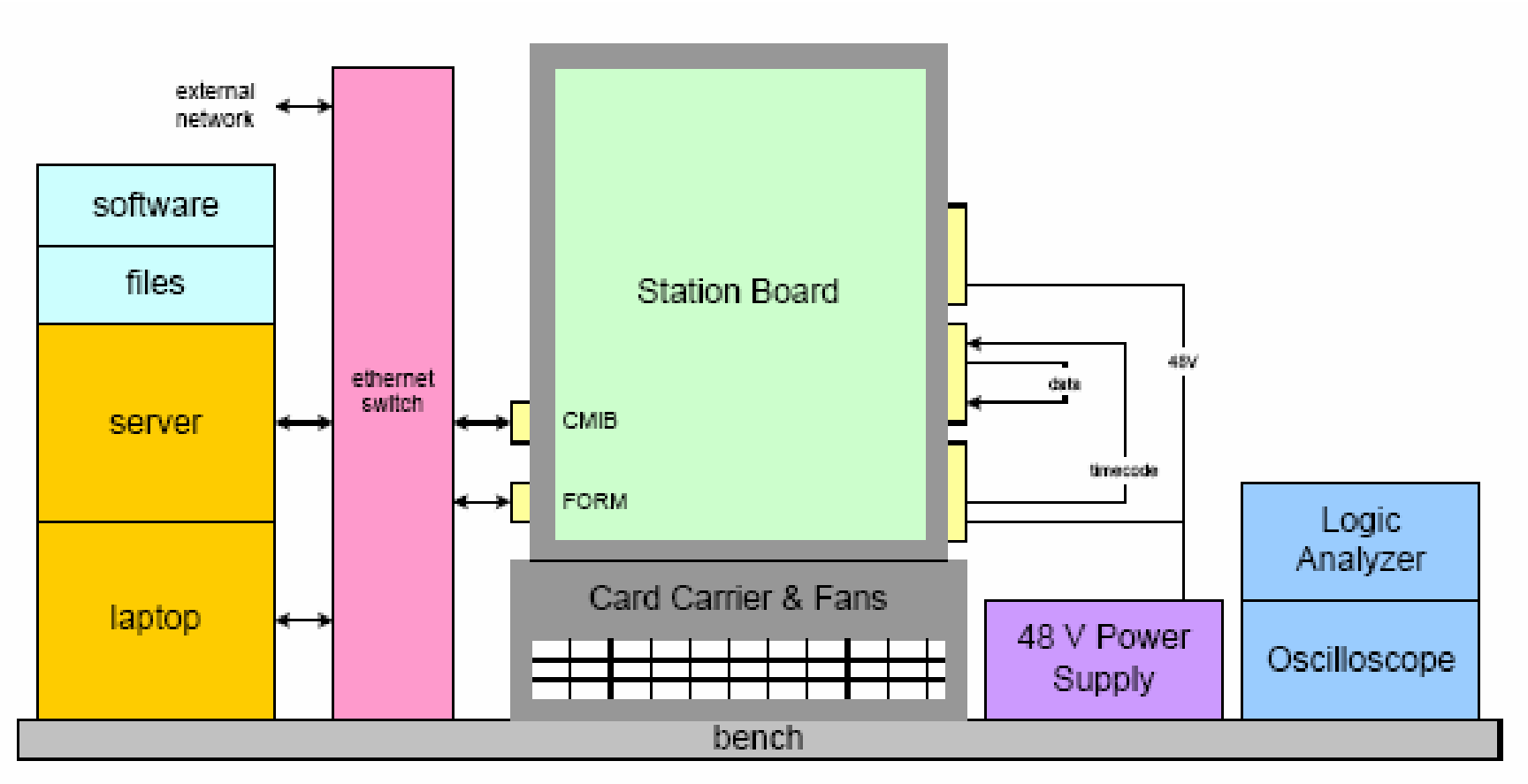
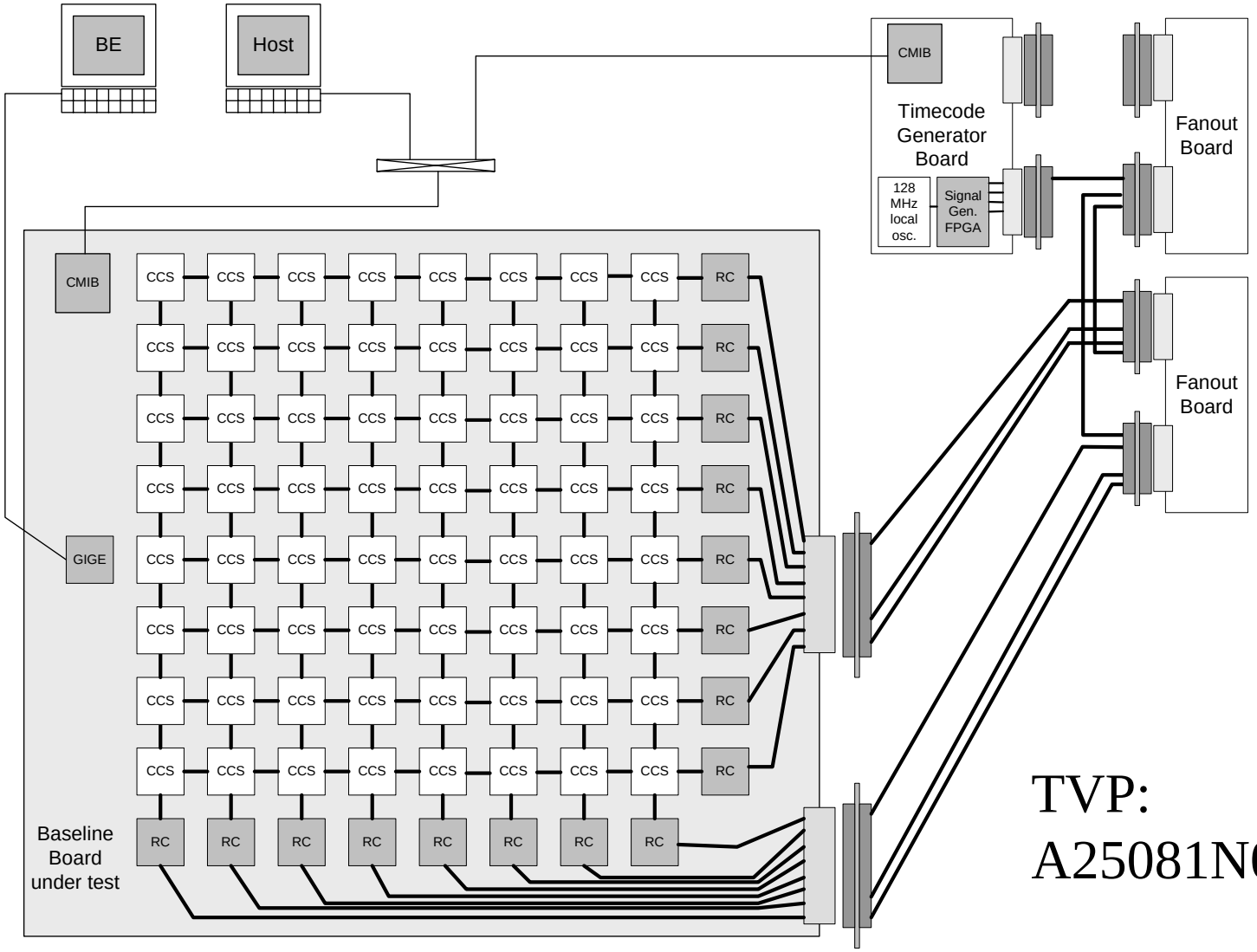
Initial Prototype Testing

- Station Board and Baseline Board tested separately.
- Station Board contains its own timing, test vector generators, and has loopback test capability for testing HM Gbps.
- Baseline Board stimulated with a Timecode Board.
  - TGB FPGA special design used to generate HM Gbps signals for testing.
  - Prototype Corr Chips socketed…all sites can be tested…some risk.
  - Formal qualification of Corr Chips before full ASIC production (hopefully in ’06).



TVP: A25040N0003



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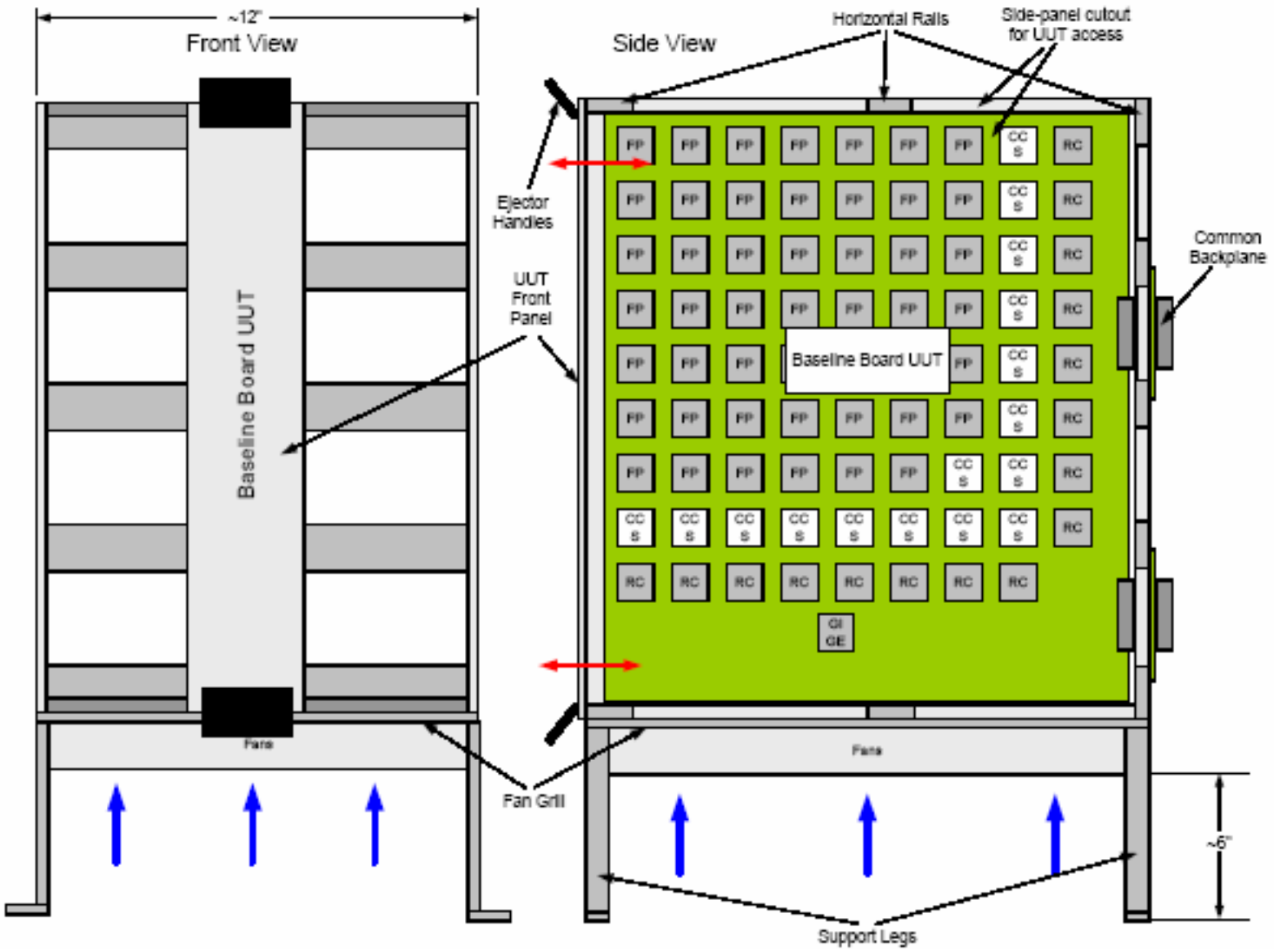
~12"
Front View
Baseline Board UUT
Fans
Side View
Horizontal Rails
Side-panel cutout for UUT access
Ejector Handles
UUT Front Panel
Common Backplane
Baseline Board UUT
Fans
Fan Grill
~6"
Support Legs

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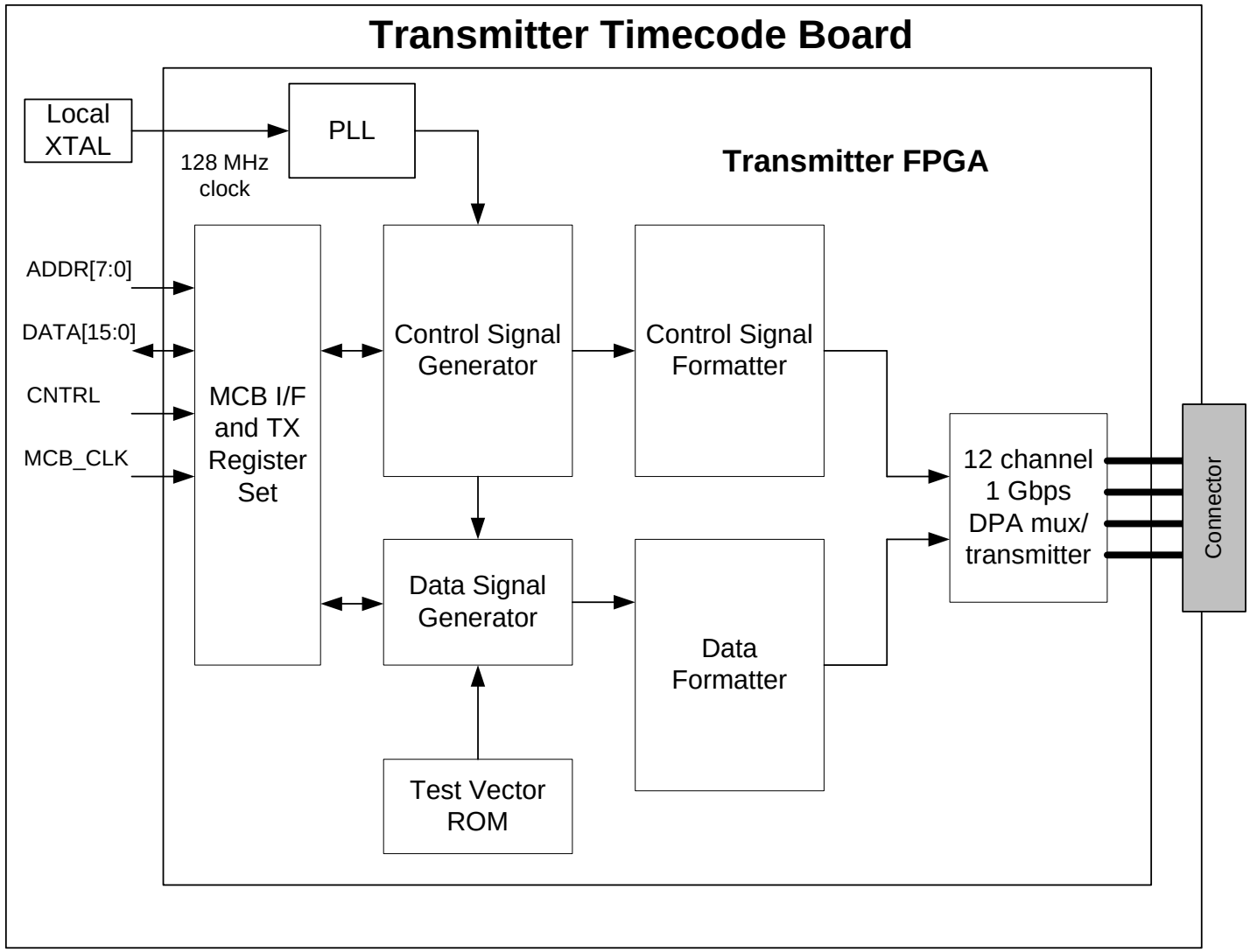
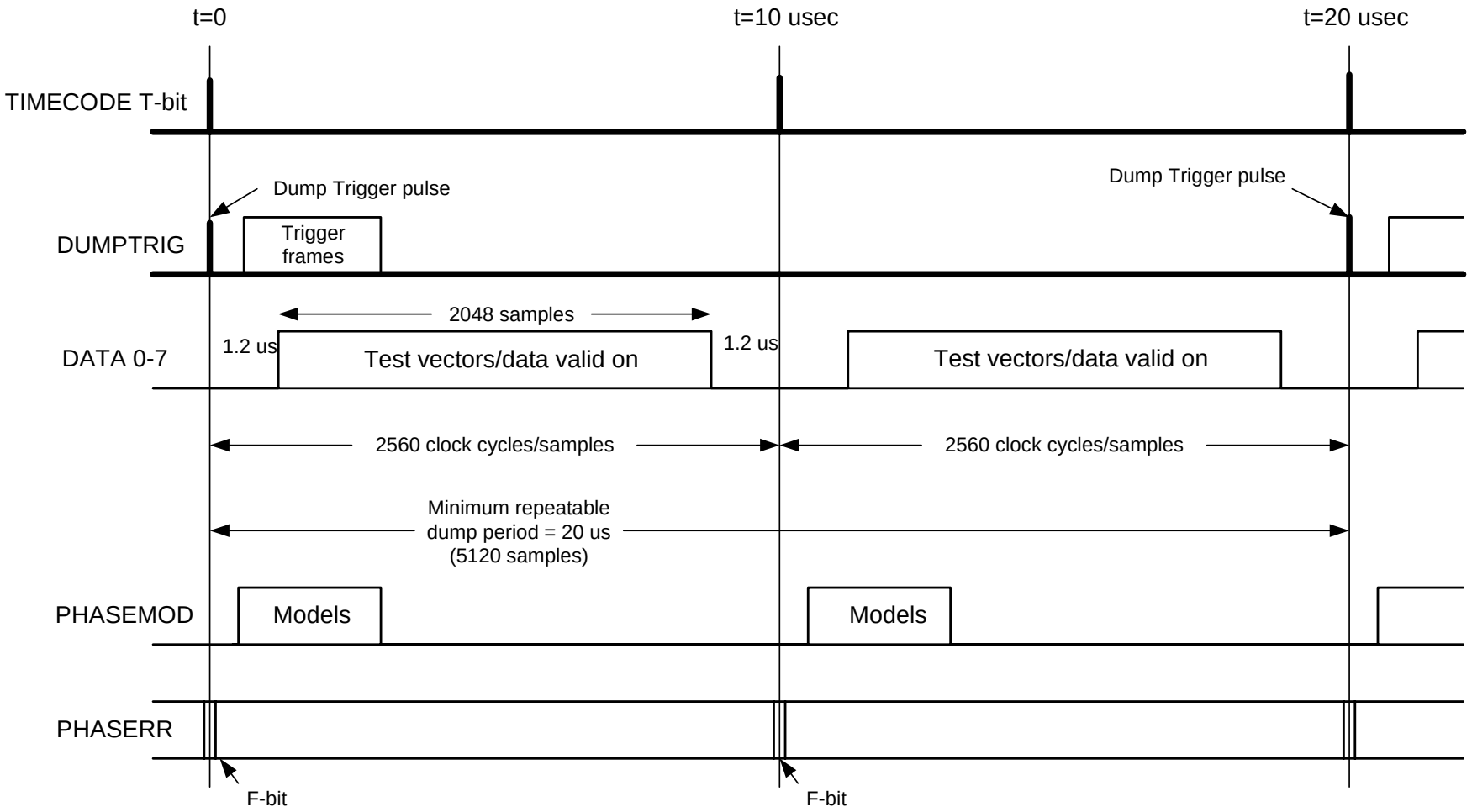
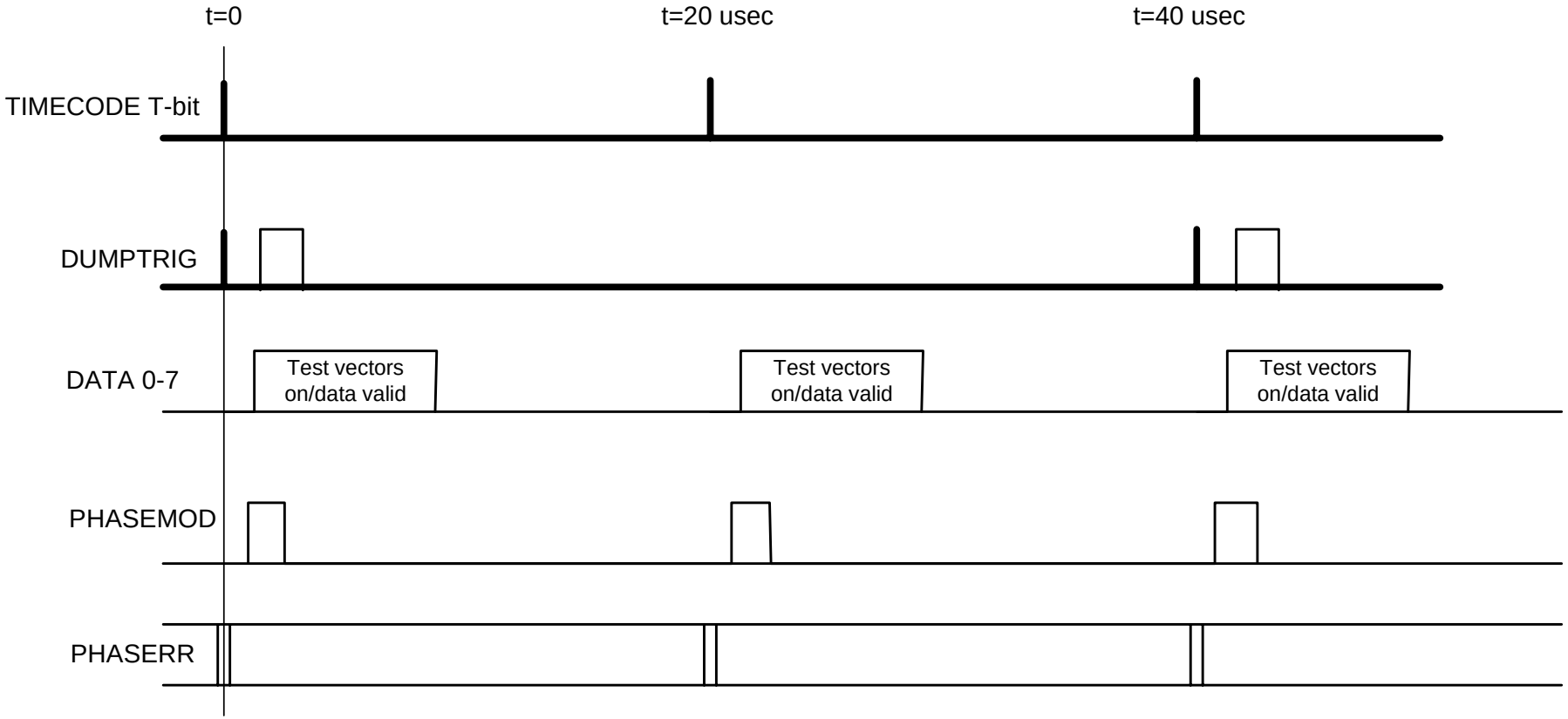
Baseline Board proto testing

- Description of test vectors, GUI panels, CBE requirements in appendix of Correlator Chip prototype verification matrix document A25082N0005 (in prep, no DRAFT release yet).


Transmitter Timecode Board
Local XTAL
PLL
128 MHz clock
Transmitter FPGA
ADDR[7:0]
DATA[15:0]
CNTRL
MCB_CLK
MCB I/F and TX Register Set
Control Signal Generator
Control Signal Formatter
Data Signal Generator
Data Formatter
Test Vector ROM
12 channel 1 Gbps DPA mux/ transmitter
Connector


t=0
t=10 usec
t=20 usec
TIMECODE T-bit
Dump Trigger pulse
Dump Trigger pulse
DUMPTRIG
Trigger frames
2048 samples
1.2 us
DATA 0-7
Test vectors/data valid on
1.2 us
Test vectors/data valid on
2560 clock cycles/samples
2560 clock cycles/samples
Minimum repeatable dump period = 20 us (5120 samples)
PHASEMOD
Models
Models
PHASERR
F-bit
F-bit


t=0
t=20 usec
t=40 usec
TIMECODE T-bit
DUMPTRIG
DATA 0-7
Test vectors on/data valid
Test vectors on/data valid
Test vectors on/data valid
PHASEMOD
PHASERR

Timing and Dump Control

☑ Enable TIMECODE

10 TIMECODE period (usec)

☑ DUMPTRIG Enable

☑ Sync Test Frame

☐ Speed dumps

☑ Normal dumps

DATA str	DUMPTRIG Period (usec)	Dump Modulo	LTA accum	Frames/s/ CCC/chip
DATA-0	20	4	100	500
DATA-1	40	8	200	125
DATA-2	60	12	300	56
DATA-3	80	16	400	31
DATA-4	100	20	500	20
DATA-5	120	24	600	14
DATA-6	140	28	700	10
DATA-7	160	32	800	8

Data Stream Control

256 Sample rate Ms/s

PHASEMOD Models SET

DATA Stream IDS ☑ hex ☐ decimal ☐ Hz, cycles

	SID	SBID	BBID	P0	P1
DATA-0	105	3	0	03026EFB	00259506
DATA-1	115	5	1	0D416D36	00A58873
DATA-2	125	7	2	05B36D8B	0047310D
DATA-3	135	9	3	1A060683	0144FA12
DATA-4	145	11	4	08646C1B	0068CD14
DATA-5	155	13	5	26CA9FCF	01E46BB2
DATA-6	165	15	6	0B156AAB	008A691B
DATA-7	175	17	7	338F391C	0283DD52

PHASERR_m (0,2,4,6) 64

PHASERR_n (1,3,5,7) 64

☑ Auto-calculate PHASEMOD coeffs

Re-Calculate PHASEMOD coeffs for current sample rate

CRC Error Generation

☐ TIMECODE
☑ DUMPTRIG
☐ PHASERR0_1
☐ PHASERR2_3
☐ PHASERR4_5
☐ PHASERR6_7
☐ PHASEMOD
☐ DATA-0
☐ DATA-1
☐ DATA-2
☐ DATA-3
☐ DATA-4
☐ DATA-5
☐ DATA-6
☐ DATA-7

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Baseline Board

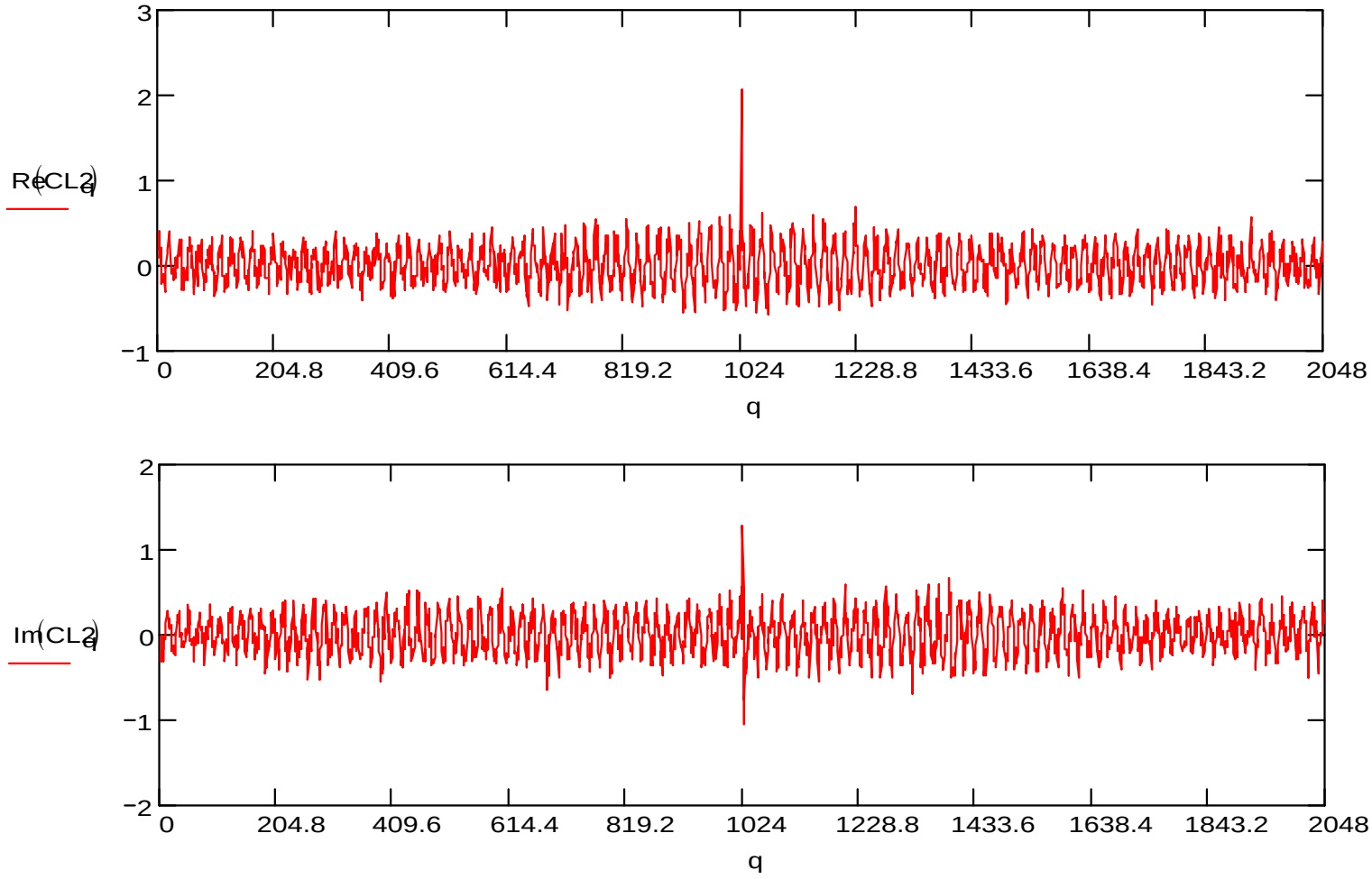
- Raw frames from CBE inspected for correctness.
- Plots from CBE…cross-correlation of vectors generated by TGB special FPGA (should) produce fringes.
- Vectors support bit-exact comparison of hardware via CBE's raw floating-point Re/Im lags with S/W reference correlator.
  - Don't need to use Corr Chip RTL simulation (slow).
  - Not quite bit-exact—within double-precision floating-point numerical error.
- Also, perform redundant correlations…compare with each other.

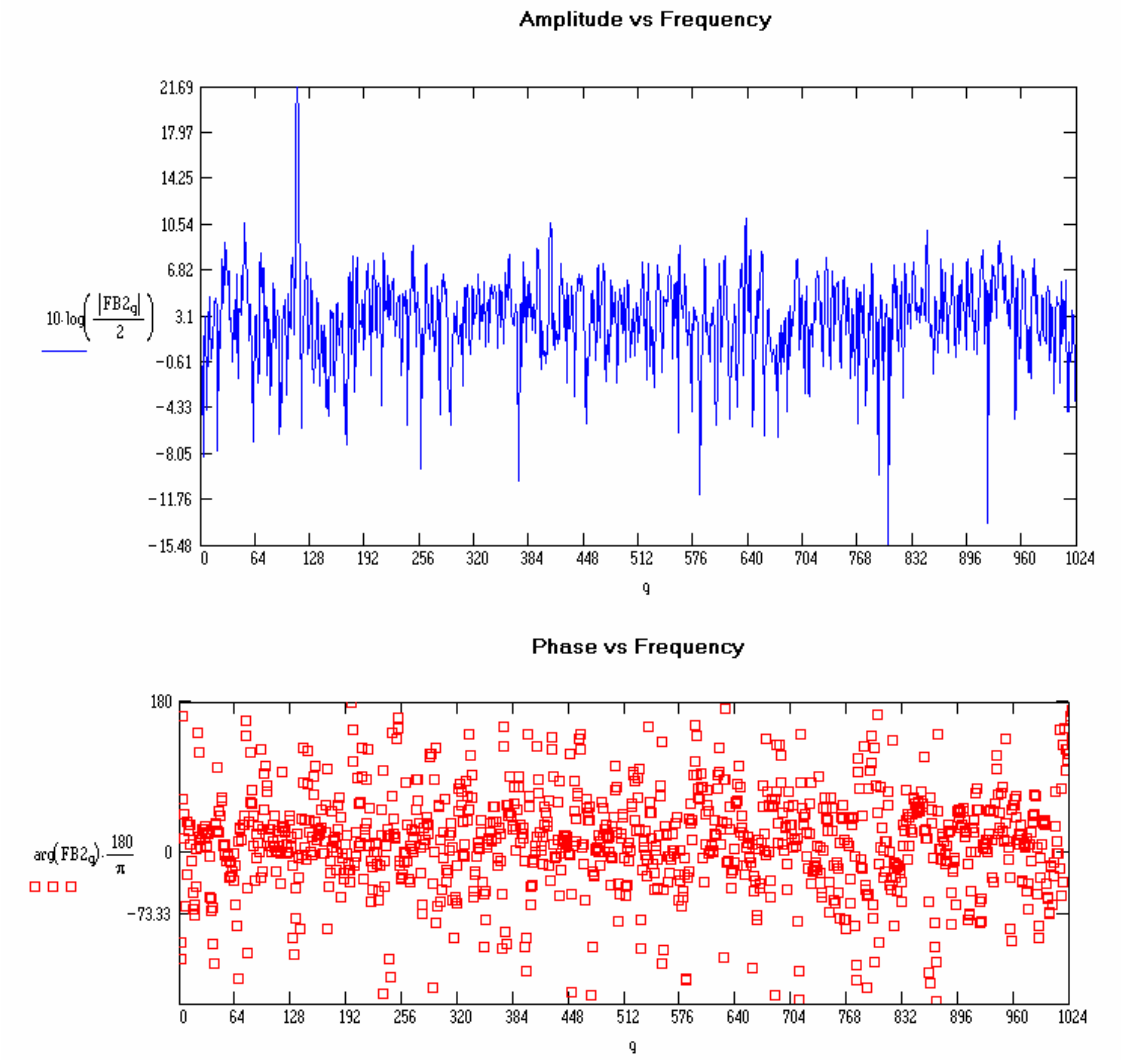
```
aaaaaaaa     W0: START SYNC WORD -- OK
e001006a     W1: B31=ASIC[1] Yin=1 Xin=1 YSyner=0 XSyner=0 ACC_OV=0 OVR=0 Rsrv=000000 NUM_CLAGS= 128 CCC=13 Cmmd=010
076423c8     W2: BBID-Y=0 SBID-Y= 7 SID-Y=100 BBID-X=1 SBID-X= 3 SID-X=200
d972e900     W3: LTA/Phase bin=55666 Recirc_blk-Y=233 Recirc_blk-X=  0
0d408a04     W4: TIMESTAMP-0= 222333444
211ecd59     W5: TIMESTAMP-1= 555666777
00000869       W6: DVCOUNT-Cntr=       2153
00000847       W7: DVCOUNT-Edge=       2119
0003a300     W8: DATA_BIAS   =    238336
0003a545     Lag    0 =     238917
0003a3e6     Lag    0 =     238566
0003a5f8     Lag    1 =     239096
0003a3d8     Lag    1 =     238552
0003a370     Lag    2 =     238448
0003a1fa     Lag    2 =     238074
0003a3a6     Lag    3 =     238502
0003a078     Lag    3 =     237688
0003a2af     Lag    4 =     238255
0003a1d2     Lag    4 =     238034
0003a2ce     Lag    5 =     238286
0003a268     Lag    5 =     238184
0003a3b6     Lag    6 =     238518
0003a256     Lag    6 =     238166
0003a1fc     Lag    7 =     238076
0003a1fa     Lag    7 =     238074
.
.
.
0003a20a     Lag  125 =     238090
0003a3fe     Lag  125 =     238590
0003a6cc     Lag  126 =     239308
0003a57c     Lag  126 =     238972
0003a550     Lag  127 =     238928
0003a418     Lag  127 =     238616
1c71c71c     W265: END SYNC WORD -- OK
b9fa8535     W266: Checksum calculated OK
```

CBE raw frame output

```
1.675218060543869e-01    -1.723961005643920e-01
3.732683427398666e-02    -1.918932786044125e-01
-5.438686505900462e-02   -1.096716264751154e-01
1.282709081580298e-03      5.246280143663417e-02
.
.
.
```

CBE raw floating-point output


Re(CL2)q
3
2
1
0
−1
0
204.8
409.6
614.4
819.2
1024
1228.8
1433.6
1638.4
1843.2
2048
q
Im(CL2)q
2
1
0
−1
−2
0
204.8
409.6
614.4
819.2
1024
1228.8
1433.6
1638.4
1843.2
2048
q


Amplitude vs Frequency
21.69
17.97
14.25
10.54
6.82
3.1
−0.61
−4.33
−8.05
−11.76
−15.48
10·log(|FB2q|/2)
0
64
128
192
256
320
384
448
512
576
640
704
768
832
896
960
1024
q
Phase vs Frequency
180
0
−73.33
arg(FB2q)·180/π
0
64
128
192
256
320
384
448
512
576
640
704
768
832
896
960
1024
q

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Test Equipment

- Agilent 16900A/16950A **logic analyser**.
  - 64 channels, 600 MHz state, 4 GHz timing.
  - Mate with soft-touch probe headers on board.
  - 4 test pins out of FPGAs.
- Agilent Infineon **Digital Storage Oscilloscope**.
  - 4 channels, 20 Gs/s/channel. 7 GHz bandwidth.
  - 2 differential or single-ended probes.
  - Probing…difficult due to speed, signal integrity, routing density…use signal vias…special probing kits.
  - Jitter analysis software.
- X-ray machine, BGA re-work machine.

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Prototype System Testing

- Connect Station Board outputs to Baseline Board inputs.
- Establish/test HM Gbps connectivity.
- Delay Module test vectors stimulate Station Board and downstream Baseline Board.
  - Compare results with software filter/correlator that processes the same test vectors.
  - Not bit-exact comparison…statistical only.

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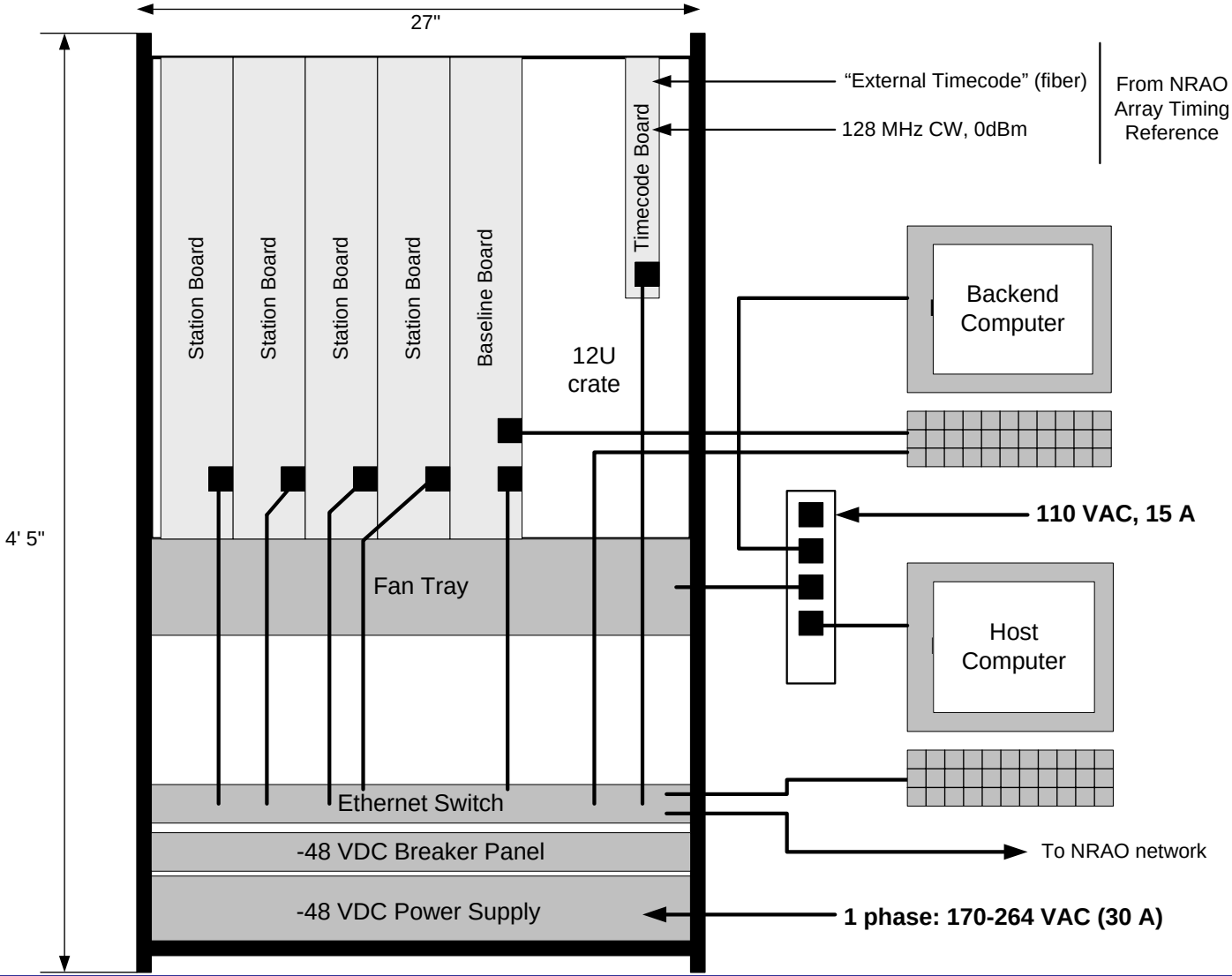
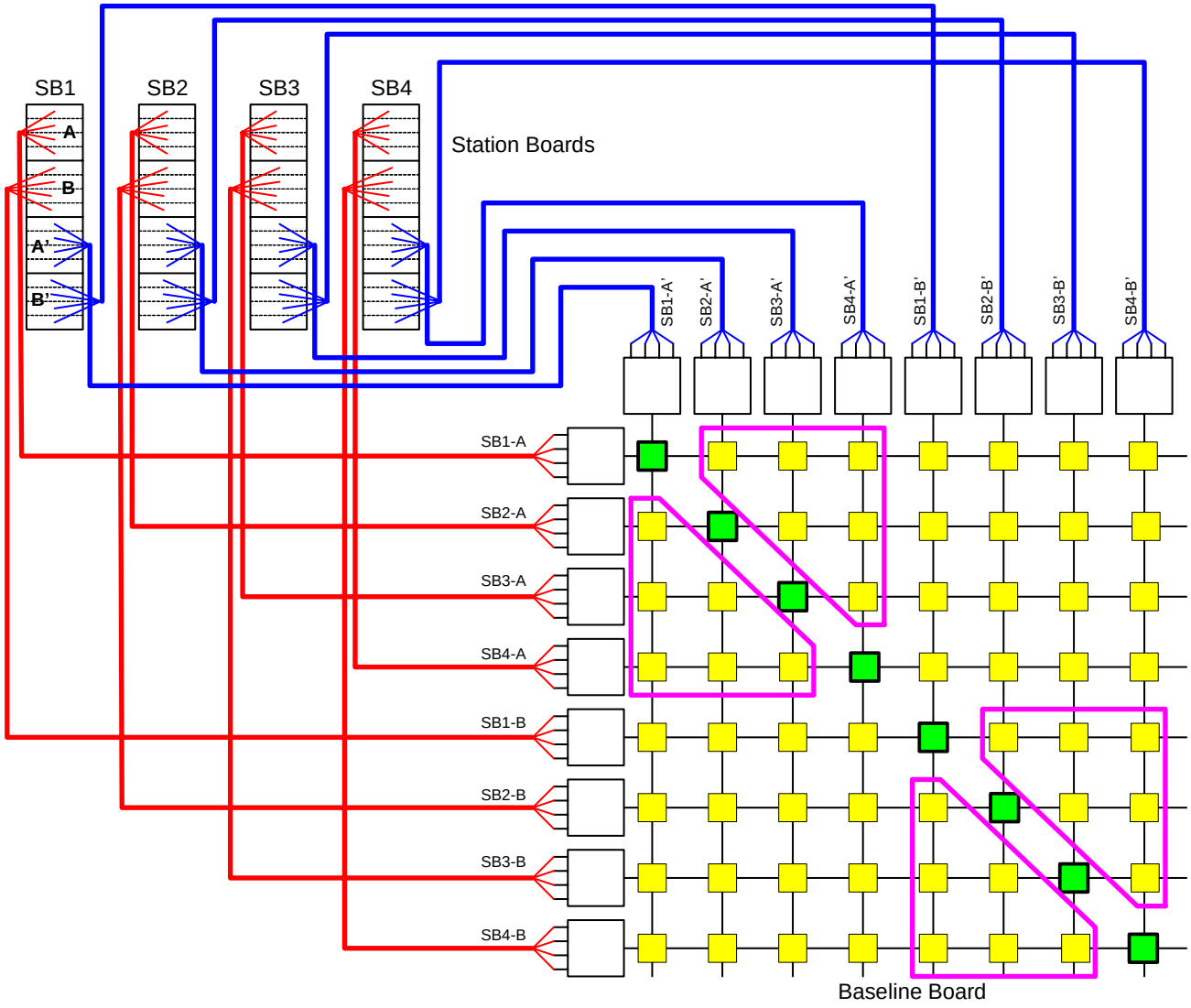
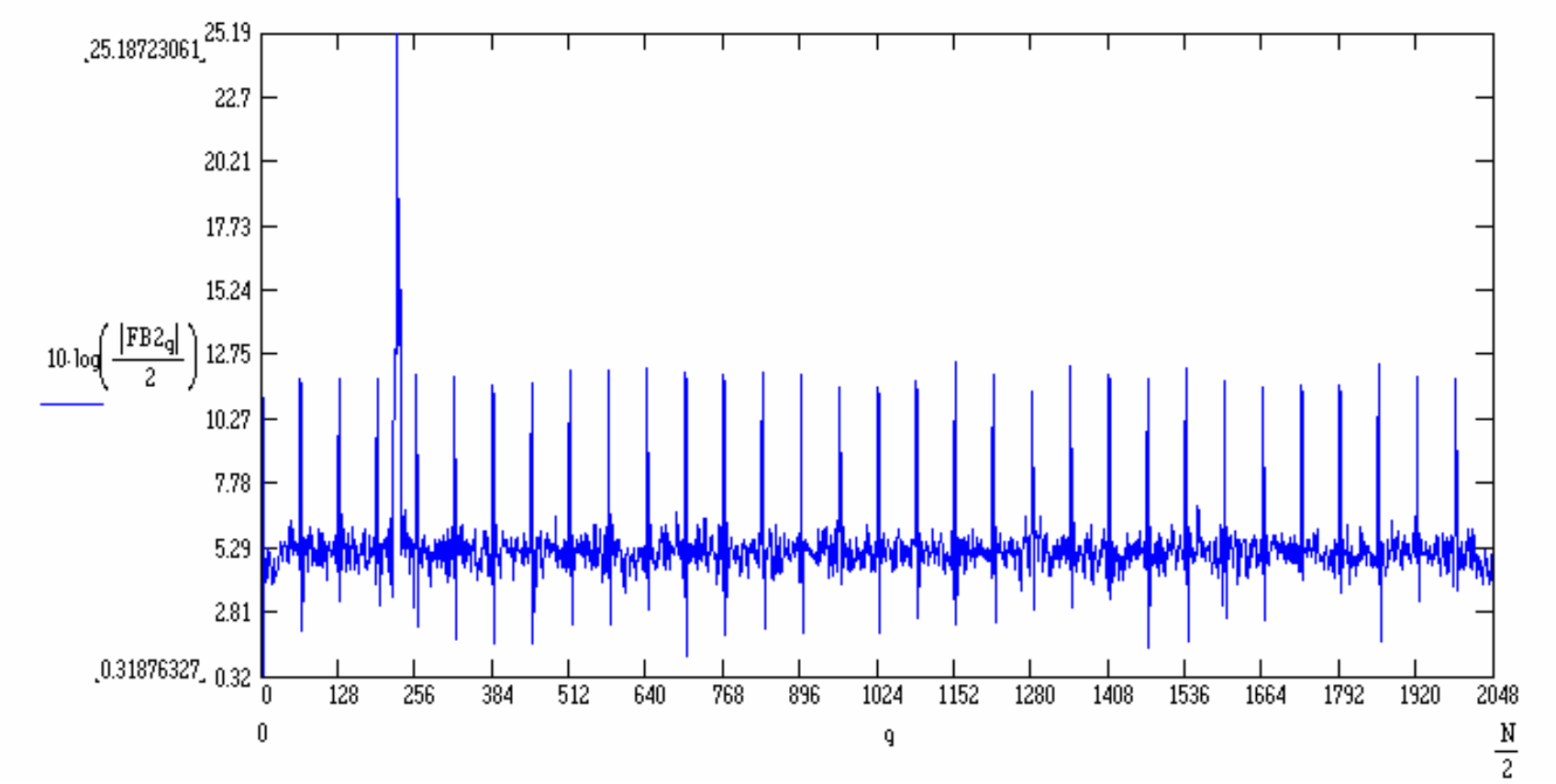
On-the-Sky Testing (OTS)

- DRAFT Test Plan A25010N0005.
- Prototype correlator test setup.
- 45 tests. Specified in plan in an overview fashion. Details filled in with GUIs/configuration files.
- Digital tone comb generator in DTS Tx or Rx or Station Board Input Chip useful…for detecting timing/delay tracking hiccups with Filter Chip tone extractor.


27"
4' 5"
Station Board
Station Board
Station Board
Station Board
Baseline Board
Timecode Board
12U
crate
"External Timecode" (fiber)
128 MHz CW, 0dBm
From NRAO
Array Timing
Reference
Backend
Computer
110 VAC, 15 A
Fan Tray
Host
Computer
Ethernet Switch
-48 VDC Breaker Panel
To NRAO network
-48 VDC Power Supply
1 phase: 170-264 VAC (30 A)


SB1
SB2
SB3
SB4
A
B
A'
B'
Station Boards
SB1-A'
SB2-A'
SB3-A'
SB4-A'
SB1-B'
SB2-B'
SB3-B'
SB4-B'
SB1-A
SB2-A
SB3-A
SB4-A
SB1-B
SB2-B
SB3-B
SB4-B
Baseline Board


25.18723061
25.19
22.7
20.21
17.73
15.24
12.75
10.27
7.78
5.29
2.81
0.31876327
0.32
10·log(|FB2q|/2)
0
128
256
384
512
640
768
896
1024
1152
1280
1408
1536
1664
1792
1920
2048
0
q
N/2

TEST	Purpose of Test	Description/Test Setup	Expected Outcome	Notes
0	Shipping damage check, prototype correlator installation and setup.	Unpack system, check for damage, install boards. Install system in test location.	All components available and undamaged. System installation successful.	Some assembly required.
1	System power-up and self-check with local 128 MHz oscillator on the Timecode Board.	Connect AC power to -48 VDC power supply. Connect AC power to to AC-powered components. Power-up system, use the Timecode local crystal oscillator. Perform Station Board checks. Perform Baseline Board checks. Check connectivity of Station-to-Baseline	All self-checks and functions ok. Backend receives frames. RTDD can display data products.	No antennas are required.
2	Computer network setup and check.	The Host Computer must be connected to the embedded processors via the switch. The switch is connected to the NRAO network to allow for time setting (or this setting may be manual via a control computer GUI), and for connection to Model Server.	Connected to network. Communications established with NRAO Model Server.	The control computer sets correlator configurations. The only connection to EVLA M&C is the Model Server and, optionally, the time setting.
3	Run self-checks with connection to NRAO "External Timecode", and 128 MHz 0 dBm CW.	Same as TEST 1, except use NRAO time reference. Check for timing synchronization of TIMECODE to array UTC.	TIMECODE synchronized to NRAO UTC. Phase-lock achieved on all chips on all boards. All intra-system checks ok.	No antennas required.

11	**First fringe test,** single, short baseline, 8-bit, 4-bit re-quantization. One sub-band. One antenna should be "Reference Antenna", with well-known LO fiber delay.	Set RF to C-band for minimal interference. Set antenna differential frequency shift to 1 kHz. Observe and track strong continuum source. Turn on digital tone comb generator in DTS transmitter. Turn on one sub-band filter at the center of the wideband.	Stable phase-cal ampl and phase vs time, with delay tracking active. State counts, auto-spectra, power measurements within normal regions. Cross-correlation fringes detected, displayed with RTDD. Ampl and phase vs frequency as expected. SNR as expecte	This test requires 2 antennas, possibly for an extended period of time.
12	First fringe check compared with old correlator, short baseline.	Single baseline fringes with old correlator for comparison with new correlator, TEST 11. Minimal setup change…route analog out of DTS receiver to old correlator. Fshifts turned off.	Check SNR and normalized amplitudes. Check spectrum. Check and compare with AIPS.	This test requires 2 antennas for a short period for the observation. Comparison of old and new correlator can be performed off-line.
13	Fringe test, single, short baseline, 3-bit, 4-bit re-quantization. One sub-band.	Set RF to X-band for full 2 GHz bandwidth. Set differential frequency shift to 1 kHz. Observe and track strong continuum source. Turn on digital tone comb generator in DTS transmitter. Turn on one sub-band filter at the center of the wideband. Turn o	Stable phase-cal ampl and phase vs time, with delay tracking active. State counts, auto-spectra, power measurements within normal regions. Cross-correlation fringes detected, displayed with RTDD. Ampl and phase vs frequency as expected. SNR as expecte	This test requires 2 antennas, possibly for an extended period of time.

31	High SNR solar observation.	Correlator settings as required by astronomy teams, possibly incorporating "wideband recirculation". Possibly requiring 64 lags per CCC output mode from correlator.	Results as required by astronomy teams.	This test requires 4 antennas for the duration of the experiment.
32	Narrowband, high-spectral resolution.	Maximum spectral resolution on desired sub-band bandwidth. Possibly 1 Hz resolution. Correlator settings, number of antennas, set by astronomy team. Try to exercise all stages in the Filter Chip.	Results as required by astronomy teams.	This test requires 4 antennas for the duration of the experiment.
33	Radar-mode data capture.	Set sub-band for capture to 31.25 kHz. Capture data into NFS files. Use Filter Chip Stage 2 mixer to stop fringes and very-fine delay tracking. Observe spectral-line source with continuum.	Correlate captured data in software. Ensure results are as expected.	This test requires 4 antennas for the duration of the data capture portion of the experiment.
34-44	Astronomer-driven key science experiments of various kinds: continuum, high dynamic range spectral-line, mixed continuum and spectral-line, pulsar, recirculation, fast dumping, long integrations, radar mode.			

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OTS

- Station Board real-time S/W *critical* for OTS testing.
  - Delay tracking…models from NRAO "Model Server".
  - Phase model generation.
  - Dump control (DUMPTRIG) generation.
  - Acquisition of state counts, wideband correlation coefficients, etc.

- "Programmer's Guide" (A25290N0000) contains comprehensive information on many low-level real-time functions that software needs to control.

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OTS

- Many tests require science input and work for source selection and image processing/data analysis.
- Last 10 tests are completely astronomer-driven experiments of various kinds.
- OTS testing not used to qualify hardware for Stage 3 production. Used to demonstrate correlator functionality, provide “early”-use correlator, 1st step in total system integration testing.

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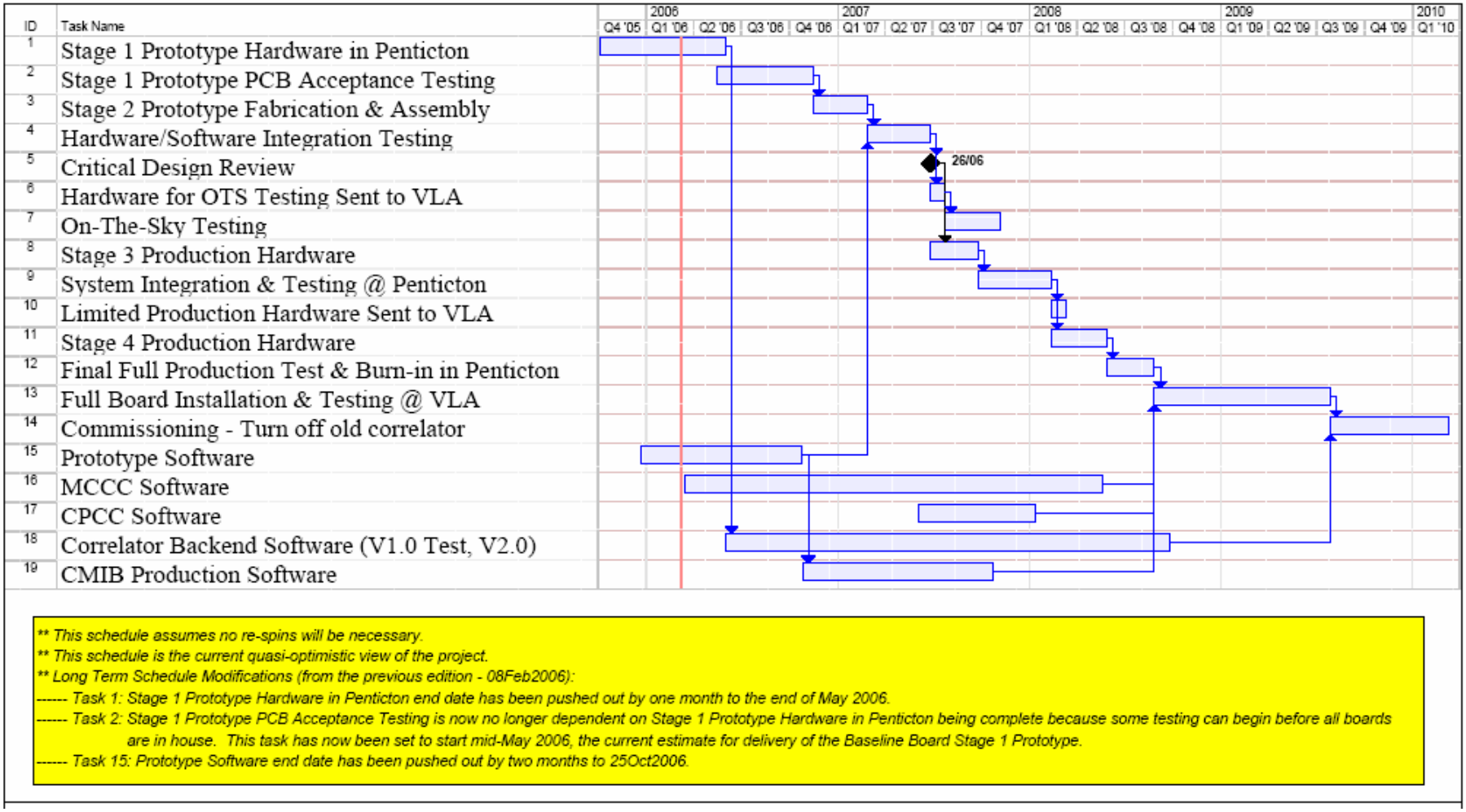
Schedule

- Many unquantifiable uncertainties/risks. Have paid in $, time, and tools to minimize risks as much as possible.
- Allocated ~6 months for initial prototype testing.
- Another ~6 months for getting proto corrs for OTS ready.
- ~4 months for OTS testing.
- ~Nov. 15/06 deadline for decision on Corr chip production in FY 06/07. Currently $ not in FY 06/07 budget.



*** This schedule assumes no re-spins will be necessary.*
*** This schedule is the current quasi-optimistic view of the project.*
*** Long Term Schedule Modifications (from the previous edition - 08Feb2006):*
------ Task 1: Stage 1 Prototype Hardware in Penticton end date has been pushed out by one month to the end of May 2006.
------ Task 2: Stage 1 Prototype PCB Acceptance Testing is now no longer dependent on Stage 1 Prototype Hardware in Penticton being complete because some testing can begin before all boards are in house. This task has now been set to start mid-May 2006, the current estimate for delivery of the Baseline Board Stage 1 Prototype.
------ Task 15: Prototype Software end date has been pushed out by two months to 25Oct2006.