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Expanded Very Large Array

Programmer's Guide to the EVLA Correlator

B. Carlson

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Outline

- Purpose.
- Timing and Delay Tracking.
- Phase Models.
- Dump Control.
- Station Board.
- Baseline Board.
- System.

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Purpose

- Comprehensive User Manual of the correlator from a programmer's perspective.
- Define details of timing, delay tracking, phase models, dump control.
- Discuss each function on each board/chip in some reasonable detail—note references to additional documentation.
- DRAFT2 released.

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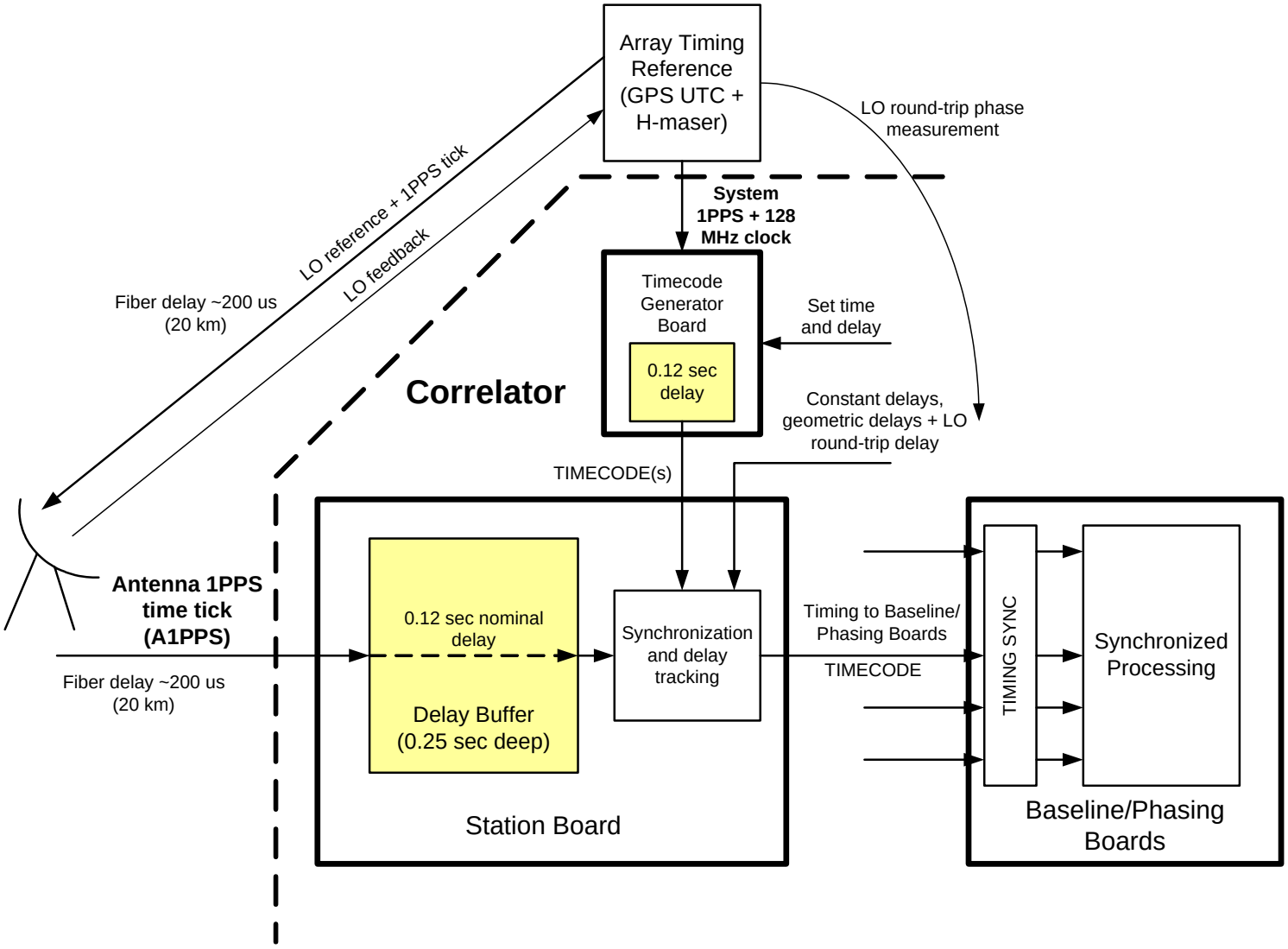
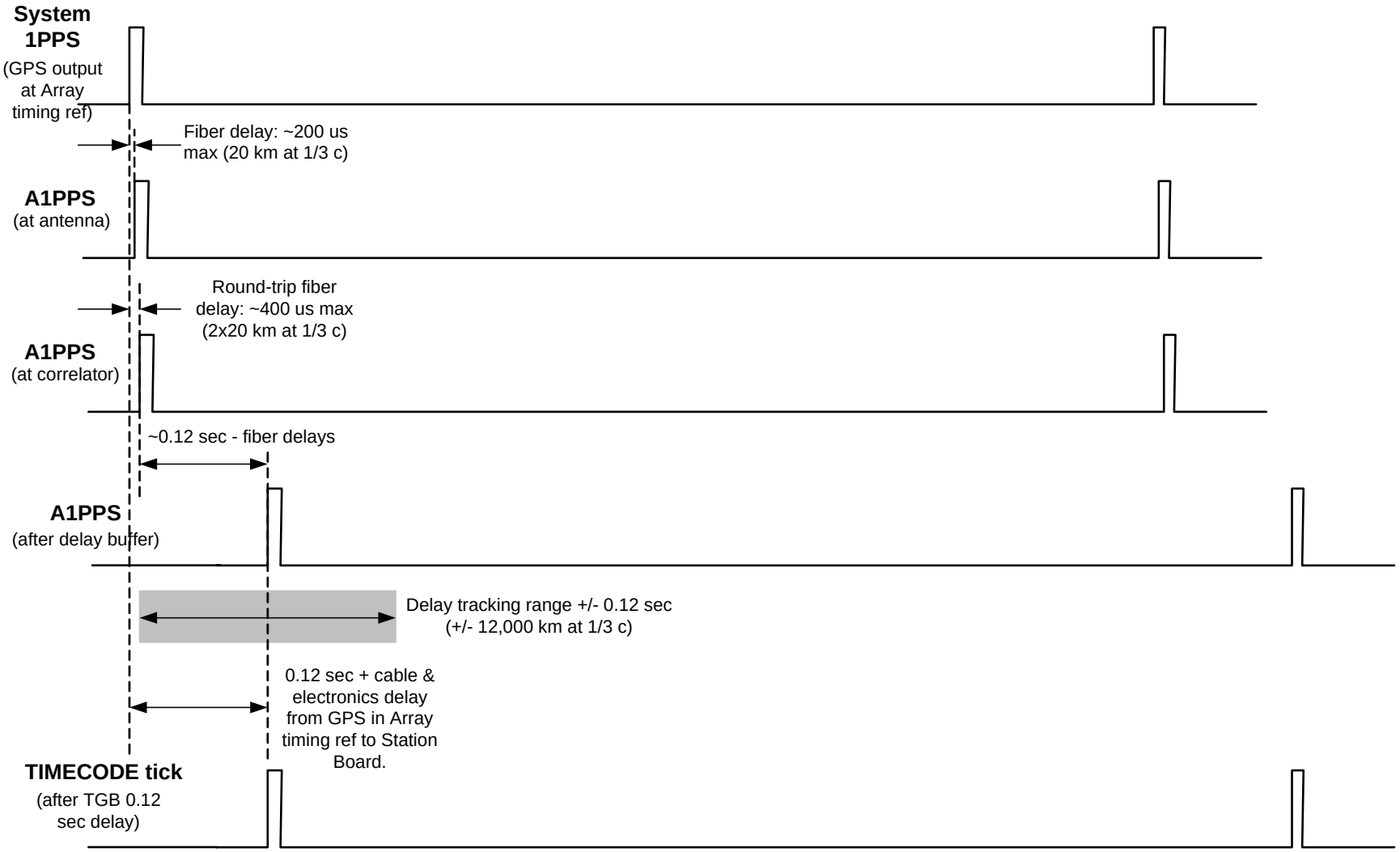
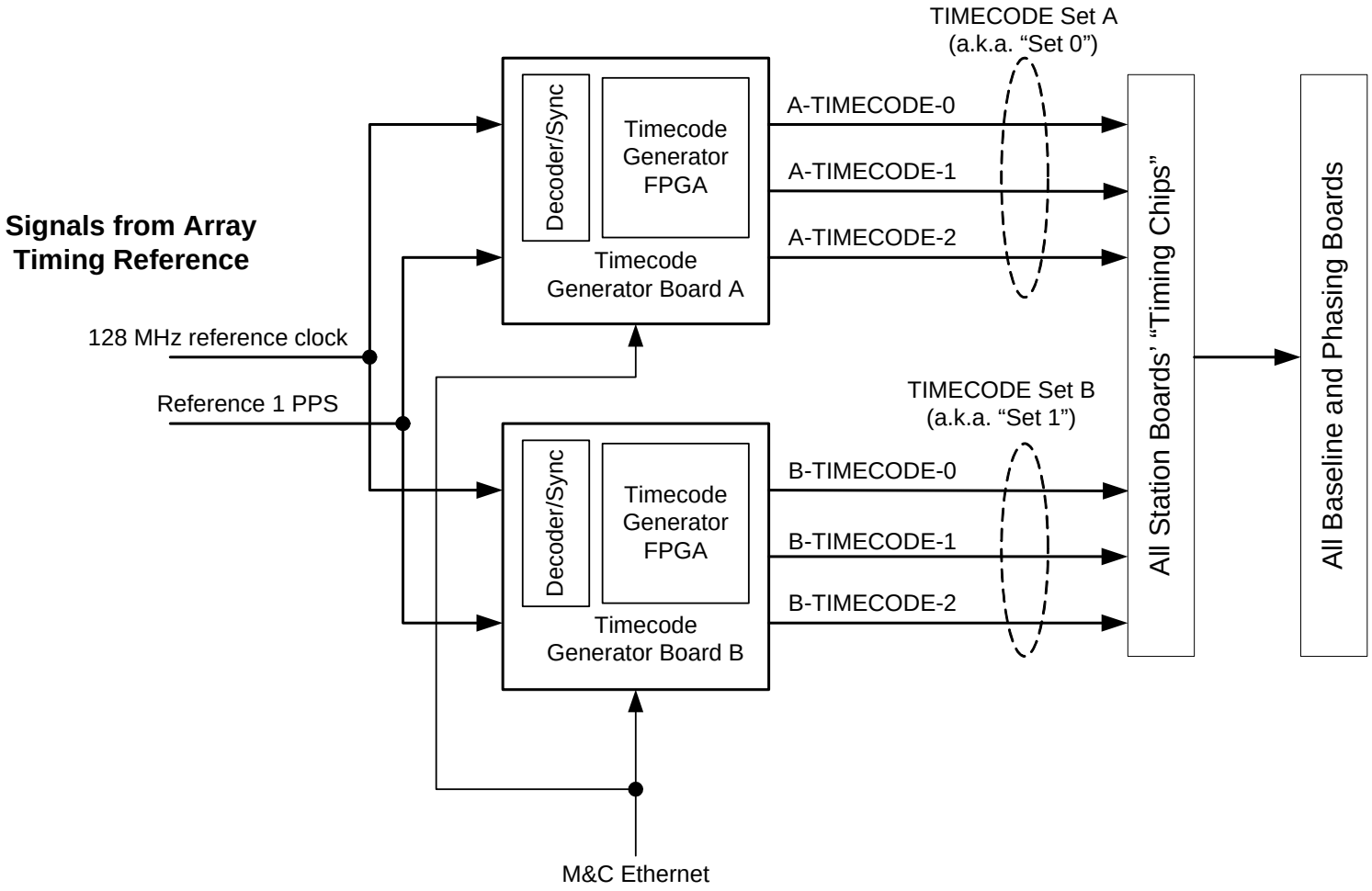
Timing and Delay Tracking

- Critical real-time functions to “get right” for OTS testing.
- Fundamental array/correlator timing. TIMECODE…
- Fiber delay models/compensation; accuracy of timestamp…accuracy of model application time.
- Delay sign convention.
- Wideband/sub-band delay tracking.

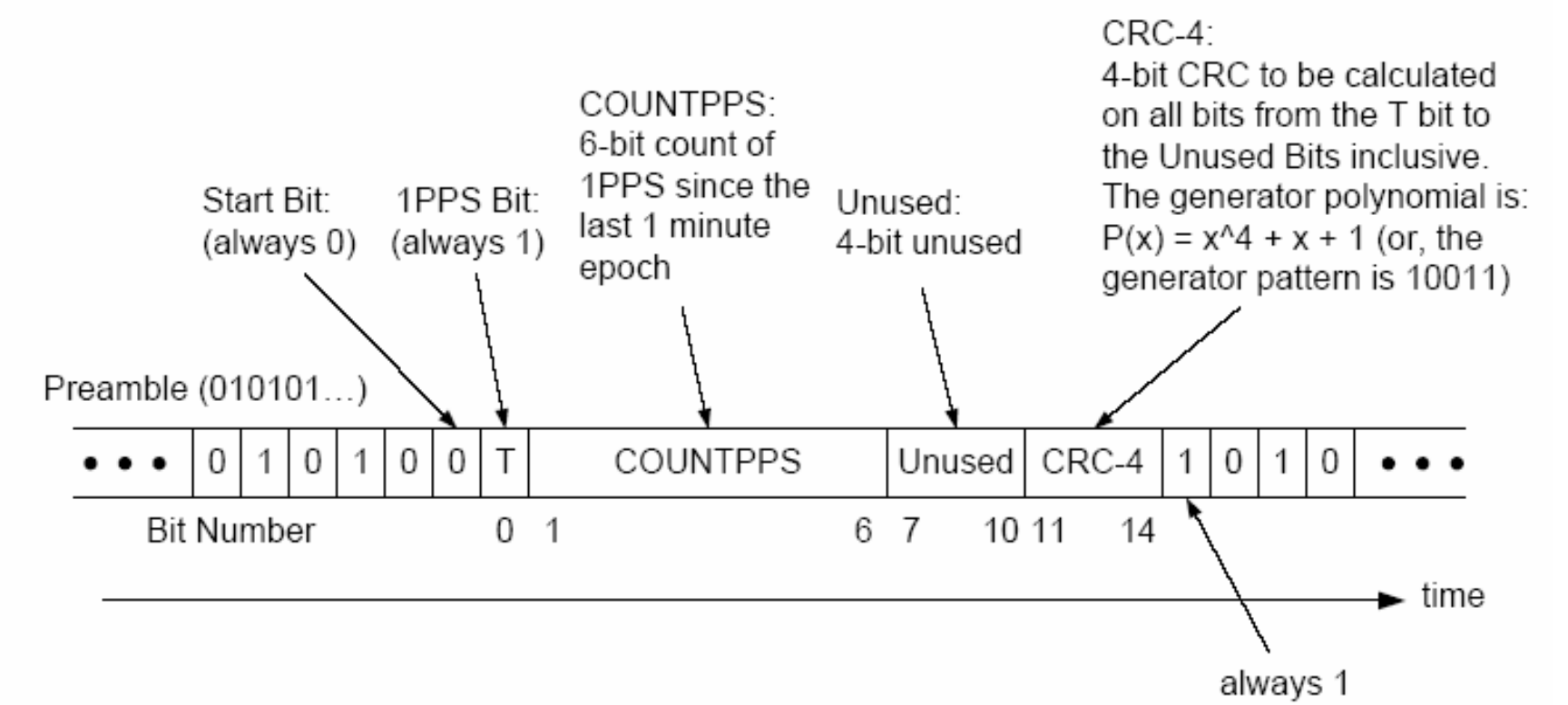

Array Timing Reference (GPS UTC + H-maser)
LO round-trip phase measurement
System 1PPS + 128 MHz clock
LO reference + 1PPS tick
LO feedback
Fiber delay ~200 us (20 km)
Timecode Generator Board
0.12 sec delay
Set time and delay
Correlator
Constant delays, geometric delays + LO round-trip delay
TIMECODE(s)
Antenna 1PPS time tick (A1PPS)
0.12 sec nominal delay
Delay Buffer (0.25 sec deep)
Synchronization and delay tracking
Timing to Baseline/ Phasing Boards
TIMECODE
Fiber delay ~200 us (20 km)
Station Board
TIMING SYNC
Synchronized Processing
Baseline/Phasing Boards


System
1PPS
(GPS output
at Array
timing ref)
Fiber delay: ~200 us
max (20 km at 1/3 c)
A1PPS
(at antenna)
Round-trip fiber
delay: ~400 us max
(2x20 km at 1/3 c)
A1PPS
(at correlator)
~0.12 sec - fiber delays
A1PPS
(after delay buffer)
Delay tracking range +/- 0.12 sec
(+/- 12,000 km at 1/3 c)
0.12 sec + cable &
electronics delay
from GPS in Array
timing ref to Station
Board.
TIMECODE tick
(after TGB 0.12
sec delay)

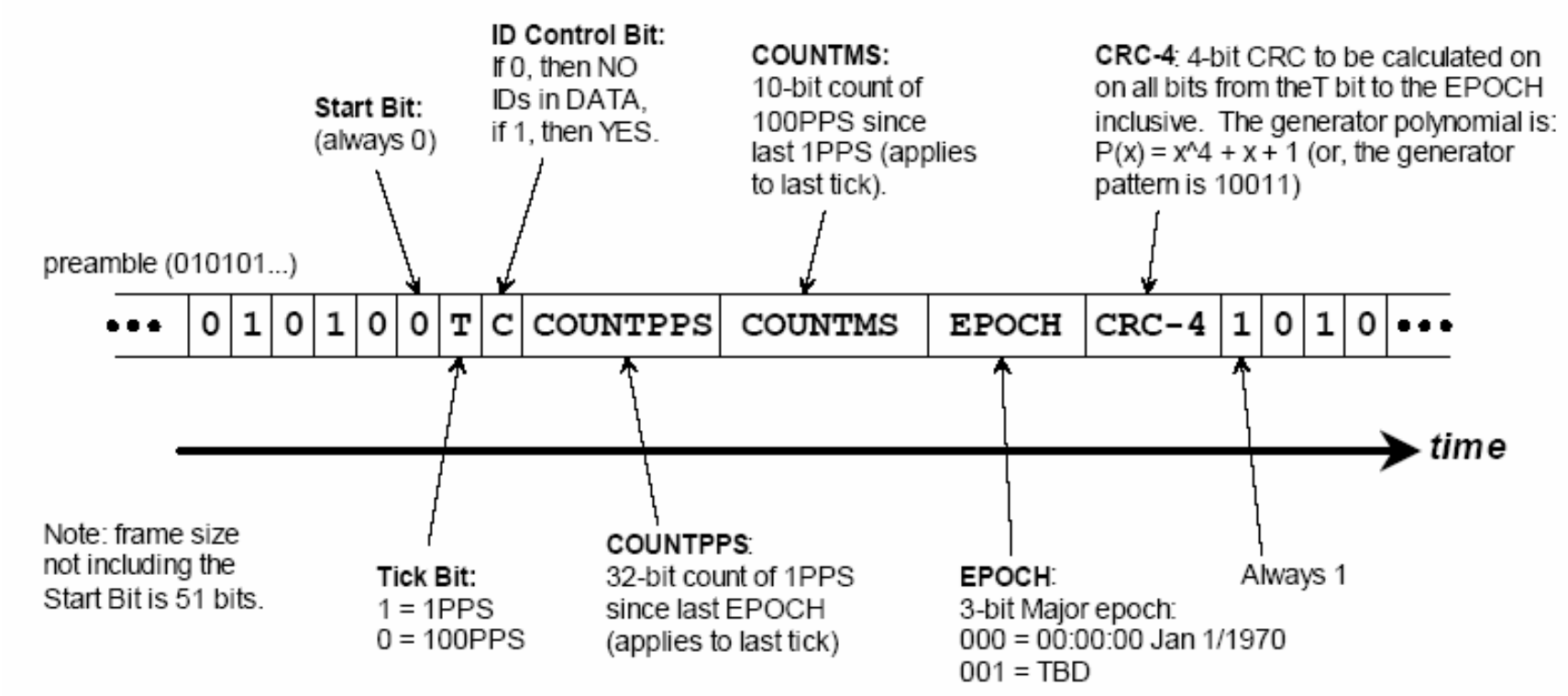
TIMECODE initialization/selection



External Timecode from NRAO



Correlator TIMECODE



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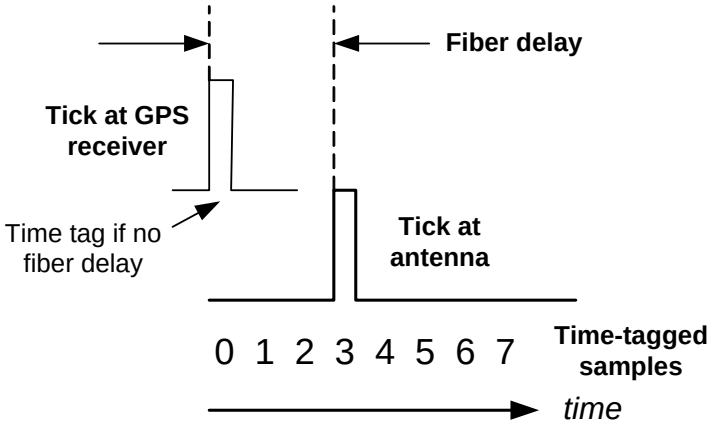
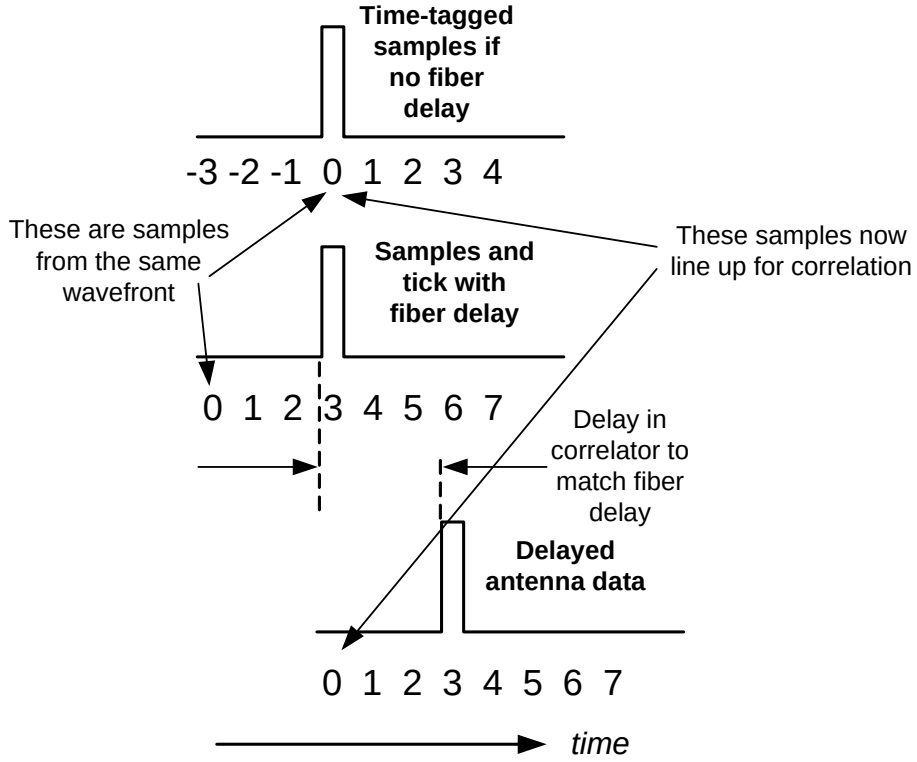
Fiber delay models

- Array Timing Reference-to-antenna fiber delays need to be known well enough to ensure that fringes are found within the delay search range of the correlator.
  - Min +/-250 nsec; max +/-32 usec for sub-band 128 MHz.
- Accuracy of fiber delay model for at least one antenna determines accuracy of timestamps and when models are applied in correlator.
- Fiber delays are put into the correlator as +'ve delay offsets.

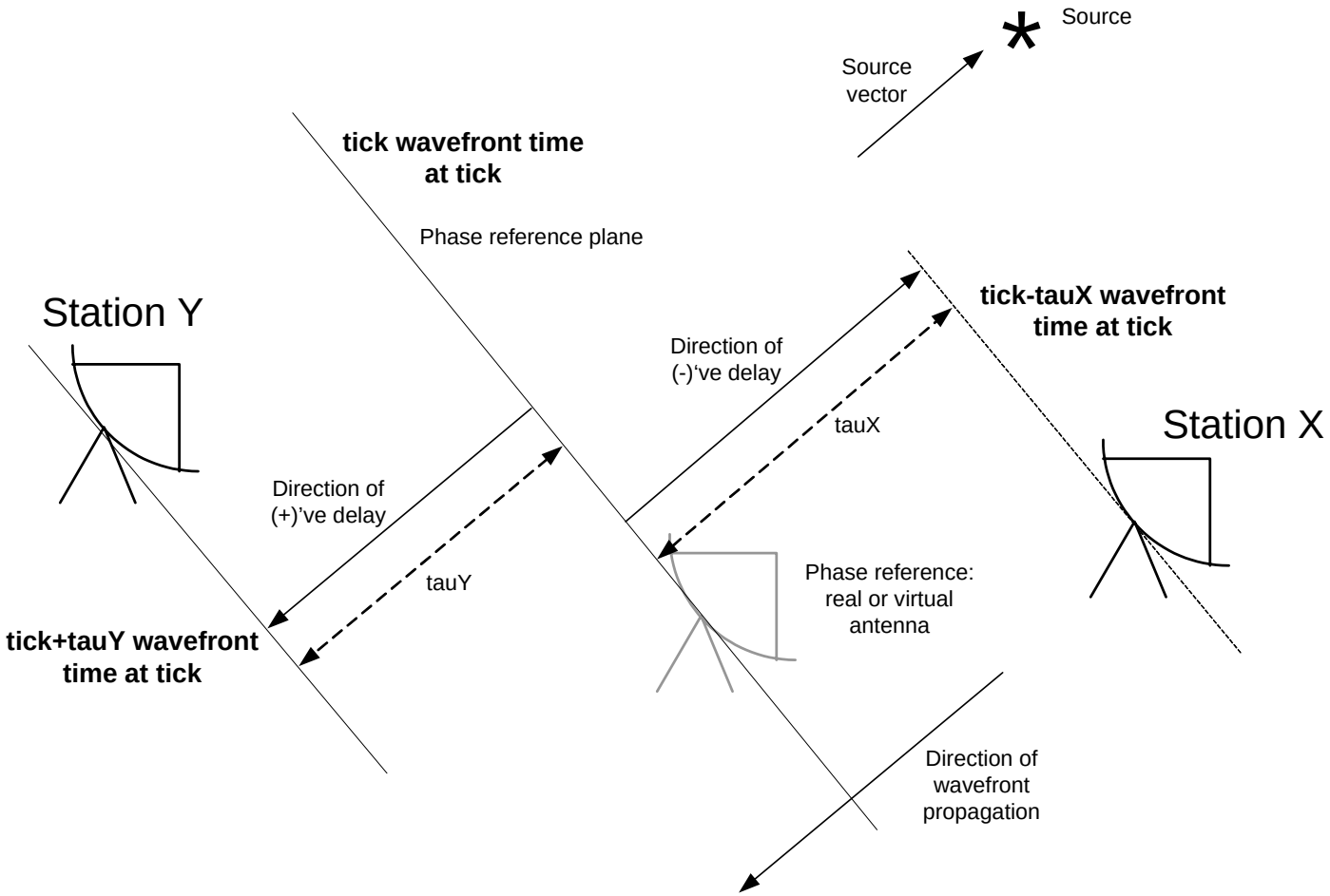

Fiber delay
Tick at GPS receiver
Time tag if no fiber delay
Tick at antenna
0 1 2 3 4 5 6 7
Time-tagged samples
time

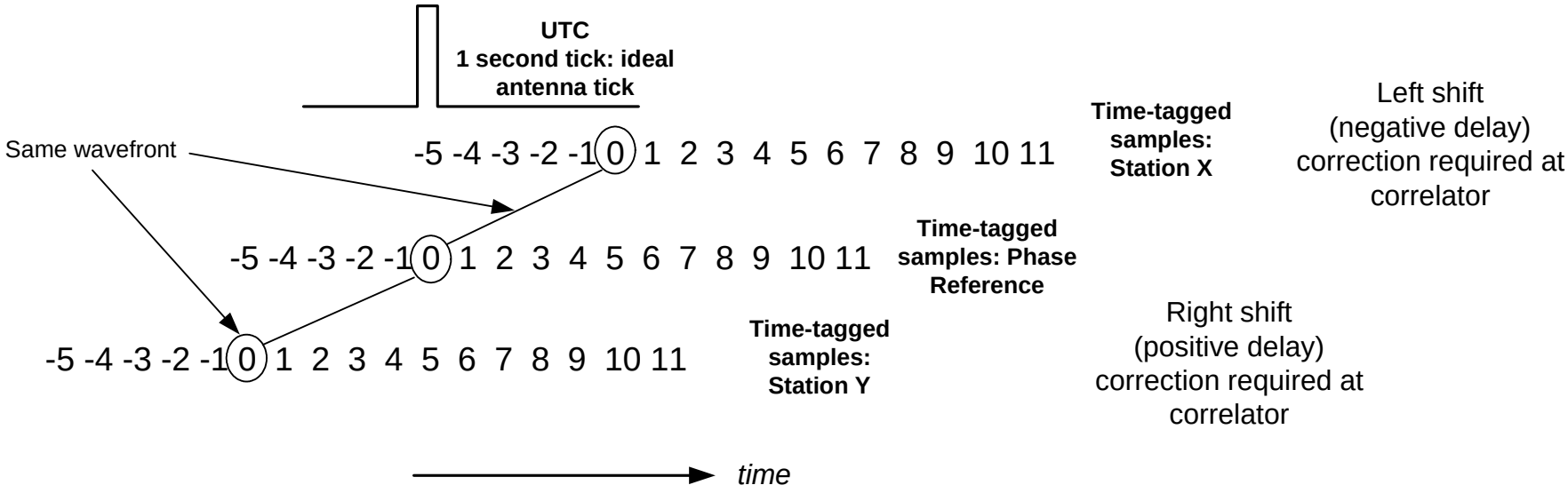
(a)


Time-tagged samples if no fiber delay
-3 -2 -1 0 1 2 3 4
These are samples from the same wavefront
These samples now line up for correlation
Samples and tick with fiber delay
0 1 2 3 4 5 6 7
Delay in correlator to match fiber delay
Delayed antenna data
0 1 2 3 4 5 6 7
time

(b)

Delay sign convention




UTC
1 second tick: ideal antenna tick
Same wavefront
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10 11
Time-tagged samples: Station X
Left shift (negative delay) correction required at correlator
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10 11
Time-tagged samples: Phase Reference
-5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10 11
Time-tagged samples: Station Y
Right shift (positive delay) correction required at correlator
time

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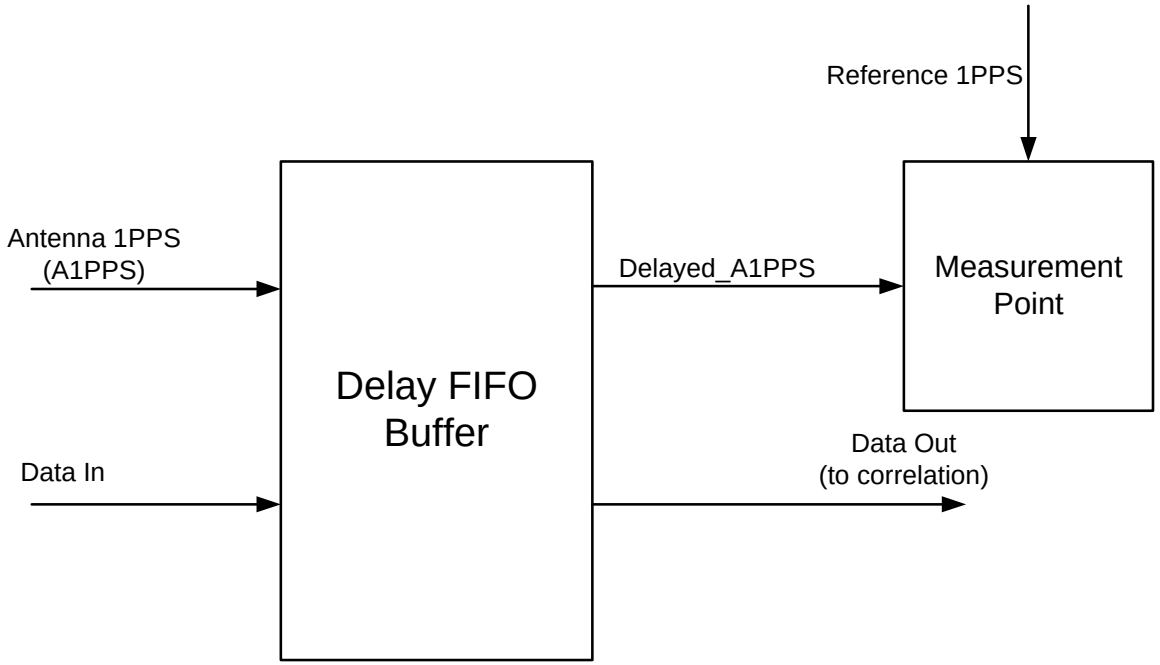
Delay Tracking

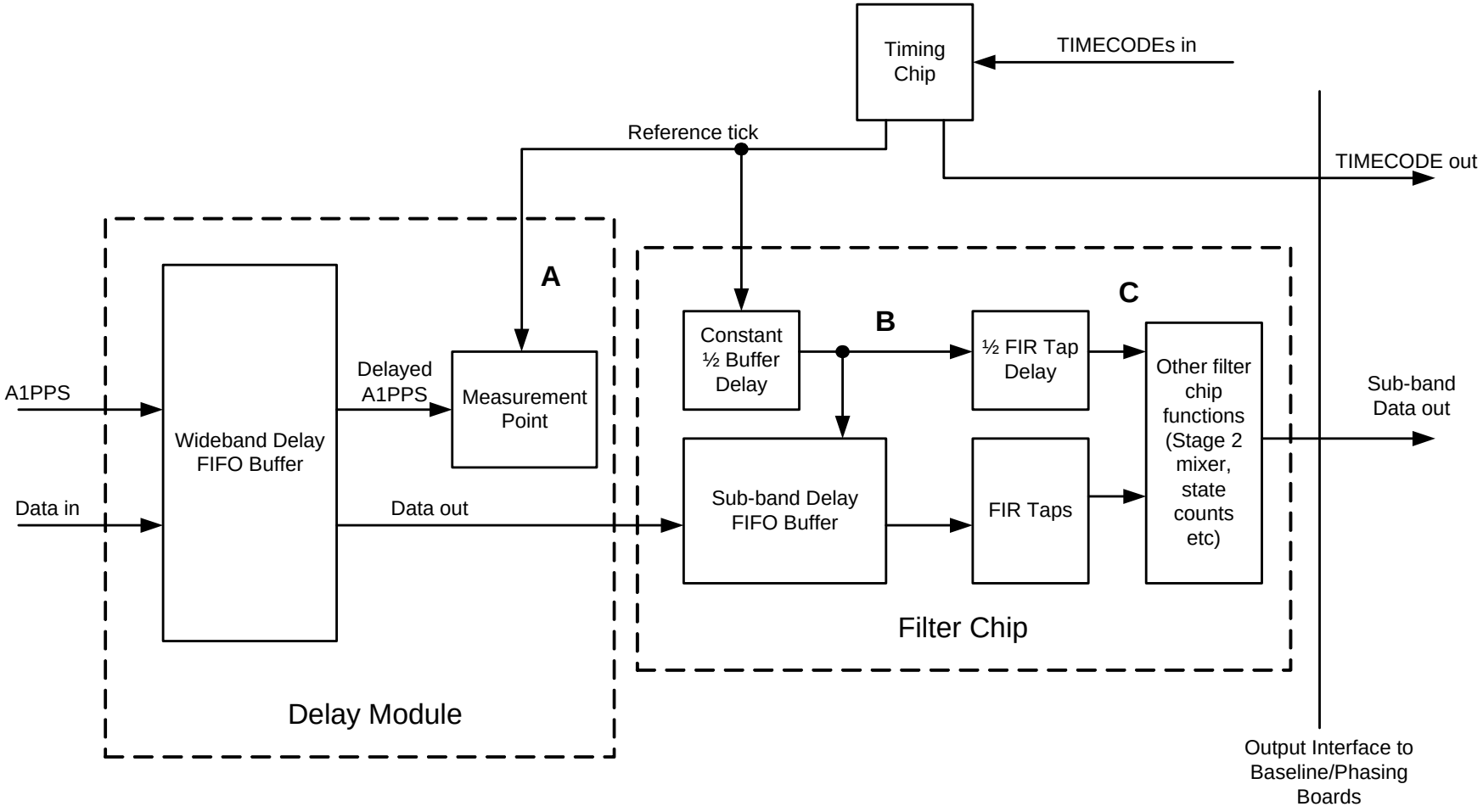
- Develop simplified model.

- Define the “Delay Tracker Quiescent State” to be when the A1PPS and the reference (TIMECODE) tick at output of delay buffer are lined up.
  - Sets value of Reference Pointer.
  - Allows antenna-to-correlator fiber delays to be completely factored out.

Delay Tracking—simple model



Delay tracking—actual model (simplified)



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Delay Tracking

- Wideband: handled by the Delay Module.
  - H/W logic handles complexity of de-multiplexed data stream and delay slewing; presents relatively simple software interface.
  - Concrete example given to go from floating-point point-slope model to H/W register values.
  - Delay always specified in terms of number of 244 psec (244.140625) units.
- Sub-band: handled by the Filter Chip (but operates on wideband data).
  - Similar to Delay Module, but only +/-16 usec.
  - Delay specified in terms of “samples at the original sample rate”.
  - Concrete example given…

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Delay Tracking

- Very fine delay tracking (+/-1/32 samples) handled and timed completely in hardware. S/W needs only to set where it is applied.

- Can be applied using the Filter Chip Stage 2 DSSB mixer or, in the Correlator Chip mixer (normally).
  - If applied in the Filter Chip, “PHASERR” going to the Baseline Boards is forced to 0 by H/W.

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Delay Tracking

- M&C delivers models to the correlator with a "Model Server".
  - Separate models for wideband delay and sub-band delay.
- Models:
  - Constant "clock model"…for constant LO distribution fiber delays.
  - LO fiber round-trip delay model.
  - Geometric delay model (CALC).
  - Could do WVR measurements if desired…
- Convenient if model's "t_o" in terms easily understood by the correlator (i.e. # seconds since Epoch – TIMECODE COUNTPPS).

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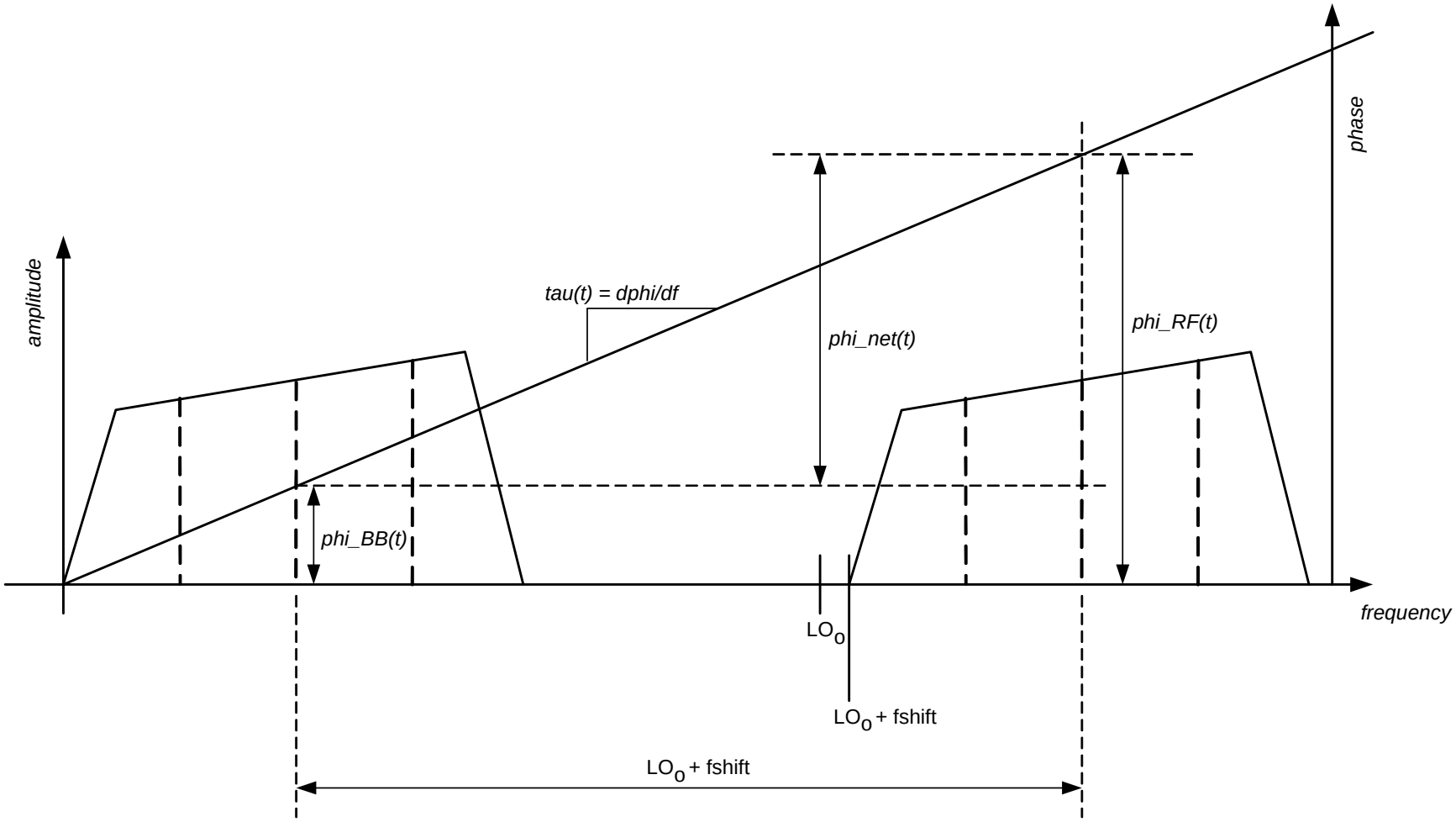
Phase Models and Fringe Rotation

- Earth-rotation phase, fiber round-trip phase, fshift phase.

- Normally applied in Correlator Chip.
  - Could be partially or completely applied in Filter Chip DSSB mixer but lose benefit of doing it at the last possible point (and mixer band-edge degradation).

- “t” of calculation depends on:
  - Delay through Filter Chip stages…measured for each Filter Chip in the Output Chip of the Station Board.
  - Recirculation parallel or serial phase.

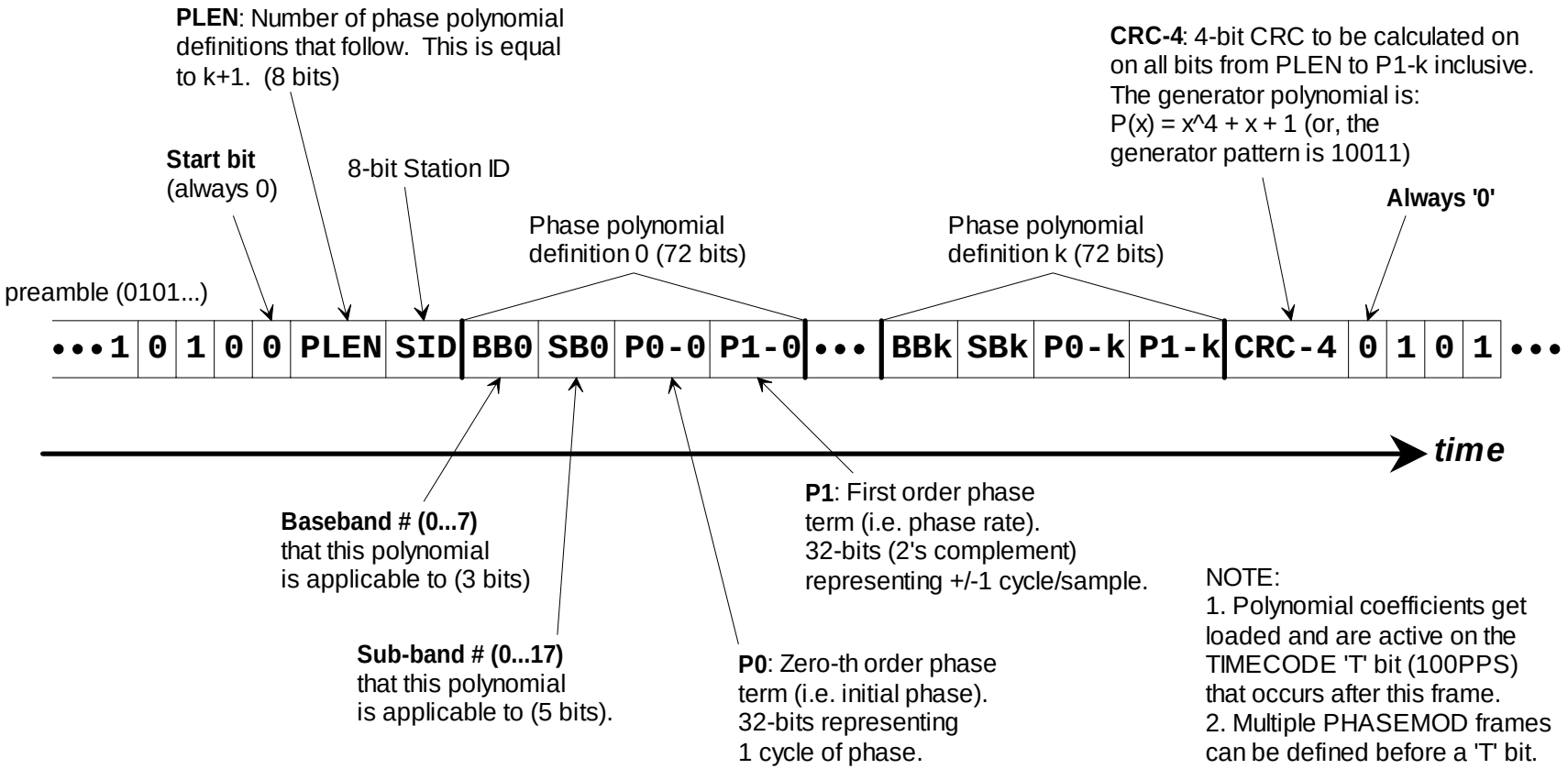

phase
amplitude
tau(t) = dphi/df
phi_net(t)
phi_RF(t)
phi_BB(t)
frequency
LO0
LO0 + fshift
LO0 + fshift

Phase Models and Fringe Rotation

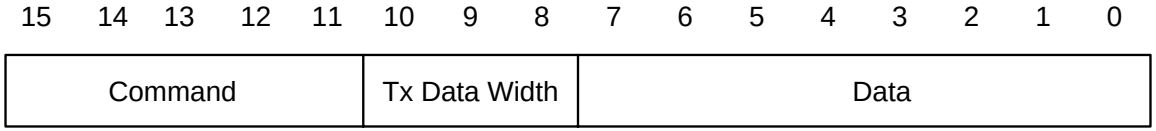
- Calculation is:

$$\phi(t) = -\tau(t) \times (Net\_LO) - fshift \times t$$

- Concrete example given…
  - Net_LO includes the fshift, and thus is different for each antenna.
  - How to calculate P0 and P1 PHASEMOD coefficients.
  - How to build the PHASEMOD frame—**HES**—Hardware Executable Script. Written to Timing Chip on Station Board.

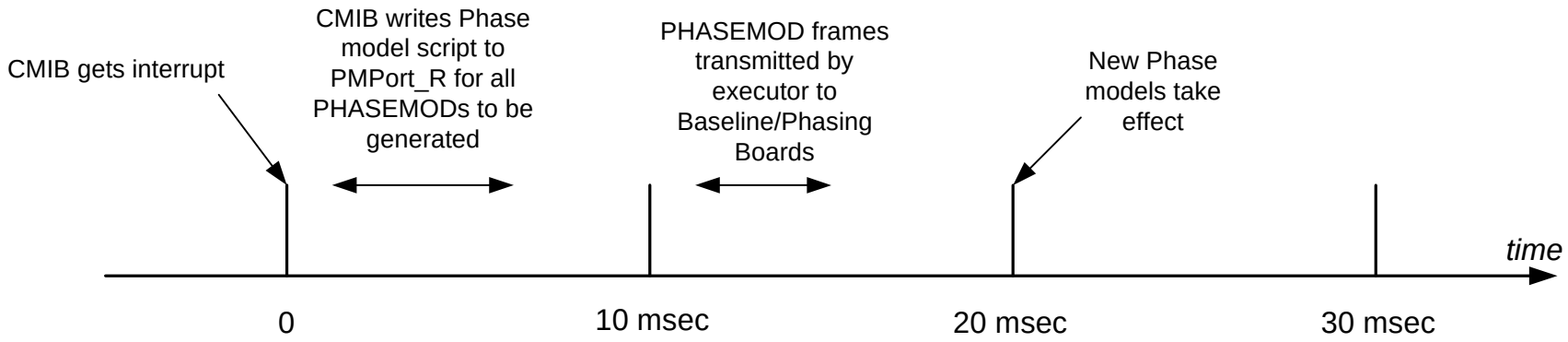


PHASEMOD Format



Command [15:11]	Command Name	Action
00000	N/A	Reserved. Ignored by the executor.
00001	**SBIT**	Generate a Start Bit. Effectively generates a '100' output.
00010	**FOD**	Generate **Width** bits of **Data**
00011	**CRC**	Generate a 4-bit CRC
00100	**END**	Stop execution, continuously generate Preamble (101010…), and wait for 10-msec tick to come along before executing the next Command written to the other RAM. **Once the microprocessor writes an END Command, it must not write any more Commands until after the next 10-msec tick**.
1xxxx	**NOP**	Generate a defined ***count***+1 of the '10' pattern. **Here, *count* is bits 0-14 of this word**.
All others	N/A	Reserved for future use. Ignored by the executor.

Cmd	Width	Data	Description
NOP	Count=99		100 Preambles to ensure first frame occurs well after the 10-msec tick.
SBIT	n/a	n/a	Start bit ‘100’ output
FOD	111	0x01	PLEN=1; this frame contains one PHASEMOD
FOD	111	0x55	SID=0x55
FOD	010	0x3	Baseband=3
FOD	100	0x10	Sub-band=16
FOD	111	0xFB	P0—Byte 0
FOD	111	0x3F	P0—Byte 1
FOD	111	0x86	P0—Byte 2
FOD	111	0x32	P0—MSByte 3
FOD	111	0x5D	P1—Byte 0
FOD	111	0xF1	P1—Byte 1
FOD	111	0xF4	P1—Byte 2
FOD	111	0xFF	P1—MSByte 3
CRC	n/a	na/	CRC-4 code
NOP	Count=9		Insert some Preamble for good measure
Other PHASEMOD frames…			
END	Count=31959		Preamble Fill


CMIB gets interrupt
CMIB writes Phase model script to PMPort_R for all PHASEMODs to be generated
PHASEMOD frames transmitted by executor to Baseline/Phasing Boards
New Phase models take effect
time
0
10 msec
20 msec
30 msec

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Phase Models and Fringe Rotation

- Each Station Board CMIB must write phase models (i.e. build PHASEMOD) for all of its own outputs.

- Other models may be present, but they are ignored by downstream hardware.

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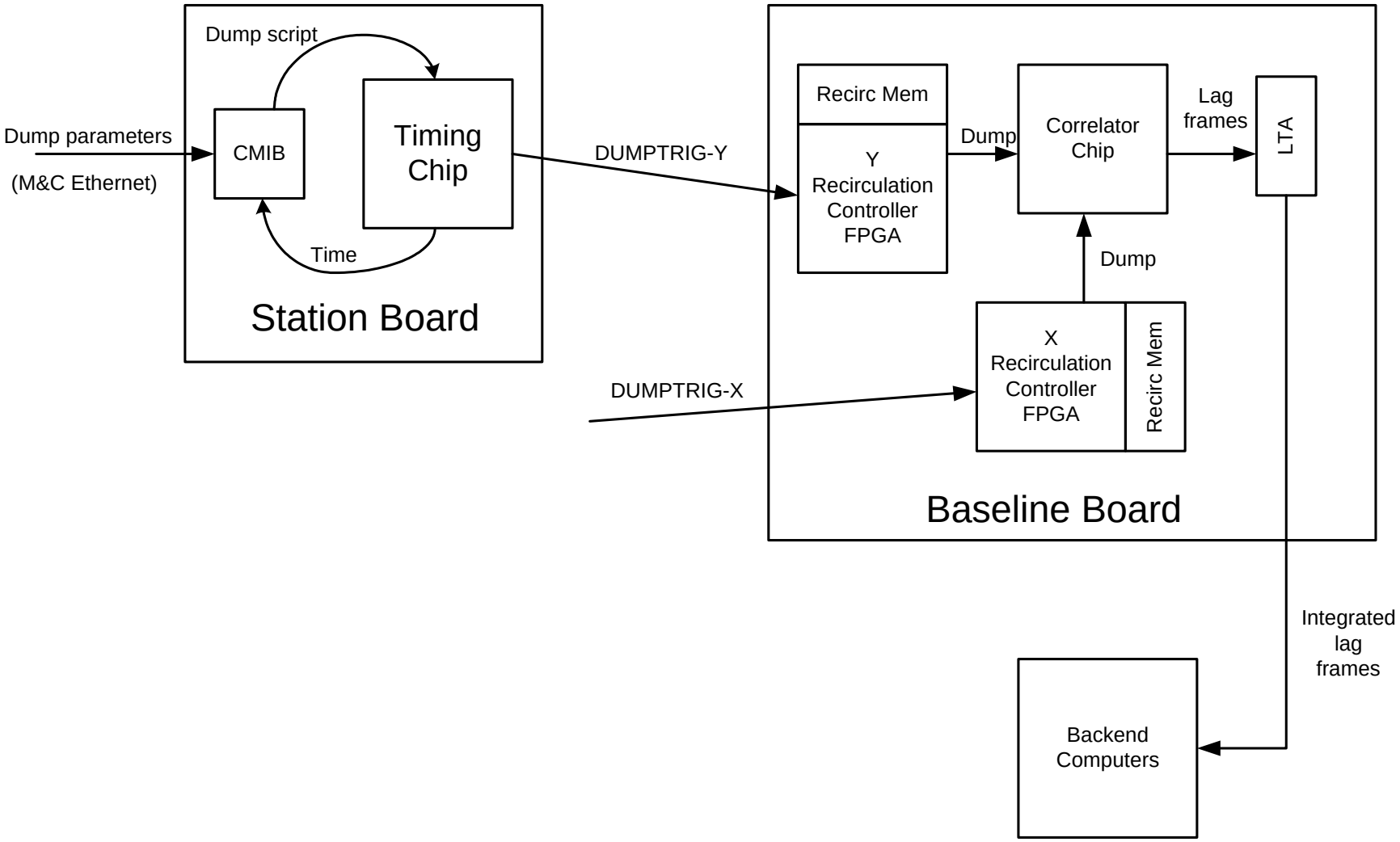
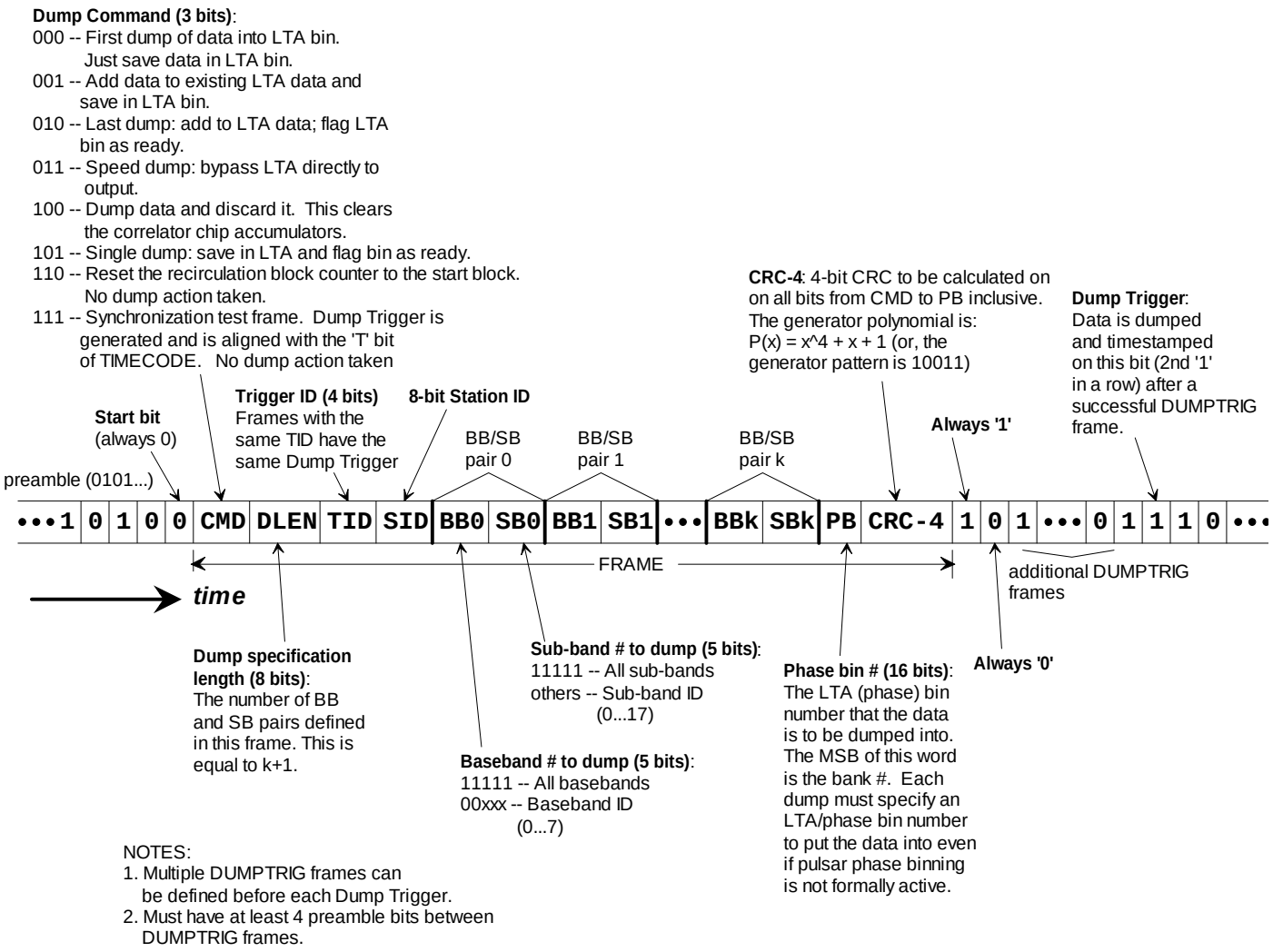
Dump Control

- Station Board generates the DUMPTRIG signal to control all down-stream dumping/integration for the Correlator Chip and the LTA.

- Sub-array/correlator-wide synchronization required to support recirculation and phase binning.
  - One way or another, synchronize to TIMECODE to eliminate Station Board-to-Station Board communication.

- HES built by S/W to generate DUMPTRIG.


Dump script
Dump parameters
(M&C Ethernet)
CMIB
Timing Chip
Time
Station Board
DUMPTRIG-Y
Recirc Mem
Y Recirculation Controller FPGA
Dump
Correlator Chip
Lag frames
LTA
Dump
X Recirculation Controller FPGA
Recirc Mem
DUMPTRIG-X
Baseline Board
Integrated lag frames
Backend Computers



DUMPTRIG Format

Dump CMD	Name	Description
000	**FDS**	**First Dump Save**. First dump of frame data into LTA bin. Save frame into LTA bin and overwrite existing data in bin **unless** the bin is flagged as ready for readout, in which case the new frame will be discarded.
001	**AFS**	**Add Frame Save**. Add frame data to existing LTA bin and save the result back into the same bin.
010	**LDS**	**Last Dump Save**. Add frame data to LTA bin, save result back into the same bin, and flag the bin as ready for readout (transmission to backend).
011	**SPD**	**Speed Dump**. Bypass LTA and transfer frame data to output for transmission to the backend.
100	**DD**	**Dump Discard**. This clears the Correlator Chip accumulators. This action is taken by the Correlator Chip; the LTA does not see the frame.
101	**SDS**	**Single Dump Save**. Save frame data in LTA bin and flag bin as ready.
110	**RRC**	**Reset Recirculation Counter**. Force reset of the recirculation block counter to the start block. No dump action is taken. This applies to any recirculation chip that receives this command (i.e. no selection of SID, BBID, SBID etc. is performed).
111	**STF**	**Synchronization Test Frame**. Receiver expects Dump Trigger aligned with the 'T' bit of TIMECODE. No dump action taken.

- H/W Integration Time (**HW_IT**) – This is the fundamental hardware dump/integration time and is expressed in seconds. For each HW_IT one or more DUMPTRIG frames and a Dump Trigger are generated, normally resulting in the generation of one or more lag frames from the Correlator Chip.

- LTA Integration Time (**LTA_IT**) – This is the integration time in the LTA and is expressed in seconds. The LTA_IT must always be an integer multiple of HW_IT since the LTA always integrates an integer number of Correlator Chip lag frames.

- Backend Integration Time (**BE_IT**) – This is the integration time in the Backend computers and is expressed in seconds. The BE_IT must always be an integer multiple of LTA_IT, since the Backend always integrates an integer number of LTA frames.

For each stream (a stream being the output of a Digital Filter on the Station Board), there can be a different HW_IT. However, there is a hardware restriction in that every HW_IT must be an integer multiple of the smallest HW_IT that is in DUMPTRIG.

HW_IT_{max} is 500 μsec. *A larger HW_IT may result in overflow of the Correlator Chip accumulators.*

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Dump Modes

- Normal dump-and-integrate.
- Recirculation dump-and-integrate.
  - Recirc FPGA on Baseline Board handles all counting, memory pointer offsets etc. Driven by Dump Triggers and CMDs.
- Phase binning.
- Recirculation and phase binning ☹.
- Burst dumping.

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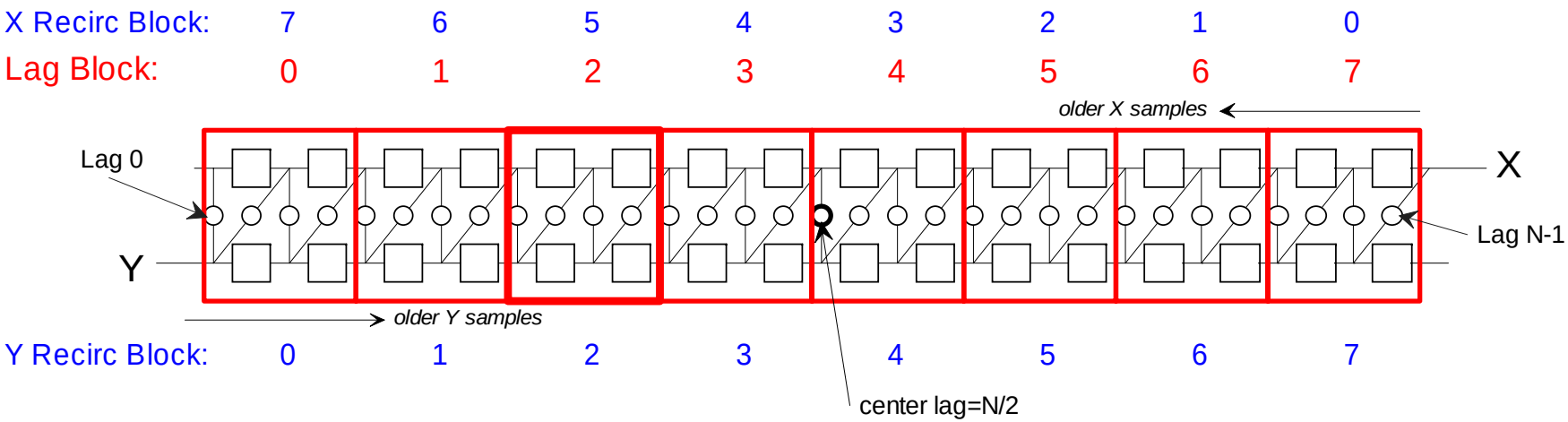
Normal dump-and-integrate

CMD	Time	Phase bin	Bank	Action
DD	*0*	*X*	*X*	*Dump/discard. Clears accumulators*
FDS	500 us	0	0	First dump into LTA
AFS	1 ms	0	0	Add to LTA
AFS	1.5 ms	0	0	Add to LTA
AFS	2.0 ms	0	0	Add to LTA
AFS	2.5 ms	0	0	Add to LTA
LDS	3.0 ms	0	0	Add to LTA, flag as ready
FDS	3.5 ms	1	0	First dump into LTA
AFS	4 ms	1	0	Add to LTA
AFS	4.5 ms	1	0	Add to LTA
AFS	5.0 ms	1	0	Add to LTA
AFS	5.5 ms	1	0	Add to LTA
LDS	6.0 ms	1	0	Add to LTA, flag as ready
FDS	6.5 ms	2	0	First dump into LTA
…	…	…		…

Recirculation dump-and-integrate

CMD	Time	Phase bin	Bank	Lags	Action
DD	*0*	*X*	*X*	*N/A*	*Dump/discard. Clears corr chip accumulators.*
RRC	*0*	*X*	*X*	*N/A*	*Force reset of recirc. block counter*
FDS	500 us	0	0	0-127	First dump of data into LTA
FDS	1 ms	0	0	128-255	First dump of data into LTA
FDS	1.5 ms	0	0	256-383	First dump of data into LTA
FDS	2.0 ms	0	0	384-511	First dump of data into LTA
RRC	*2.0 ms*	*X*	*X*	*N/A*	*Force reset of recirc. block counter*
AFS	2.5 ms	0	0	0-127	Add to LTA
AFS	3.0 ms	0	0	128-255	Add to LTA
AFS	3.5 ms	0	0	256-383	Add to LTA
AFS	4.0 ms	0	0	384-511	Add to LTA
RRC	*4.0 ms*	*X*	*X*	*N/A*	*Force reset of recirc. block counter*
LDS	4.5 ms	0	0	0-127	Add to LTA, flag as ready
LDS	5.0 ms	0	0	128-255	Add to LTA, flag as ready
LDS	5.5 ms	0	0	256-383	Add to LTA, flag as ready
LDS	6.0 ms	0	0	384-511	Add to LTA, flag as ready
RRC	*6.0 ms*	*X*	*X*	*N/A*	*Force reset of recirc. block counter*
FDS	6.5 ms	1	0	0-127	First dump of data into LTA
FDS	7.0 ms	1	0	128-255	First dump of data into LTA
FDS	7.5 ms	1	0	256-383	First dump of data into LTA
FDS	8.0 ms	1	0	384-511	First dump of data into LTA
RRC	*8.0 ms*	*X*	*X*	*N/A*	*Force reset of recirc. block counter*
AFS	8.5 ms	1	0	0-127	Add to LTA
…	…	…	…	…	…

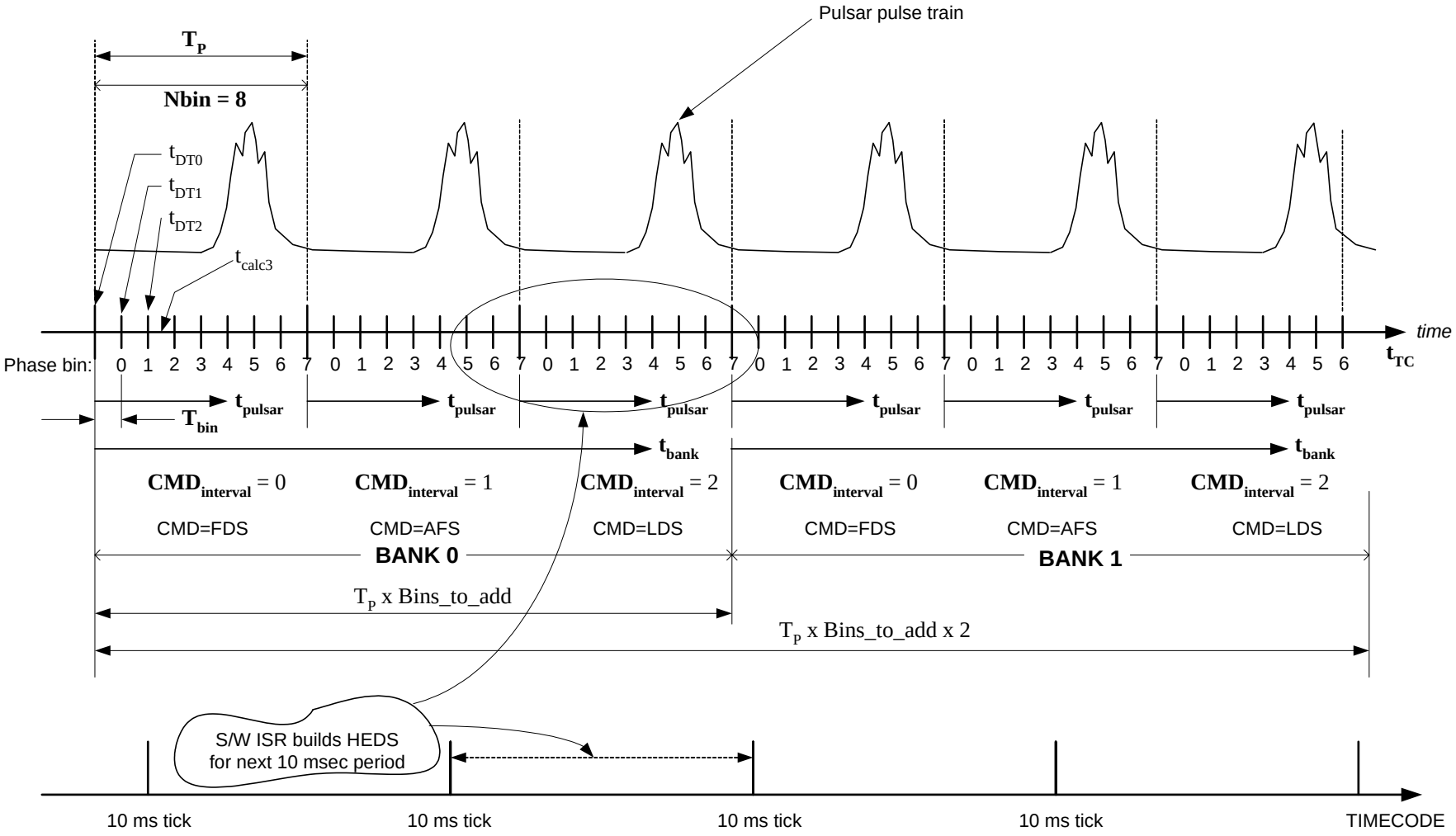
N-lag Correlator Recirculation Block Numbering
(for case of N=32, block size = 4 lags)



Phase binning

CMD	Time	Phase bin	Bank	Action
DD	*0*	*X*	*X*	*Dump/discard. Clears corr chip accumulators.*
FDS	250 μs	0	0	First dump bin 0
FDS	500 μs	1	0	First dump bin 1
FDS	750 μs	2	0	First dump bin 2
FDS	1 ms	3	0	First dump bin 3
FDS	1.25 ms	4	0	First dump bin 4
AFS	1.5 ms	0	0	Add to LTA bin 0
AFS	1.75 ms	1	0	Add to LTA bin 1
AFS	2 ms	2	0	Add to LTA bin 2
AFS	2.25 ms	3	0	Add to LTA bin 3
AFS	2.5 ms	4	0	Add to LTA bin 4
AFS	2.75 ms	0	0	Add to LTA bin 0
AFS	3 ms	1	0	Add to LTA bin 1
AFS	3.25 ms	2	0	Add to LTA bin 2
AFS	3.5 ms	3	0	Add to LTA bin 3
AFS	3.75 ms	4	0	Add to LTA bin 4
LDS	4 ms	0	0	Add to LTA, flag as ready bin 0
LDS	4.25 ms	1	0	Add to LTA, flag as ready bin 1
LDS	4.5 ms	2	0	Add to LTA, flag as ready bin 2
LDS	4.75 ms	3	0	Add to LTA, flag as ready bin 3
LDS	5 ms	4	0	Add to LTA, flag as ready bin 4
FDS	5.25	0	1	First dump bin 0, bank 1
…	…	…	…	…

Based on this example, it is useful to develop an algorithm that, given TIMECODE in seconds and the pulsar ephemeris period in seconds, can determine the phase bin number, the bank, the CMD, the HW_IT, the LTA_IT, and the time of the Dump Trigger. This algorithm, if applied on all Station Boards that are part of the experiment, will result in the correct sequencing of DUMPTRIGs, all synchronized to the pulsar. This algorithm must be developed with the knowledge that during the current 10 msec interrupt service routine, we must determine what happens for the next 10 msecs of time, where "what happens" means knowing what CMD sequences are transmitted, and when Dump Trigger pulses occur.


Pulsar pulse train
T_P
Nbin = 8
t_{DT0}
t_{DT1}
t_{DT2}
t_{calc3}
time
t_{TC}
Phase bin: 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6
t_{pulsar}
T_{bin}
t_{bank}
$CMD_{interval}$ = 0
$CMD_{interval}$ = 1
$CMD_{interval}$ = 2
CMD=FDS
CMD=AFS
CMD=LDS
BANK 0
BANK 1
T_p x Bins_to_add
T_p x Bins_to_add x 2
S/W ISR builds HEDS
for next 10 msec period
10 ms tick
TIMECODE

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Phase binning and recirculation

- Almost too painful to contemplate.

- Lose “recirculation factor” number of Phase bins
  - E.g. if recirculation factor is 4, then there are 1000/4=250 phase bins available.
  - “number of places to put data in LTA” is always constant.
  - Left as an exercise for the reader to develop the S/W algorithm to implement.

CMD	Time	Phase bin	Bank	Action
DD	*0*	*X*	*X*	*Dump/discard. Clears corr chip accumulators. Resets recirc block counter.*
FDS	250 μs	0	0	First dump bin 0 – recirc block 0
FDS	500 μs	0	0	First dump bin 0 – recirc block 1
FDS	750 μs	0	0	First dump bin 0 – recirc block 2
FDS	1.0 ms	0	0	First dump bin 0 – recirc block 3
RRC	*1.0 ms*	*X*	*X*	*Force reset of recirc block counter*
FDS	1.25 ms	1	0	First dump bin 1 – recirc block 0
FDS	1.5 ms	1	0	First dump bin 1 – recirc block 1
FDS	1.75 ms	1	0	First dump bin 1 – recirc block 2
FDS	2.0 ms	1	0	First dump bin 1 – recirc block 3
RRC	*2.0 ms*	*X*	*X*	*Force reset of recirc block counter*
FDS	2.25 ms	2	0	First dump bin 2 – recirc block 0
FDS	2.5 ms	2	0	First dump bin 2 – recirc block 1
FDS	2.75 ms	2	0	First dump bin 2 – recirc block 2
FDS	3.0 ms	2	0	First dump bin 2 – recirc block 3
RRC	*3.0 ms*	*X*	*X*	*Force reset of recirc block counter*
LDS	3.25 ms	0	0	Add to LTA bin 0 – recirc block 0
LDS	3.5 ms	0	0	Add to LTA bin 0 – recirc block 1
LDS	3.75 ms	0	0	Add to LTA bin 0 – recirc block 2
LDS	4.0 ms	0	0	Add to LTA bin 0 – recirc block 3
RRC	*4.0 ms*	*X*	*X*	*Force reset of recirc block counter*
…	…	…	…	…

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Burst Dumping

- Used when integration time is too small to allow for contiguous data capture.

- 3 ways of doing it:
  - Explicit control and synchronization of DUMPTRIG.
  - Explicit control of LTA's burst-mode.
  - Implicit—let rate at which GigE chip can transmit data to Backend automatically control bursts.
    - LTA fills up…priority naturally transfers to LTA-to-GigE data transfer.
    - What data acquired for what baselines at what time is indeterminate.

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DUMPTRIG Synchronization

- Important for recirculation to ensure X/Y memory offset pointers correct.

- Correlator Chip XSTATUS, YSTATUS, and DESSR registers indicate if X/Y dump pulses not synchronized.
  - If not, it means that the lags being acquired for a particular lag block are indeterminate.

DUMPTRIG HES Example

Cmd	Width	Data	#bits @ 128 Mbps	#bits (elapsed)	Description
TRIG	n/a	n/a	2	2	Dump Trigger @ TIMECODE T-bit
NOP	Count=9		20	22	Preamble
SBIT	n/a	n/a	3	25	Start bit '100' output
FOD	010	0x00	3	28	CMD=000; First dump.
FOD	111	0x01	8	36	DLEN=1
FOD	011	0x00	4	40	TID=0
FOD	111	0x23	8	48	SID=0x23
FOD	100	0xFF	5	53	BB0=0xFF; **all** basebands
FOD	100	0xFF	5	58	SB0=0xFF; **all** sub-bands
FOD	111	0x80	8	66	Phase Bin MSByte=0, Bank=1
FOD	111	0x03	8	74	Phase Bin LSByte=3
CRC	n/a	na/	4	78	CRC-4 code
NOP	Count=31959		63920	63998	Preamble Fill
TRIG	n/a	na/	2	64000	Dump Trigger at t=500.0 μsec
Repeat above, CMD=001			63998	127998	Dump Trigger at t≅1.0 msec
Repeat 18 more times. Last CMD=010.					
END	n/a	n/a	na/		End of script
TRIG	n/a	n/a	n/a		Dump Trigger @ TIMECODE T-bit
Other Commands for other frames.					

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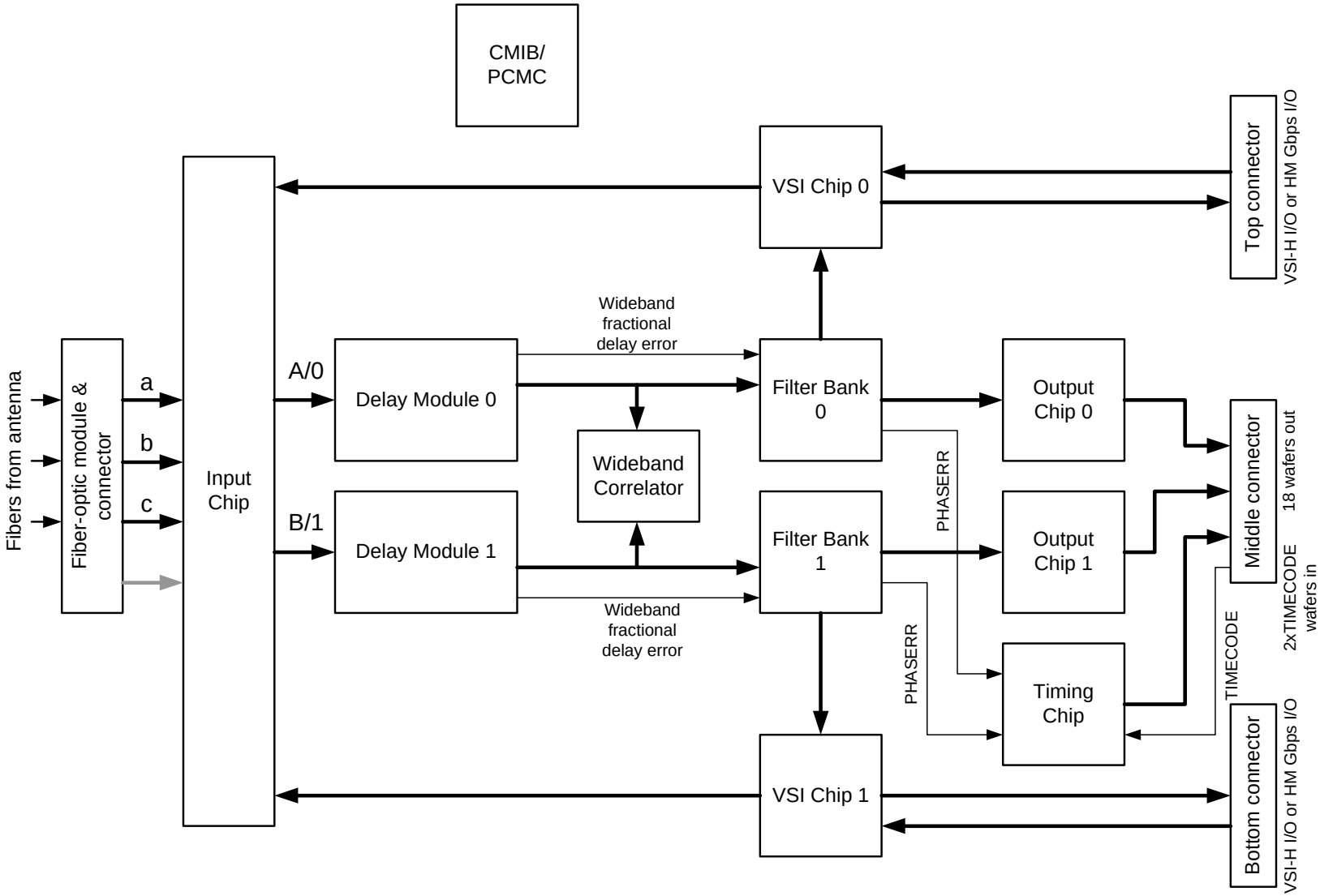
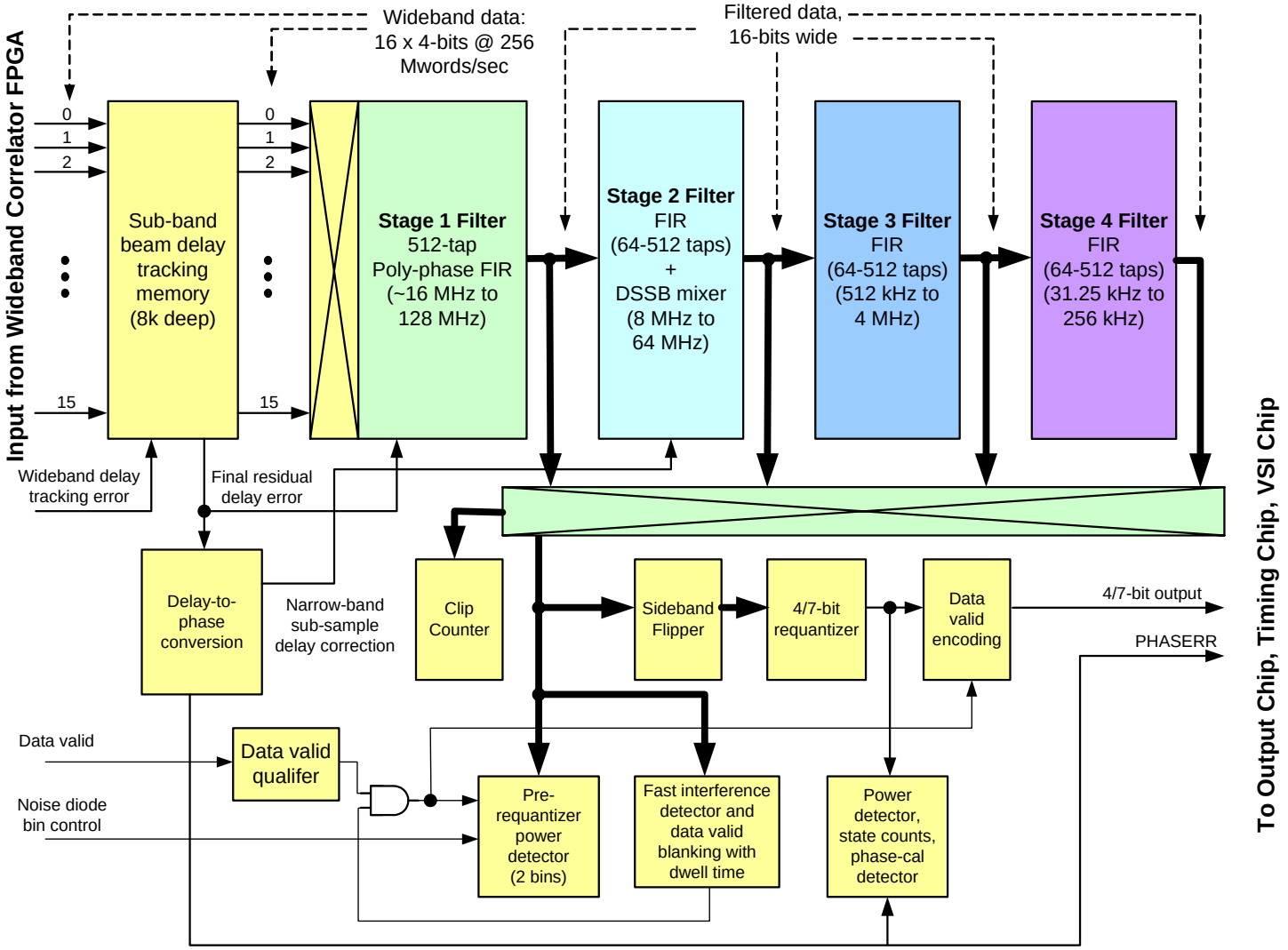
Station Board

- Overall functional description.
- Descriptions of chip functions from S/W perspective.
- Some blanks need to be filled in as some FPGA designs need upgrade or are in flux.
- References to documentation…


CMIB/
PCMC
VSI Chip 0
Top connector
VSI-H I/O or HM Gbps I/O
Wideband
fractional
delay error
Fibers from antenna
Fiber-optic module &
connector
a
b
c
Input
Chip
A/0
B/1
Delay Module 0
Delay Module 1
Wideband
Correlator
Filter Bank
0
Filter Bank
1
Output
Chip 0
Output
Chip 1
PHASERR
PHASERR
Middle connector
18 wafers out
2xTIMECODE
wafers in
TIMECODE
Timing
Chip
Wideband
fractional
delay error
VSI Chip 1
Bottom connector
VSI-H I/O or HM Gbps I/O


Wideband data:
16 x 4-bits @ 256
Mwords/sec
Filtered data,
16-bits wide
Input from Wideband Correlator FPGA
0
1
2
15
Sub-band
beam delay
tracking
memory
(8k deep)
Stage 1 Filter
512-tap
Poly-phase FIR
(~16 MHz to
128 MHz)
Stage 2 Filter
FIR
(64-512 taps)
+
DSSB mixer
(8 MHz to
64 MHz)
Stage 3 Filter
FIR
(64-512 taps)
(512 kHz to
4 MHz)
Stage 4 Filter
FIR
(64-512 taps)
(31.25 kHz to
256 kHz)
Wideband delay
tracking error
Final residual
delay error
Delay-to-
phase
conversion
Narrow-band
sub-sample
delay correction
Clip
Counter
Sideband
Flipper
4/7-bit
requantizer
Data
valid
encoding
4/7-bit output
PHASERR
Data valid
Data valid
qualifer
Noise diode
bin control
Pre-
requantizer
power
detector
(2 bins)
Fast interference
detector and
data valid
blanking with
dwell time
Power
detector,
state counts,
phase-cal
detector
To Output Chip, Timing Chip, VSI Chip

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Station Board Data Products

- Wideband state counts.
- Wideband correlation lags.
- 16-bit stage output clip counter.
- Pre-re-quantizer power measurement.
- Re-quantizer state counts.
- Re-quantizer power.
- Re-quantizer clip counter.
- Tone extractor I&Q.
- RFI blanker counter.
- Radar-mode data capture.

Station Board miscl

- Memory map.
- PCMC
  - Processor boot, PCI devices, absolute memory addresses.
  - FPGA programming (“personality” programming). Byte-wide.
  - A/D readings for V + T monitor.
  - 10 msec interrupt.

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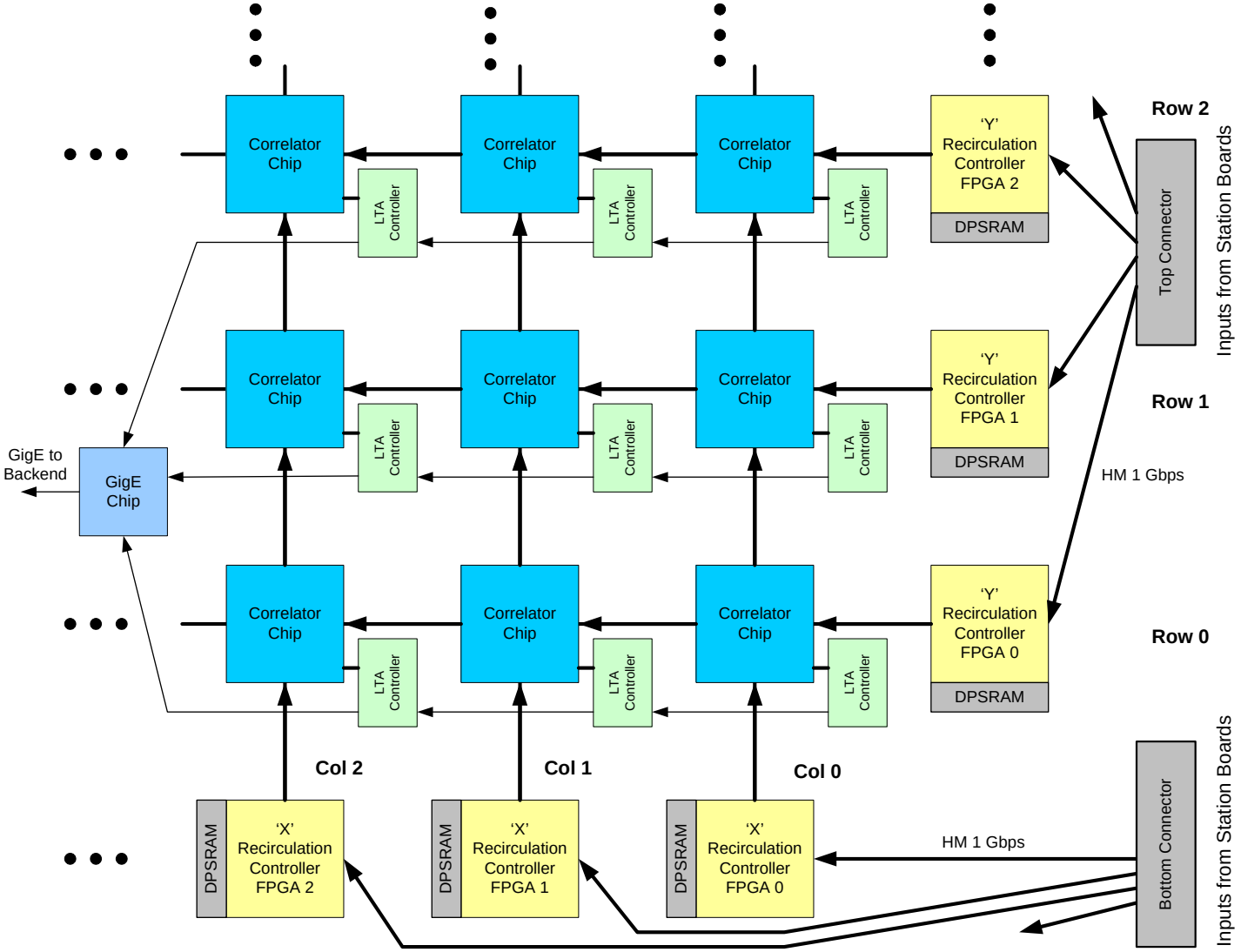
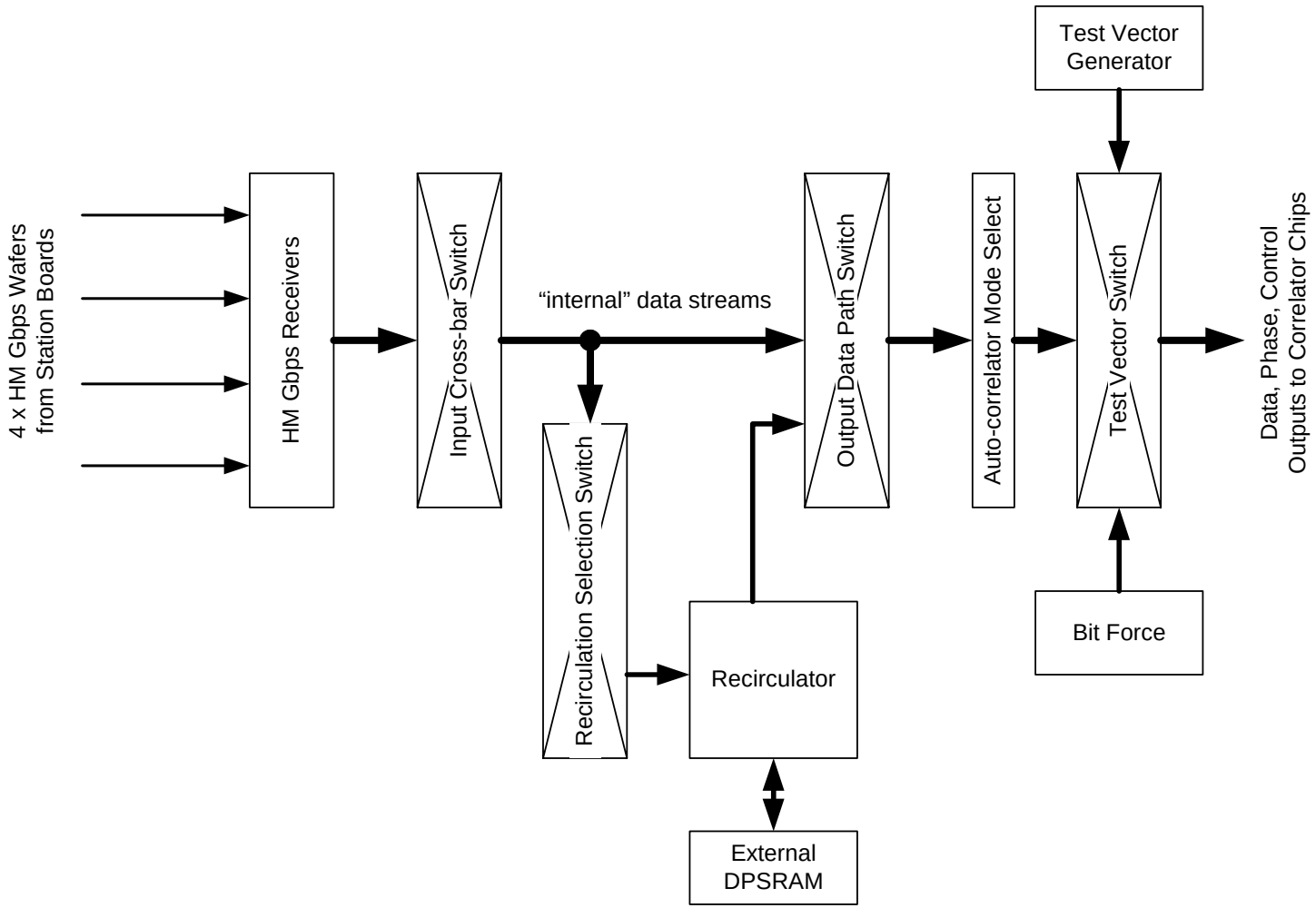
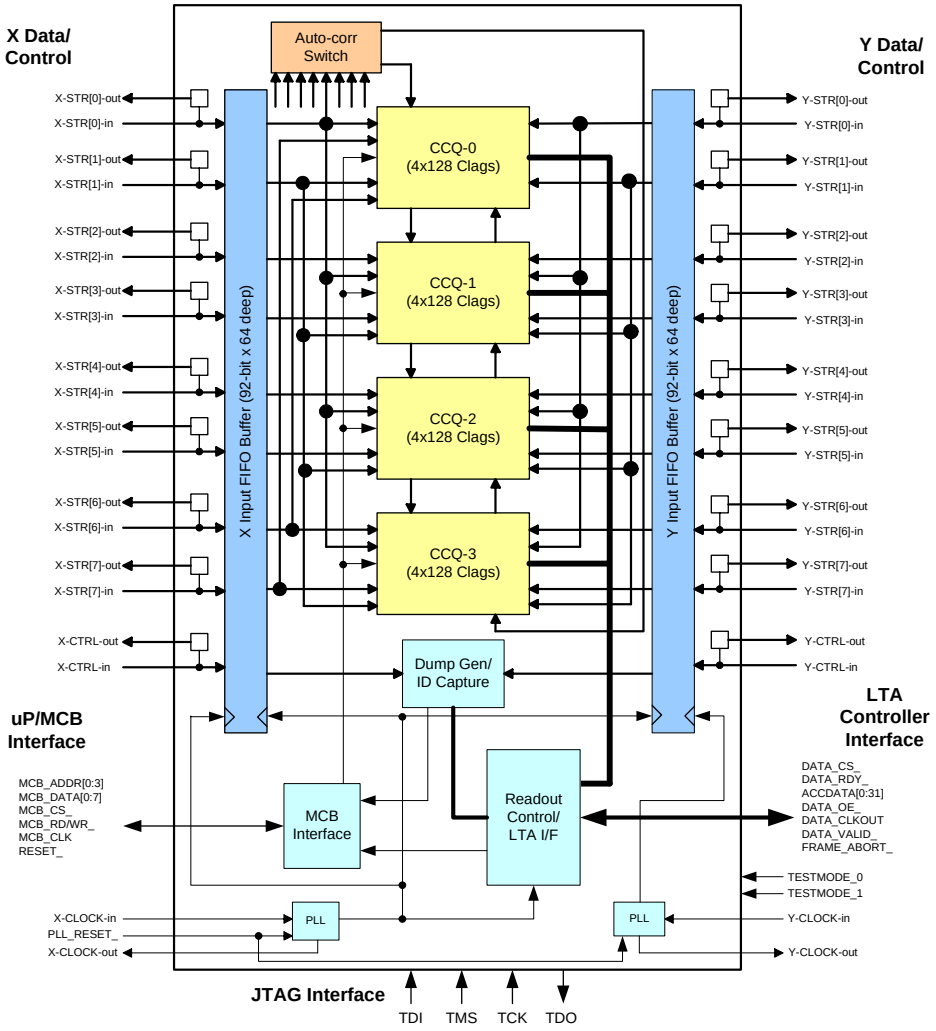
Baseline Board

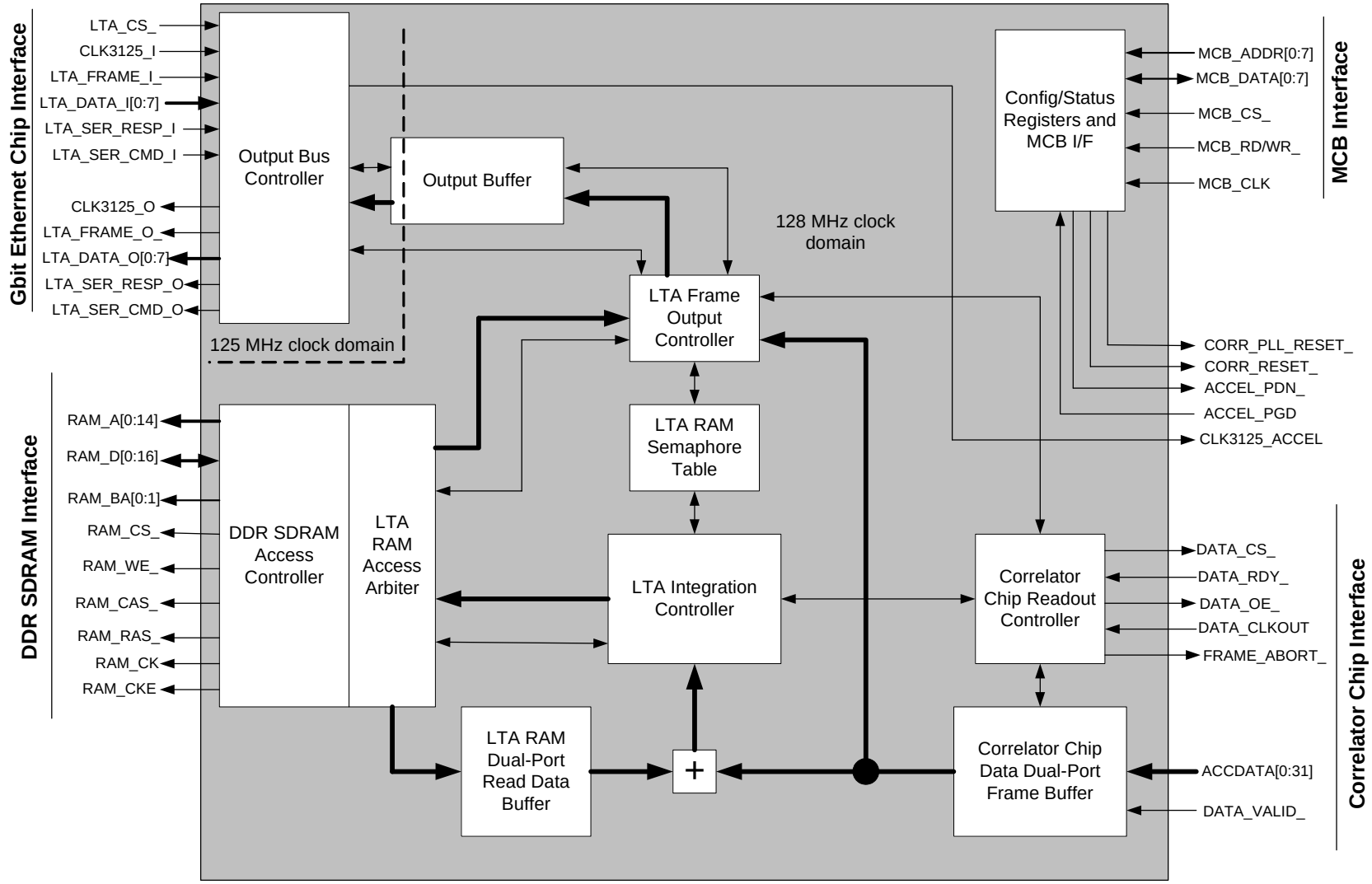
- Overall description.
- Important points of note for each chip…details refer to RFS docs.
- Mostly configuration and monitor. Relatively little real-time S/W.

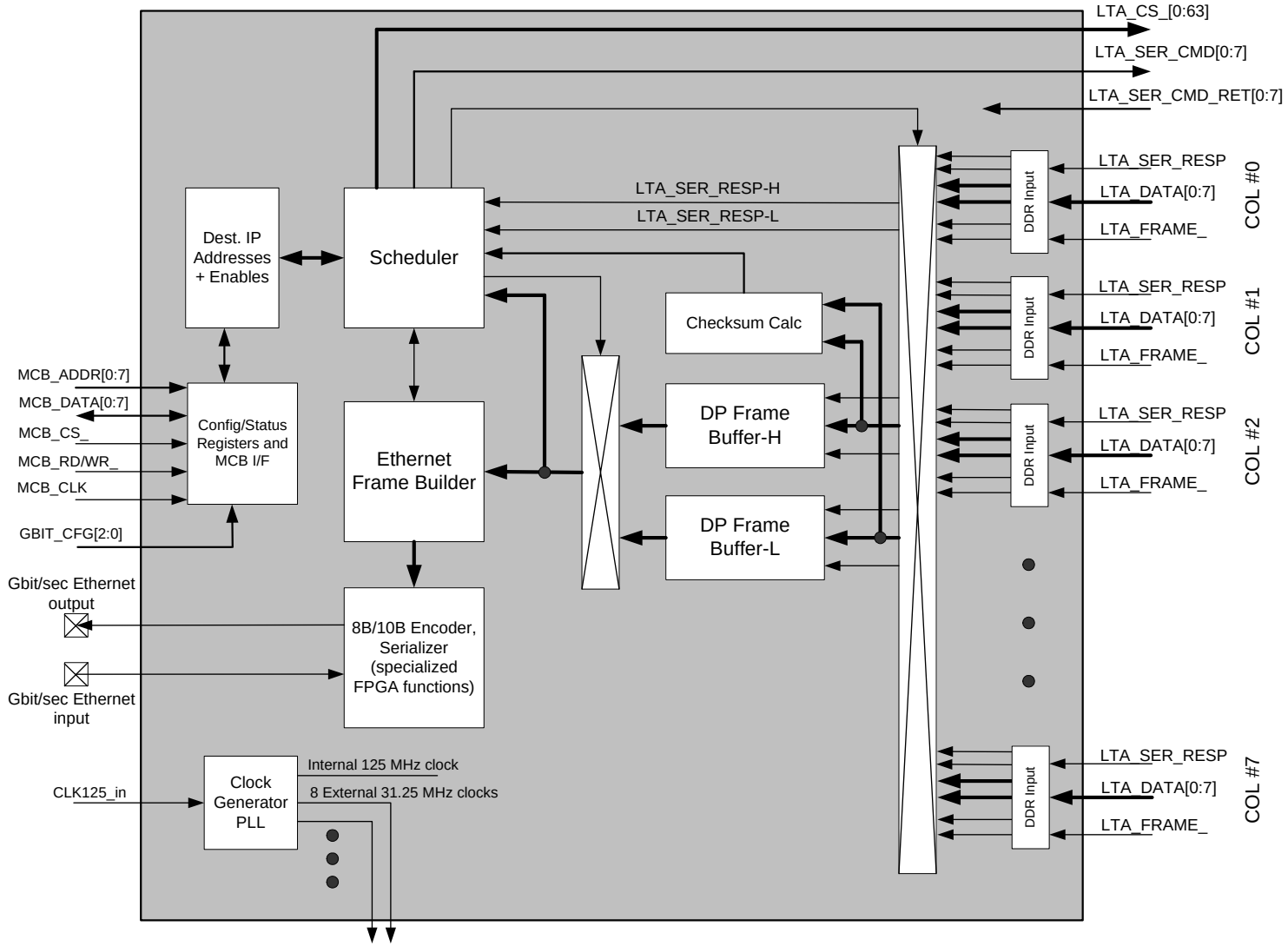

Correlator Chip
LTA Controller
'Y' Recirculation Controller FPGA 2
'Y' Recirculation Controller FPGA 1
'Y' Recirculation Controller FPGA 0
DPSRAM
Row 2
Row 1
Row 0
Top Connector
Inputs from Station Boards
HM 1 Gbps
GigE to Backend
GigE Chip
Col 2
Col 1
Col 0
'X' Recirculation Controller FPGA 2
'X' Recirculation Controller FPGA 1
'X' Recirculation Controller FPGA 0
HM 1 Gbps
Bottom Connector
Inputs from Station Boards


Test Vector Generator
4 x HM Gbps Wafers from Station Boards
HM Gbps Receivers
Input Cross-bar Switch
"internal" data streams
Output Data Path Switch
Auto-correlator Mode Select
Test Vector Switch
Data, Phase, Control Outputs to Correlator Chips
Recirculation Selection Switch
Recirculator
Bit Force
External DPSRAM

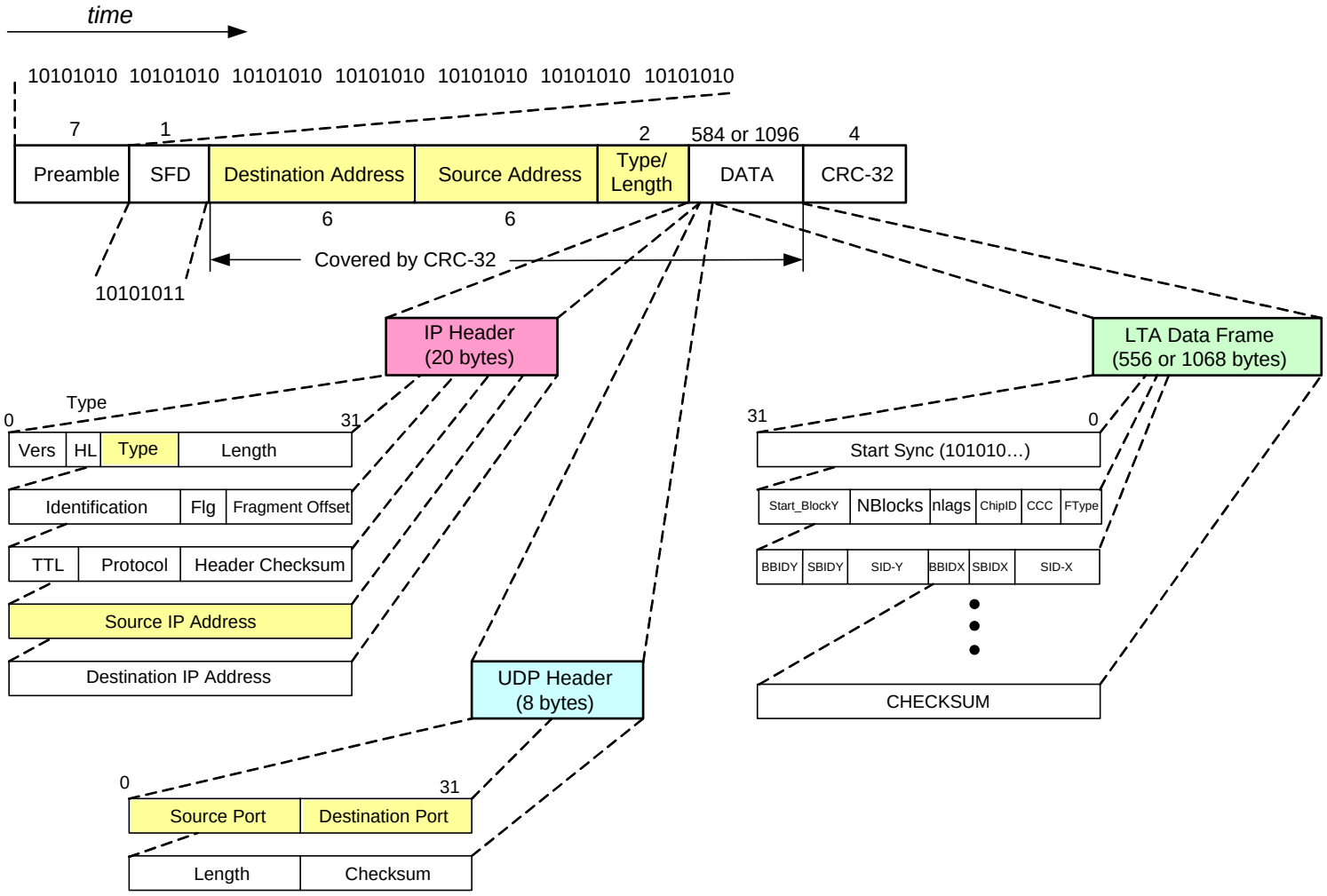
Simplified Correlator Chip Block Diagram




Gbit Ethernet Chip Interface
LTA_CS_
CLK3125_I
LTA_FRAME_I_
LTA_DATA_I[0:7]
LTA_SER_RESP_I
LTA_SER_CMD_I
CLK3125_O
LTA_FRAME_O_
LTA_DATA_O[0:7]
LTA_SER_RESP_O
LTA_SER_CMD_O
Output Bus Controller
Output Buffer
125 MHz clock domain
128 MHz clock domain
Config/Status Registers and MCB I/F
MCB_ADDR[0:7]
MCB_DATA[0:7]
MCB_CS_
MCB_RD/WR_
MCB_CLK
MCB Interface
LTA Frame Output Controller
CORR_PLL_RESET_
CORR_RESET_
ACCEL_PDN_
ACCEL_PGD
CLK3125_ACCEL
DDR SDRAM Interface
RAM_A[0:14]
RAM_D[0:16]
RAM_BA[0:1]
RAM_CS_
RAM_WE_
RAM_CAS_
RAM_RAS_
RAM_CK
RAM_CKE
DDR SDRAM Access Controller
LTA RAM Access Arbiter
LTA RAM Semaphore Table
LTA Integration Controller
Correlator Chip Readout Controller
DATA_CS_
DATA_RDY_
DATA_OE_
DATA_CLKOUT
FRAME_ABORT_
LTA RAM Dual-Port Read Data Buffer
+
Correlator Chip Data Dual-Port Frame Buffer
ACCDATA[0:31]
DATA_VALID_
Correlator Chip Interface


LTA_CS_[0:63]
LTA_SER_CMD[0:7]
LTA_SER_CMD_RET[0:7]
LTA_SER_RESP-H
LTA_SER_RESP-L
Dest. IP Addresses + Enables
Scheduler
Checksum Calc
DP Frame Buffer-H
DP Frame Buffer-L
Ethernet Frame Builder
Config/Status Registers and MCB I/F
MCB_ADDR[0:7]
MCB_DATA[0:7]
MCB_CS_
MCB_RD/WR_
MCB_CLK
GBIT_CFG[2:0]
Gbit/sec Ethernet output
Gbit/sec Ethernet input
8B/10B Encoder, Serializer (specialized FPGA functions)
CLK125_in
Clock Generator PLL
Internal 125 MHz clock
8 External 31.25 MHz clocks
DDR Input
LTA_SER_RESP
LTA_DATA[0:7]
LTA_FRAME_
COL #0
COL #1
COL #2
COL #7

IEEE 802.3 Ethernet Frame with UDP/IP and LTA Data Frame



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Baseline Board miscl

- Memory map.
- PCMC
  - Similar to Station Board (Processor boot, PCI devices).
  - FPGA programming…bit serial.
  - A/D V+T readings.
  - All Corr Chip core voltages accessed using one A/D channel and dual 32:1 analog switches. Use Recirc-Y7 to control analog switches.
  - 10 msec interrupt.
- Correlator Chip power and reset sequencing.
  - Controlled thru regs on companion LTA.
  - Power sequence, PLL reset sequence, reset sequence.

Other Boards

- Timecode Board and Phasing Board.
  - Details still to be filled in…

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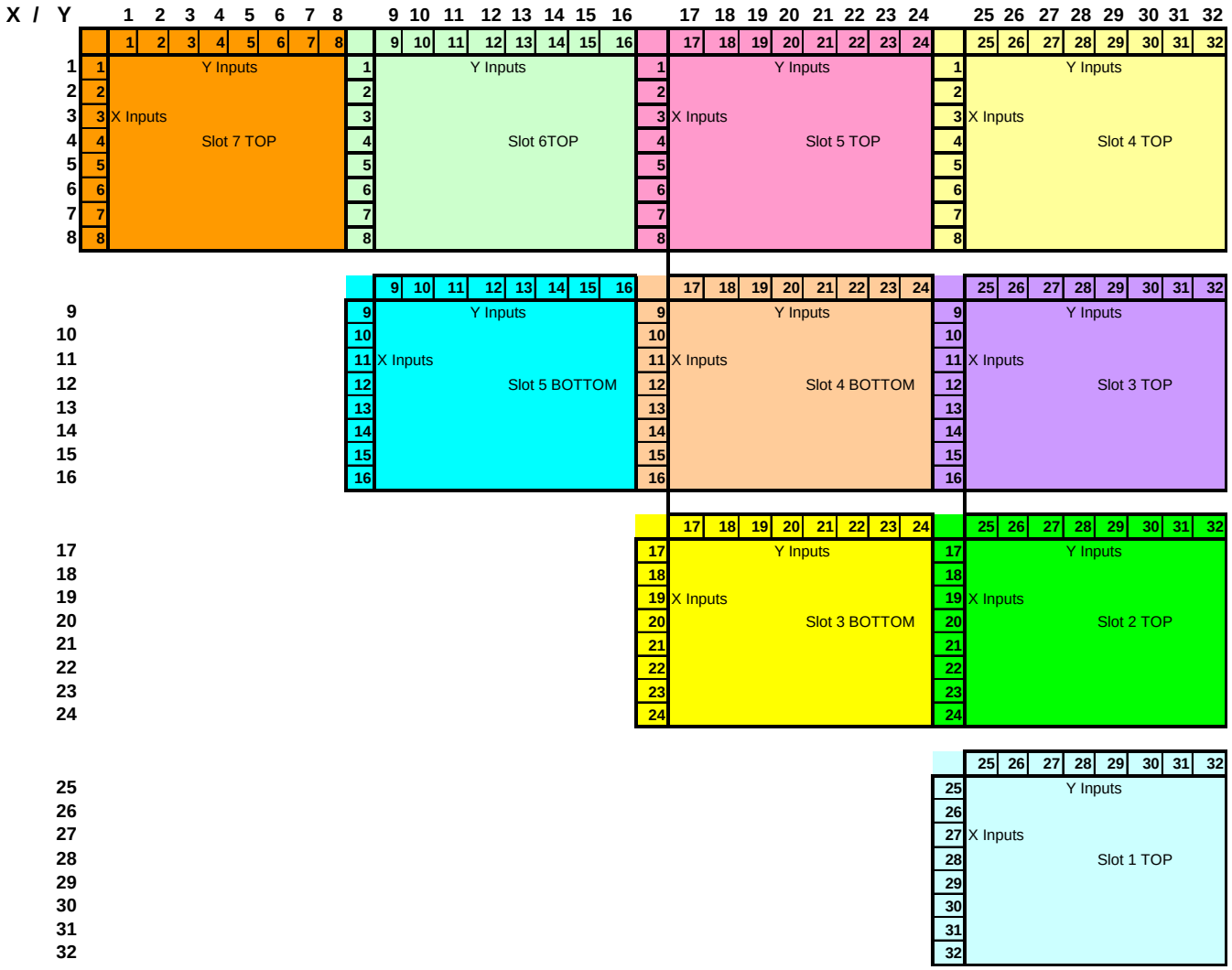
System

- Remote power monitor and control.
- M&C network.
- Baseline Board to CBE GigE switched network.
- Station-to-Baseline Board data routing.
  - Mechanical mock-up demonstrates that cable routing in Baseline rack is feasible.
- Location of Phasing Board not completely defined.
  - In Baseline racks?
  - In separate rack?
- System module numbering and identification: ICD A25010N0002.


X / Y
Y Inputs
X Inputs
Slot 7 TOP
Slot 6TOP
Slot 5 TOP
Slot 4 TOP
Slot 5 BOTTOM
Slot 4 BOTTOM
Slot 3 TOP
Slot 3 BOTTOM
Slot 2 TOP
Slot 1 TOP

Crate 0=TOP	SLOT	X-inputs	Y-inputs
0	1	25-32	25-32
0	2	17-24	25-32
0	3	9-16	25-32
0	4	1-8	25-32
0	5	1-8	17-24
0	6	1-8	9-16
0	7	1-8	1-8
1	3	17-24	17-24
1	4	9-16	17-24
1	5	9-16	9-16

Appendix I

- Copy of sub-band Stitching and Windowing from NRC-EVLA Memo# 001.
  - Important for post-Backend processing.
  - Need pre-requantizer power measurements, filter scaling factors, filter shapes for sub-band stitching. Probably needs another document to define *exactly* what numbers are needed, and what needs to be done.
  - Windowing for stitching needs more work.