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Expanded
Very Large Array

Technical Benefits and Difficulties

B. Carlson

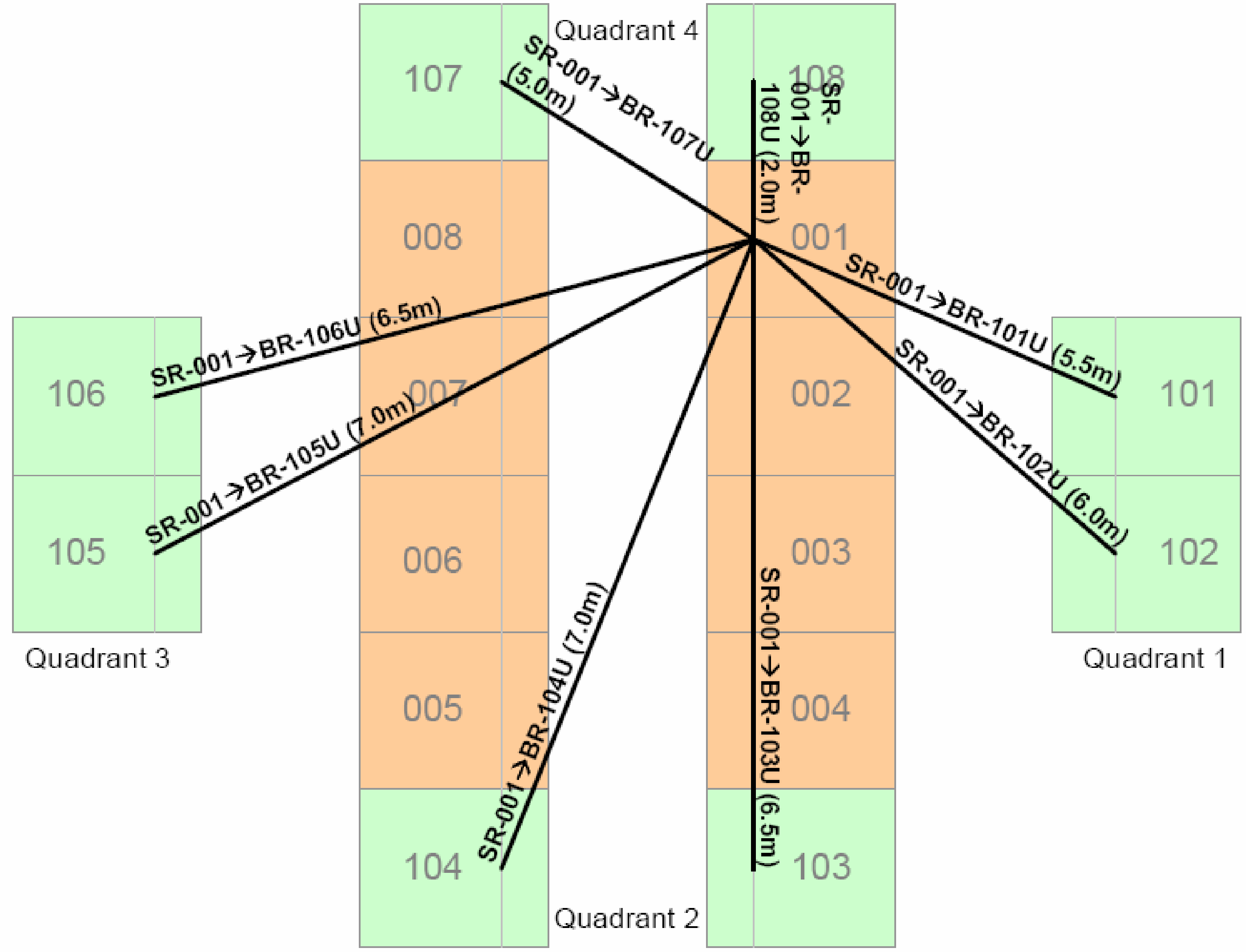
Outline

- Technical benefits.
  - Fewer Baseline Boards, racks.
  - 3X fewer hi-speed cables.
  - More logical/seamless phasing capability…all bandwidth all the time.

- Technical difficulties/uncertainties.
  - Re-timing hops.
  - Y Recirc FPGA connections for Tx or Rx (expansion).
  - Y connector out to X in via patch board.
  - DC biasing on re-timing FPGA inputs.
  - Re-timing FPGA connections; 2 x 80 lines at 512 Mbps DDR.
  - 1:2 LVDS buffers…small package…rework specialty.
  - Phasing design not yet done…logic use estimates.

Technical Benefits

- 3X fewer cables: 3X fewer cable contacts…3X more reliable.
- Vastly simpler baseline rack wiring (almost empty).
- Simpler rack-to-rack and intra-rack wiring
  - Only 64 short cables in each station rack, rather then 160 short cables in each baseline rack.
  - Rack-to-rack wiring is point-to-point…easier site installation.
- Kit with 128 bunches of 4 cables going rack-to-rack, rather than 512 individual cables.



Quadrant 4
107
108
SR-001→BR-107U (5.0m)
SR-001→BR-108U (2.0m)
008
001
SR-001→BR-101U (5.5m)
SR-001→BR-106U (6.5m)
106
007
002
101
SR-001→BR-102U (6.0m)
SR-001→BR-105U (7.0m)
105
006
003
102
Quadrant 3
Quadrant 1
SR-001→BR-104U (7.0m)
SR-001→BR-103U (6.5m)
005
004
104
103
Quadrant 2

Technical Benefits

- Maximum cable length is now 7 m…better eye at the receiving end.
- Station Board outputs have to drive only 1 m of cable. X-bar board drives long cable with high-voltage PECL drivers.
- Reduces the number of baseline racks from 16 to 8…more room in correlator room for other equipment/expansion.
- Reduces the number of Baseline Boards from 160 to 128…more reliable system.

Technical Benefits

- More logically consistent and dynamically available phasing…several options for getting data to VLBI recording equipment.
  - VLBI recording equipment can sit in racks beside baseline racks…or elsewhere, depending on interface.
  - Connect all streams into Station Board(s) that, via VSI-H output, goes to VLBI recorder (or iBob board to 10 GigE) (previous talk for details).

Technical diff/uncertainties

- Starting at the Station Board, there are 5 “hops”/re-timings of the signal before it gets to the last Recirc FPGA on the 2nd Baseline Board.
  - Low-level worry this might be a problem…you never know!
  - FPGA PLLs perform very well…currently testing 3 hops under worse conditions (longer cables between hops) than in the new scheme.
  - FPGA PLLs set for low bandwidth, max jitter rejection. 128 MHz clock jitter accumulation low compared to 1 Gbps anyway.
  - Backup plan:
    - Provide external clock input to each Station and Baseline Board via blind-mate SMA connector at the rear of the board.
    - If clock jitter becomes a problem when the whole system is together, could reasonably easily add external clock network by adding SMA bulkheads, splitter, amplifier…take more work to make it fault-tolerant redundant (that’s why we dropped doing this in the first place).

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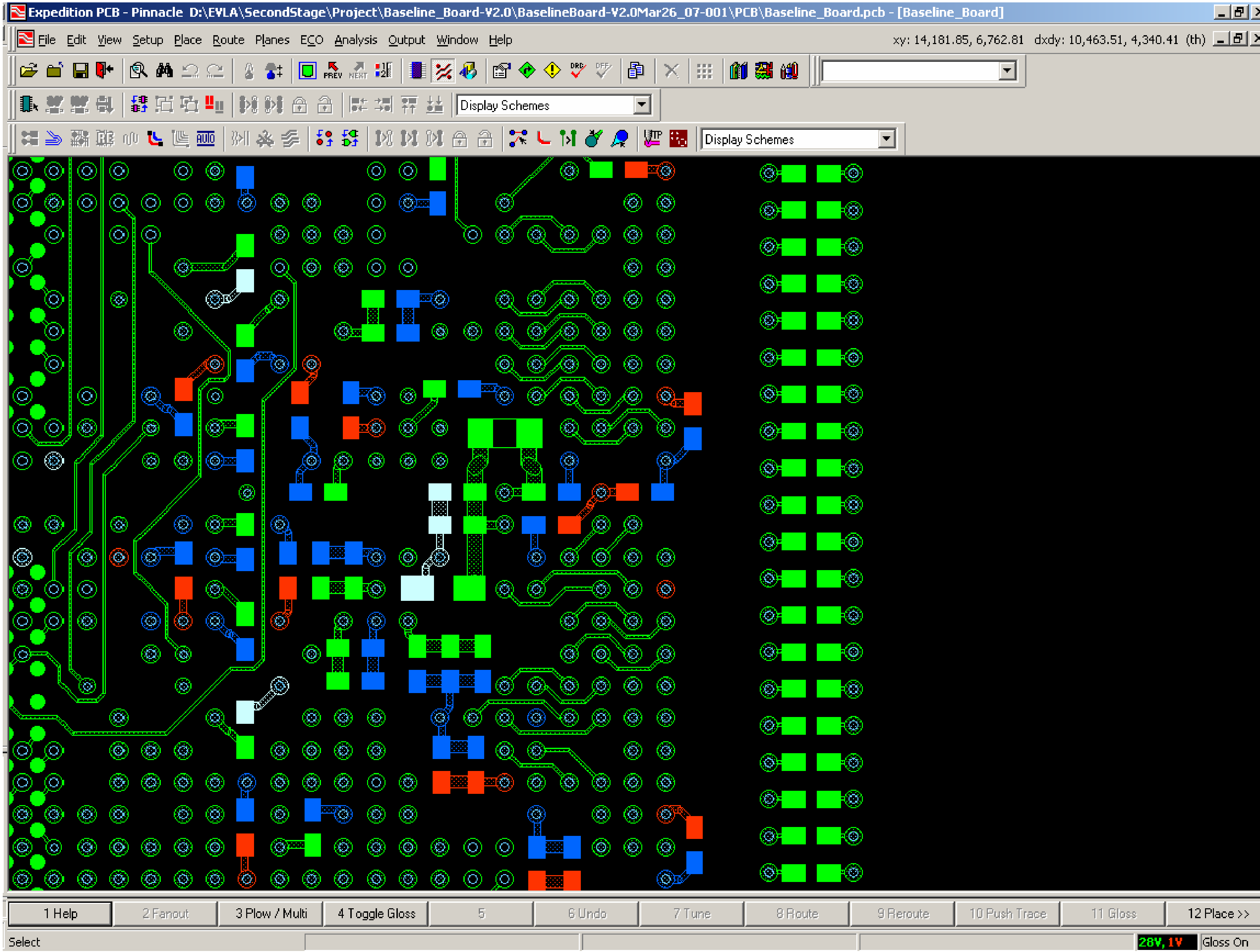
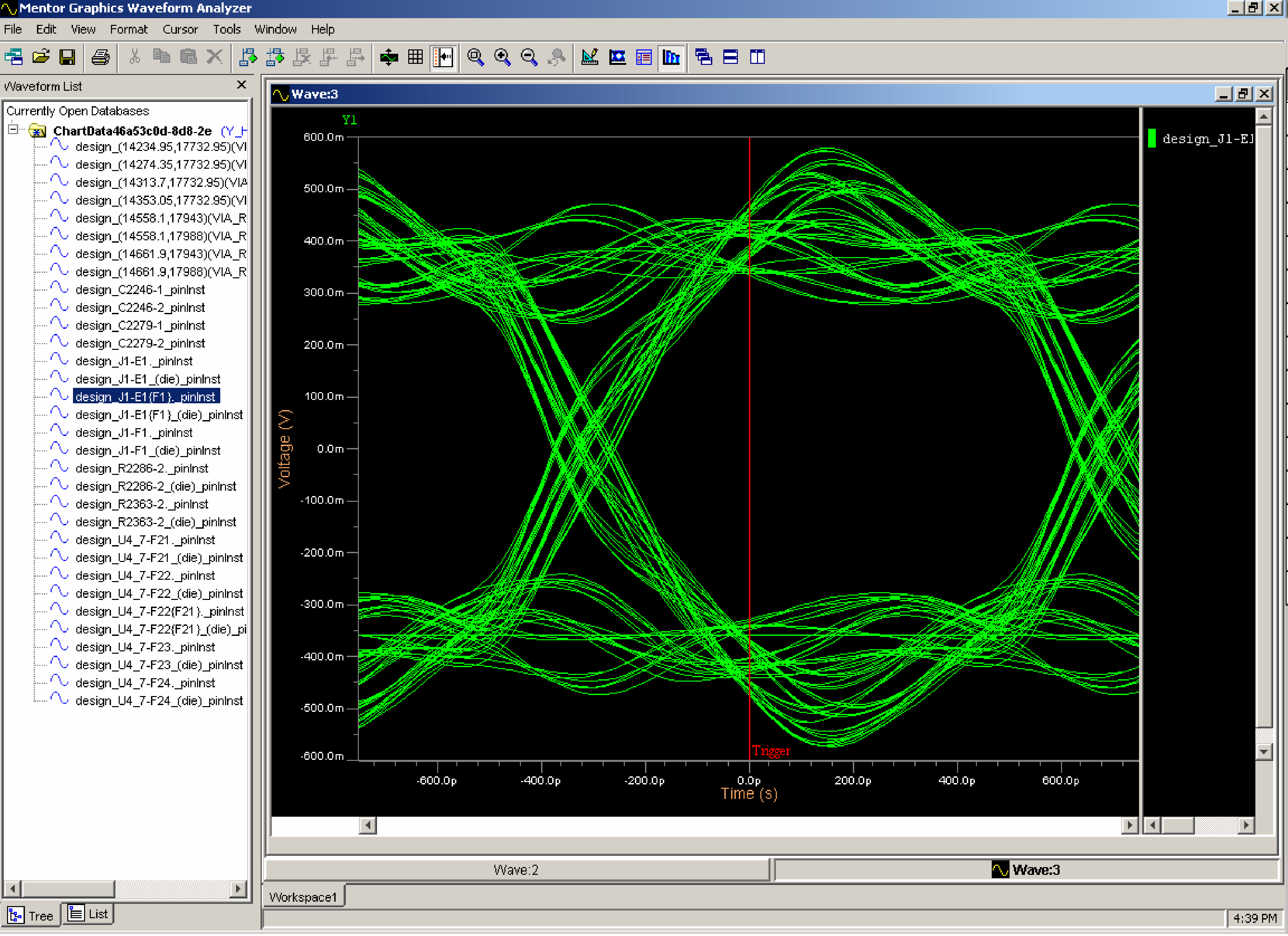
Technical diff/uncertainties

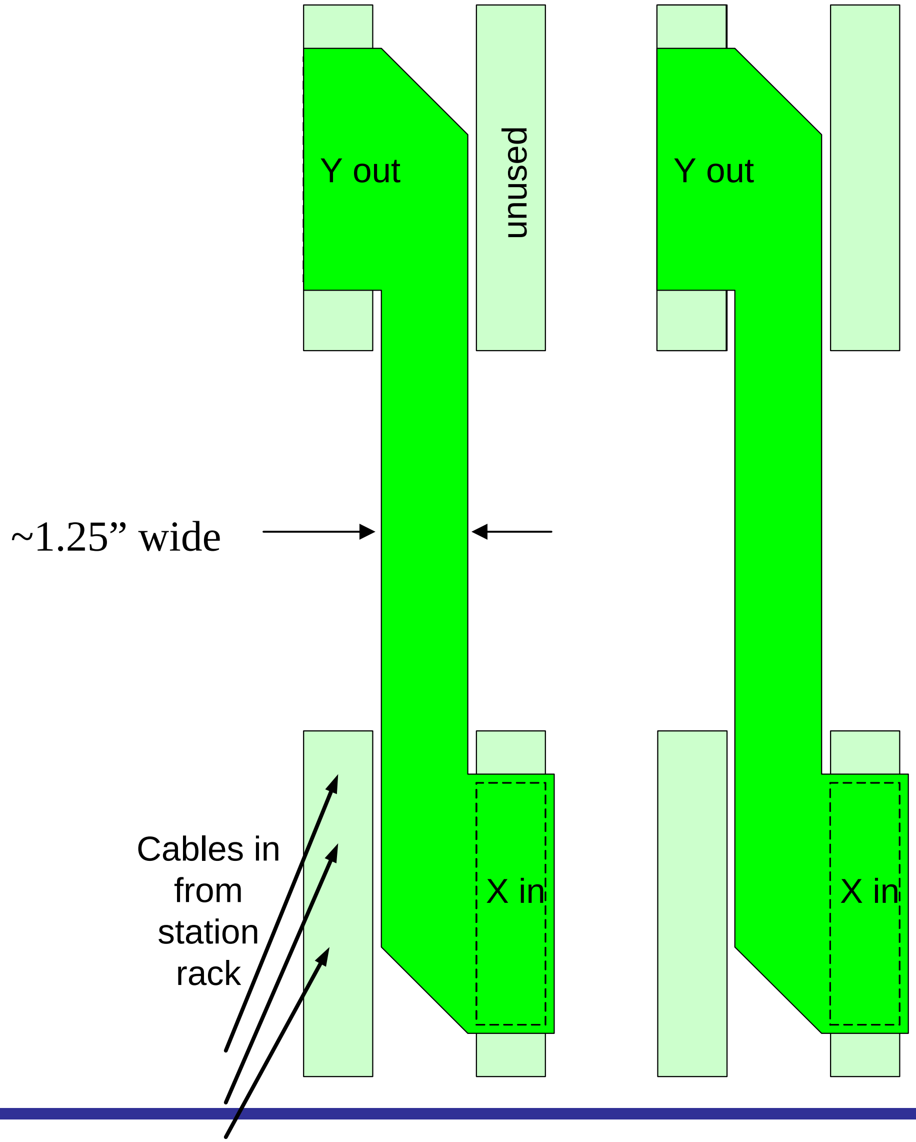
- The Y Recirc FPGAs have 1 Gbps Tx and Rx pins tied together on the outer layer of the PCB to allow for expansion:
  - Normally operate as a transmitter…so the Rx pins to Hi-z receiver in the FPGA are a stub (~1", including PCB, FPGA ~350 psec RT)
  - When operated as a receiver (expansion), the Tx pins to Hi-z transmitter in the FPGA are a stub (~0.5", including PCB, FPGA ~175 psec RT)
  - Could be signal integrity problem (round-trip is ~350 psec).
  - Signal integrity on routed board with IS_analyzer...
  - If a problem, 1 board will work anyway; could cut traces to make 2 boards work…replace Tx/Rx connections with 0201 resistor pads in next proto round if necessary. Install resistors to use receivers for expansion.


Expedition PCB - Pinnacle D:\EVLA\SecondStage\Project\Baseline_Board-V2.0\BaselineBoard-V2.0Mar26_07-001\PCB\Baseline_Board.pcb - [Baseline_Board]
File Edit View Setup Place Route Planes ECO Analysis Output Window Help
xy: 14,181.85, 6,762.81 dxdy: 10,463.51, 4,340.41 (th)
Display Schemes
Display Schemes
1 Help
2 Fanout
3 Plow / Multi
4 Toggle Gloss
5
6 Undo
7 Tune
8 Route
9 Reroute
10 Push Trace
11 Gloss
12 Place >>
Select
28V, 1V
Gloss On


Mentor Graphics Waveform Analyzer
File Edit View Format Cursor Tools Window Help
Waveform List
Currently Open Databases
ChartData46a53c0d-8d8-2e
design_(14234.95,17732.95)(VI
design_(14274.35,17732.95)(VI
design_(14313.7,17732.95)(VIA
design_(14353.05,17732.95)(VI
design_(14558.1,17943)(VIA_R
design_(14558.1,17988)(VIA_R
design_(14661.9,17943)(VIA_R
design_(14661.9,17988)(VIA_R
design_C2246-1_pinInst
design_C2246-2_pinInst
design_C2279-1_pinInst
design_C2279-2_pinInst
design_J1-E1._pinInst
design_J1-E1_(die)_pinInst
design_J1-E1{F1}._pinInst
design_J1-E1{F1}_(die)_pinInst
design_J1-F1._pinInst
design_J1-F1_(die)_pinInst
design_R2286-2._pinInst
design_R2286-2_(die)_pinInst
design_R2363-2._pinInst
design_R2363-2_(die)_pinInst
design_U4_7-F21._pinInst
design_U4_7-F21_(die)_pinInst
design_U4_7-F22._pinInst
design_U4_7-F22_(die)_pinInst
design_U4_7-F22{F21}._pinInst
design_U4_7-F22{F21}_(die)_pi
design_U4_7-F23._pinInst
design_U4_7-F23_(die)_pinInst
design_U4_7-F24._pinInst
design_U4_7-F24_(die)_pinInst
Tree
List
Wave:3
Y1
600.0m
500.0m
400.0m
300.0m
200.0m
100.0m
0.0m
-100.0m
-200.0m
-300.0m
-400.0m
-500.0m
-600.0m
Voltage (V)
Trigger
-600.0p
-400.0p
-200.0p
0.0p
200.0p
400.0p
600.0p
Time (s)
design_J1-E1
Wave:2
Wave:3
Workspace1
4:39 PM

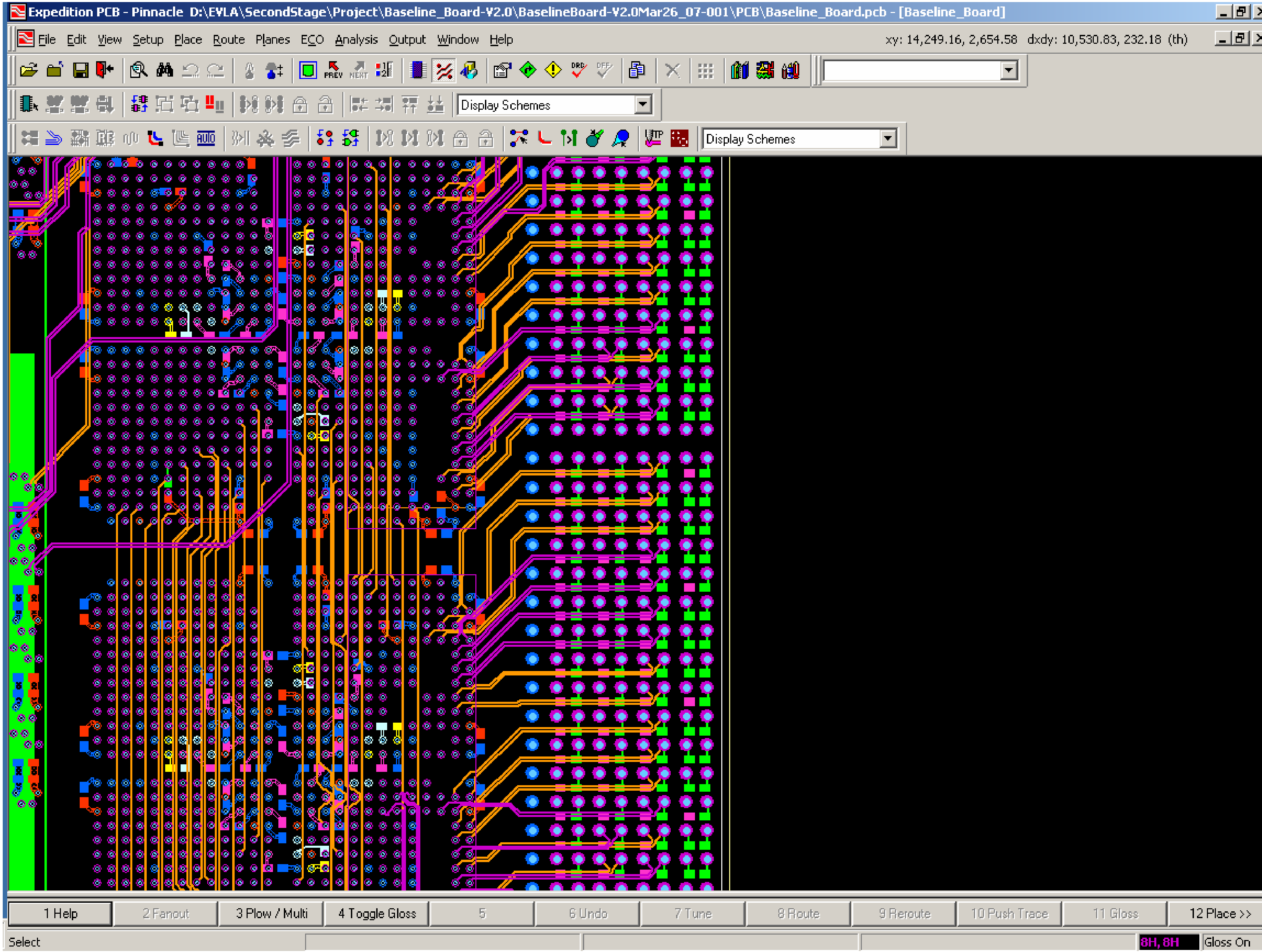
Technical diff/uncertainties

- Y connector out to X in (next board) via patch board.
  - Plugs into the Y connector and the X connector of the next board.
  - Routes 1 Gbps LVDS signals from Y Recirc FPGAs to next board's re-timing FPGAs max ~19" FR-4 + 2 connectors.
  - Use "HyperTransport" output, ~1.6X the output voltage swing (1.2 V differential). Compatible with LVDS on the input.
  - Worst case, replace with cable (~8X cost), or better PCB material (?? cost). Use largest traces possible. Use equalization on patch board?
  - 28 layers, 14 routing, 14 GND, 128 diff pairs, ~10 diff pairs per layer…should be ok.
  - Y7 output routed to X0 input…reorganize with the re-timing FPGA X-bar switch.


Y out
unused
Y out
~1.25" wide
X in
X in
Cables in
from
station
rack

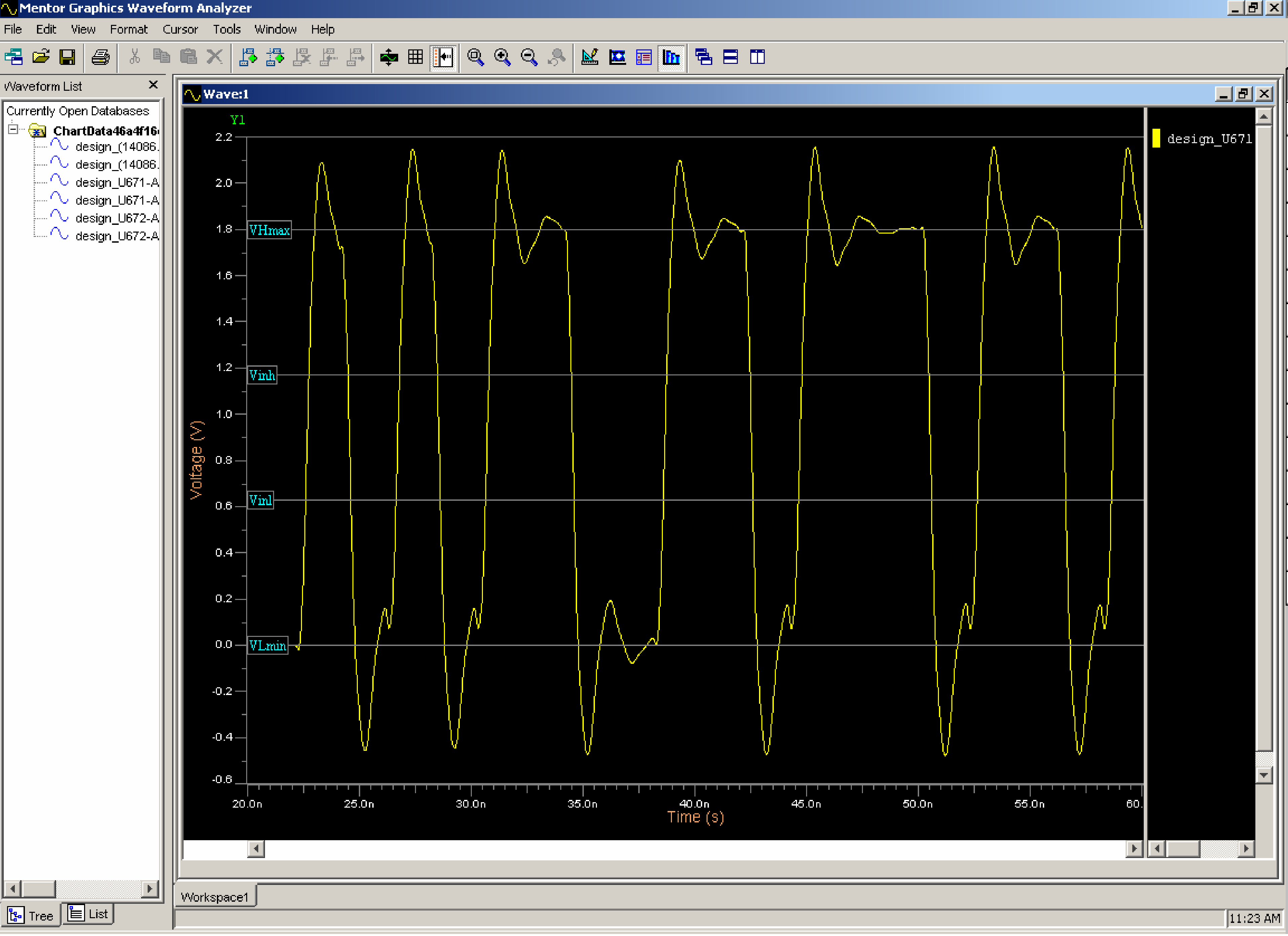
Technical diff/uncertainties

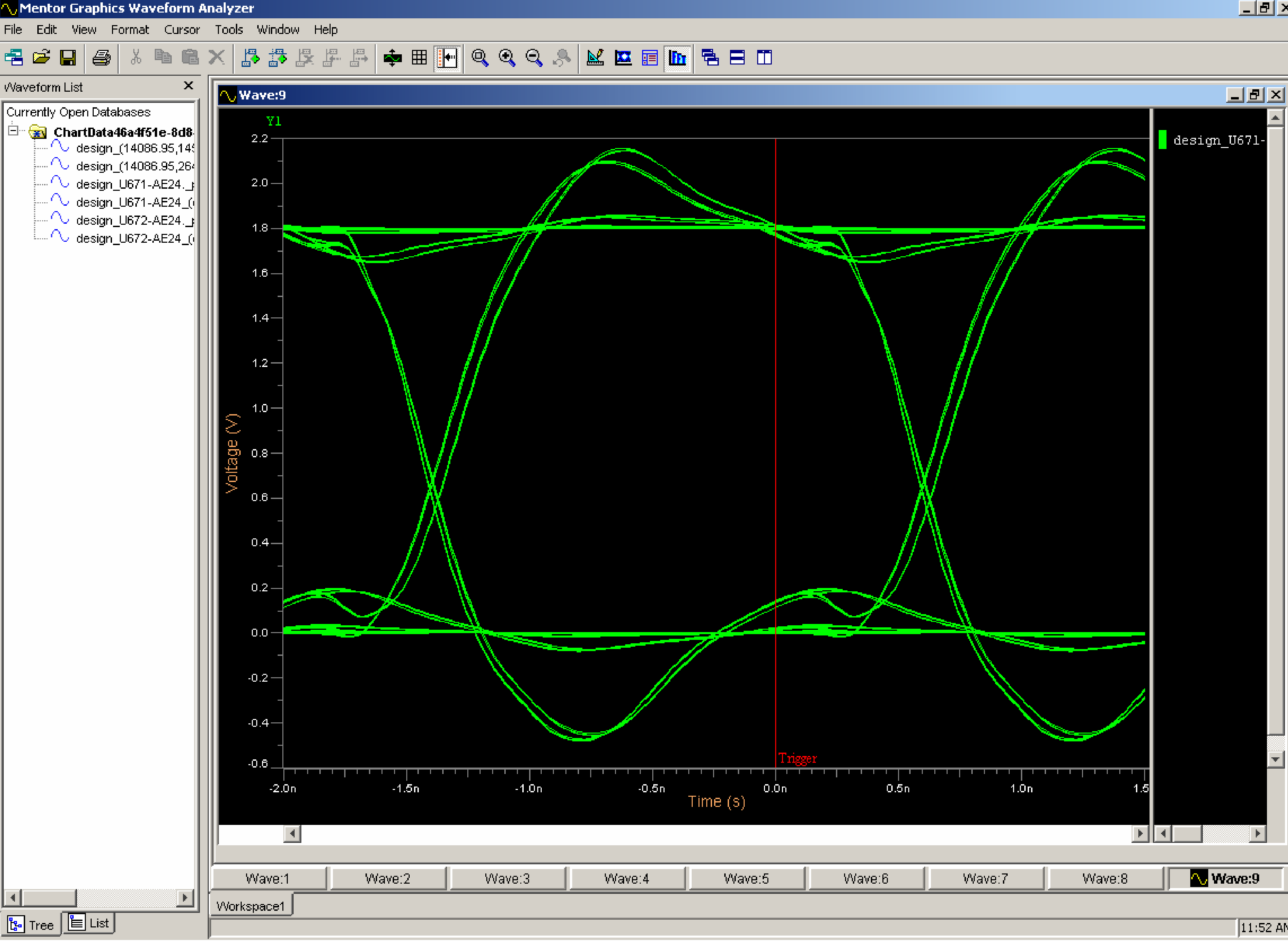
- All 1 Gbps transmitters that drive cable are AC-coupled.
- Using on-chip differential termination in the BB re-timing FPGA requires bias to be re-established.
- Can fit only *one* 10 k bias resistor per diff pair on the board…under the connector GND shield.
  - Existing Fanout Board had no bias resistor and works ok…although Altera recommends a DC bias. DC leakage input current is 10 μA.
  - Will test one bias resistor with the existing Fanout Board.
  - If necessary, could put other bias resistor on the X-bar board (at the other end of the cable).


Expedition PCB - Pinnacle D:\EVLA\SecondStage\Project\Baseline_Board-V2.0\BaselineBoard-V2.0Mar26_07-001\PCB\Baseline_Board.pcb - [Baseline_Board]
File Edit View Setup Place Route Planes ECO Analysis Output Window Help
xy: 14,249.16, 2,654.58 dxdy: 10,530.83, 232.18 (th)
Display Schemes
Display Schemes
1 Help
2 Fanout
3 Plow / Multi
4 Toggle Gloss
5
6 Undo
7 Tune
8 Route
9 Reroute
10 Push Trace
11 Gloss
12 Place >>
Select
8H, 8H
Gloss On

Technical diff/uncertainties

- Between the re-timing FPGAs on the Baseline Board, there are 80 lines going each direction to allow full cross-bar functionality for sub-arrays.
- Each line is 512 Mbps DDR. Lines are short…max ~1.2”.
- 1.8 V I/O standard (0.9 V swing)…with 11 pF load (5 pF input, 3.5 pF/in trace capacitance), the FPGA tool says it will work with 10 mA driver (522 Mbps); with 12 mA driver can do 614 Mbps.


Mentor Graphics Waveform Analyzer
File Edit View Format Cursor Tools Window Help
Waveform List
Currently Open Databases
ChartData46a4f16
design_(14086.
design_(14086.
design_U671-A
design_U671-A
design_U672-A
design_U672-A
Wave:1
Y1
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Voltage (V)
VHmax
Vinh
Vinl
VLmin
20.0n
25.0n
30.0n
35.0n
40.0n
45.0n
50.0n
55.0n
60.
Time (s)
design_U671
Workspace1
Tree
List
11:23 AM


Mentor Graphics Waveform Analyzer
File Edit View Format Cursor Tools Window Help
Waveform List
Currently Open Databases
ChartData46a4f51e-8d8
design_(14086.95,14
design_(14086.95,26
design_U671-AE24._
design_U671-AE24_(
design_U672-AE24._
design_U672-AE24_(
Wave:9
Y1
Voltage (V)
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Trigger
-2.0n
-1.5n
-1.0n
-0.5n
0.0n
0.5n
1.0n
1.5
Time (s)
design_U671-
Wave:1
Wave:2
Wave:3
Wave:4
Wave:5
Wave:6
Wave:7
Wave:8
Wave:9
Workspace1
Tree
List
11:52 AM

Technical diff/uncertainties

- 1:2 LVDS fanout buffers after the re-timing FPGAs are in 2 mm x 2 mm package.
- Re-work requires special techniques…use the BGA rework machine, but not the pickup nozzle.
- Requires some additional learning…need to operate the BGA reflow head in manual mode…needs investigation/training.

Technical diff/uncertainties

- Phasing design and PAR not complete yet.
- Estimates (per single-stream phased output):
  - Sync + phase gen: ~300 LEs/station = 9600 LEs
  - 8-bit complex phase rotation: 64 x 256 x 8-bit ROMs = 131k bits.
  - 64 8-bit complex multipliers: 64 dedicated 9-bit multipliers.
  - 32 x 8-bit complex adder tree: 62 x ~10-bit adders: 700 LEs.
  - 128-tap, 8-bit Hilbert transform:
    - 128 x 8-bit SRs: 1024 LEs.
    - 128 tap coeff mult: 32, 8-bit adders (256 LEs), 32 9-bit multipliers.
    - 32 x 9-bit coeff regs: 288 LEs; 31 x ~12-bit adders = 372 LEs
    - Re-quantization LUT: 2048 x 8-bit = 16384 RAM bits

Technical diff/uncertainties

- Single-stream phasing estimates (1 phased output):
  - 12,224 LEs, 96 x 9-bit multipliers, 200k RAM bits.
- The re-timing/Xbar requires 12k LEs, 0 RAM, 0 multipliers.
- The EP2S60 chip has ~48 k LEs, 288 9-bit multipliers, 2.5 Mbits RAM.
- With only one phased output per chip, use ~50% LEs, 33% of the multipliers, and 8% of the RAM.
  - Seems like each S60 chip might do 2 phased outputs…therefore 4 sub-arrays/sub-band. Or, S30 for 2 sub-arrays per sub-band??

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Summary

- Technical benefits.
  - Fewer Baseline Boards, racks.
  - 3X fewer hi-speed cables.
  - More logical/seamless phasing capability…all bandwidth all the time.

- Technical difficulties/uncertainties.
  - Re-timing hops.
  - Y Recirc FPGA connections for Tx or Rx (expansion).
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  - DC biasing on re-timing FPGA inputs.
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