Correlator

Outline

- Requirements
- Architecture
- Technology
- Software
- Budget
- Schedule
- Installation

Requirements

- 16 GHz bandwidth (8 x 2 GHz bands).
- 16,384 spectral channels/baseline (wideband), 0.25 million (narrower w/recirculation).
- 16 independently tunable digital sub-bands/baseband + N.B. radar filter.
- Flexible: tradeoff B.W. for freq. channels.
- 2 banks of 1000 phase bins/baseline.
- High performance, flexible dumping.
- Very long baseline capable (>10k km baselines).
- 1/16th sample digital delay tracking.
- Baseband and sub-band multi-beaming…on the same data.
- Simultaneous 1 GHz B.W. phased output on multiple sub-arrays.

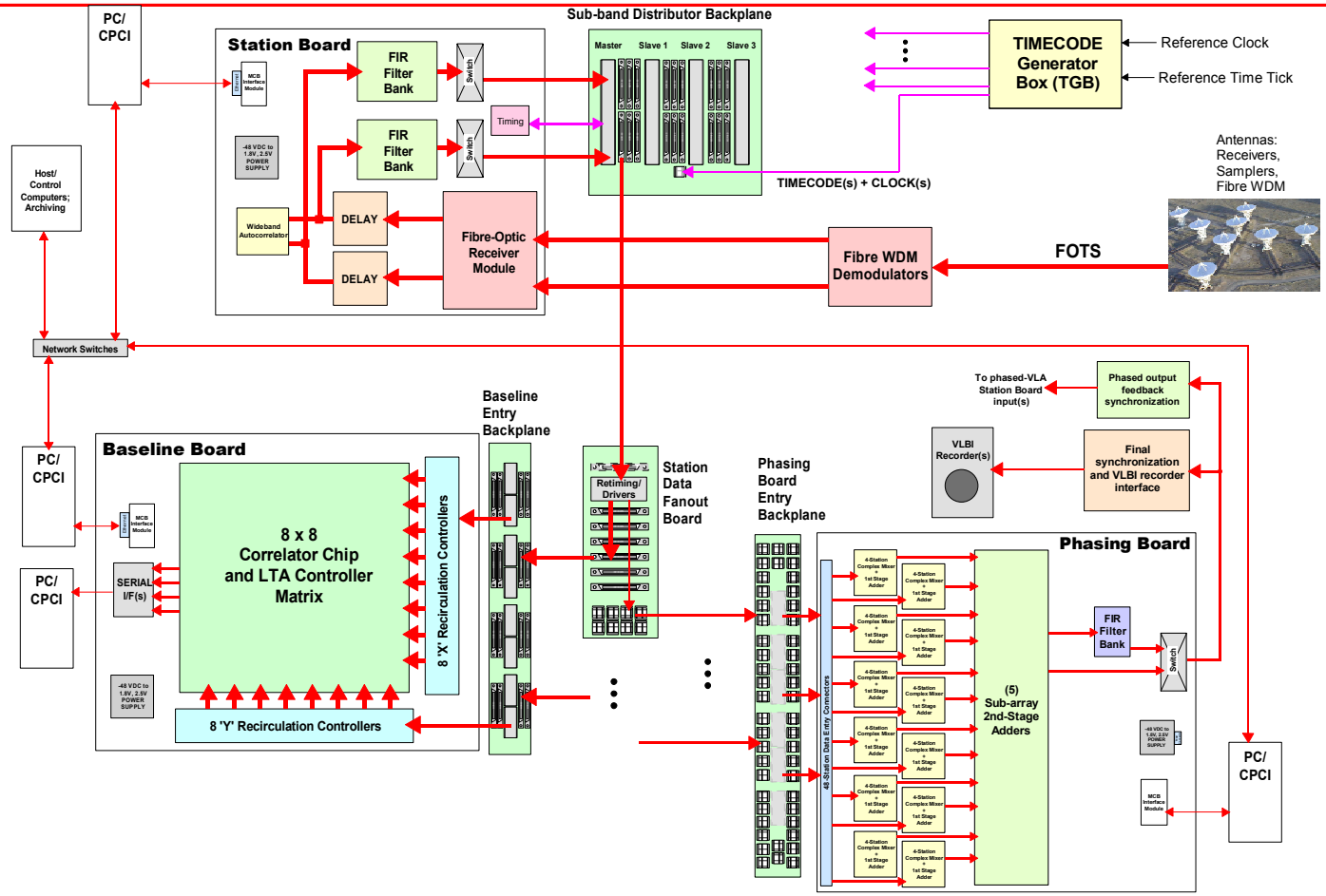
Requirements

Description	"Dream" Correlator Spec.	Planned deliverable
No. of antennas	36	32, expandable
Bandwidth	4 x 2 x 2 GHz (16 GHz)	4 x 2 x 2 GHz (16 GHz)
Freq. Resolution	few Hz ... 10's MHz	1 Hz ... 2 MHz
No. of independently tunable IF pairs	at least 4, prefer 8	64, with digital sub-bands
No. of frequency channels	1000 (full polarization per IF pair), 8000 total	1024 W.B. (more w. recirc) 16384 W.B. total (more w. recirc)
Frequency channel flexibility	split flexibly among IFs, select subset for writing	split flexibly among IFs *and sub-bands*, select subset for writing
Flexibility	Frequency resolution: factors of 2 Flexible tradeoffs (#baselines, B.W., #channels, pol'n, time res'n) Interf. sub-arrays: 4 independent Phased sub-arrays: 4 independent	Ok Can't tradeoff baselines at full bandwidth Interf. sub-array: unlimited. Phased sub-arrays: 5
Integration times	0.1 sec (less with tradeoffs)	0.011 sec (less with tradeoffs)
Total data rates	few tens of Mvis/sec	several Gvis/sec
Autocorrelations	all stokes parameters	W.B. all stokes, SNR loss S.B. all stokes, no SNR loss
RFI	as many channels as possible 10^6 dynamic range automatic flagging gating	Ok: 16,384...262,144 4-bit sampling standard, up to 8-bit sampling avail (d.r. depends on noise+RFI) post-corr. interference excision + facilitates post-corr. cancellation. from antenna, external signal
Pulsar phase binning	up to 1000	2 x 1000, min 15 μsec each
Phase Cal	at least auto-spectra	minimum 1 pCal extractor/IF
Delay tracking	$1/16^{th}$ sample, 250 km baseline	digital $\pm 1/32^{nd}$ sample, 10^4 km+ bl

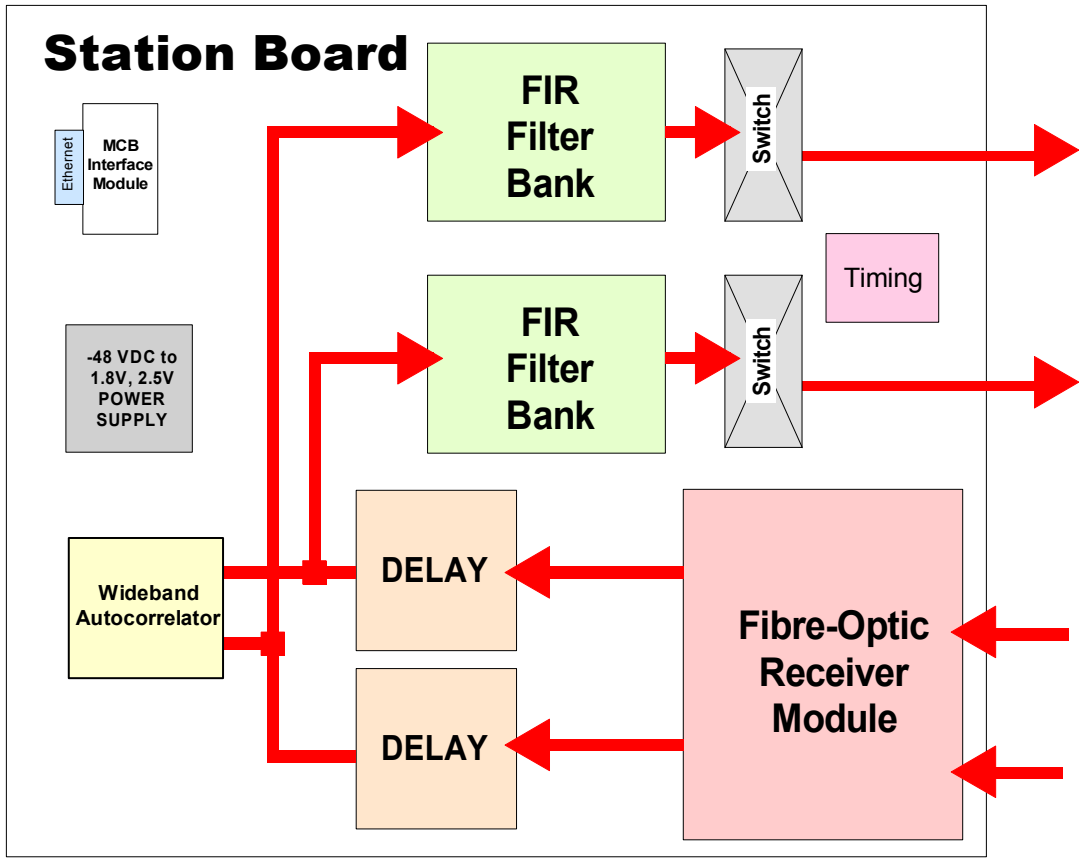
Architecture

- FIR filter banks followed by complex XF correlator:
  - "Stitch" sub-bands together after correlation to yield wideband cross-corr.
  - Use small LO offsets in antenna to keep fringe rotators "wet": *fringe stopping, anti-aliasing, artifact decorrelation, digital sub-sample delay tracking, VLBI.*
  - Each poly-phase FIR independently programmable for flexibility…scientific req't.
- Three main modules:
  - Station Board (2 x 2 GHz).
  - Baseline Board (64 baselines ea).
  - Phasing Board (48 stations, 2 sub-bands, 5 sub-arrays).
- Plus some 4 small interconnect modules…expandable, flexible.

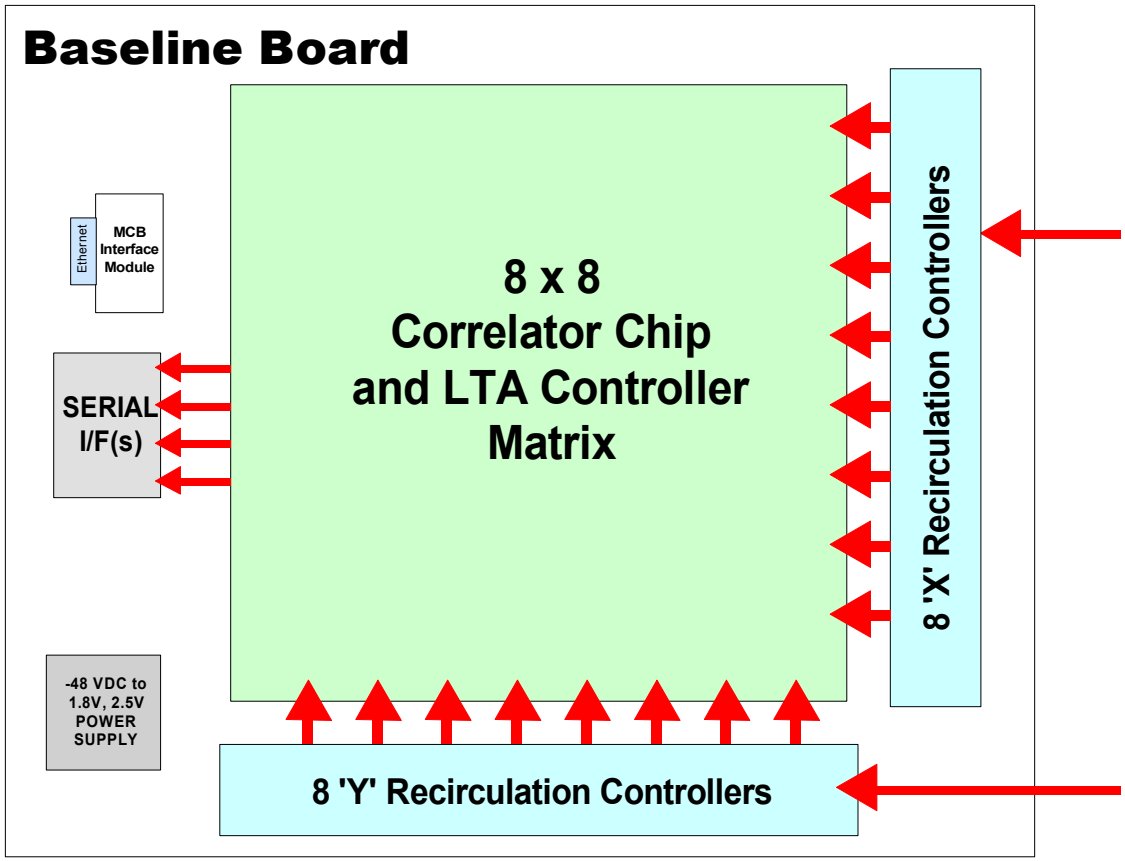
Architecture



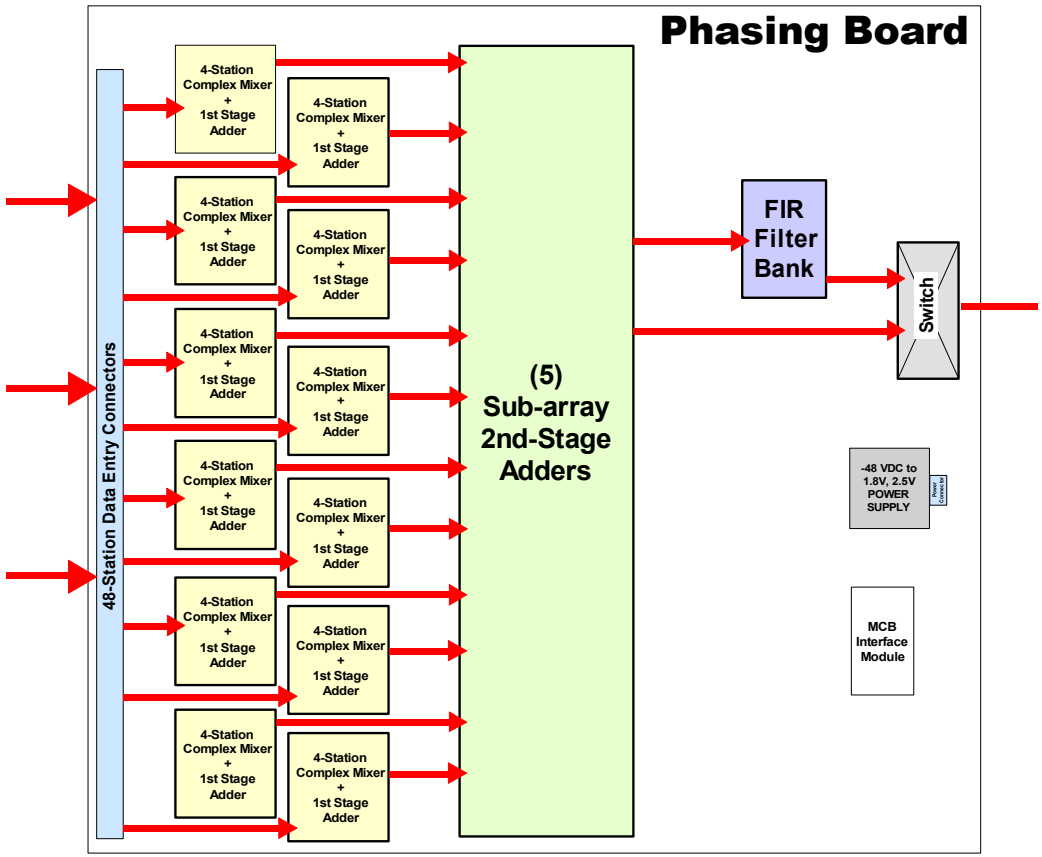
Architecture



Architecture



Architecture



Architecture

- Future upgrade possibilities:
  - "maxed-out" on bandwidth.
  - replace Baseline Board with "Moore" lags…(more channels and/or more bandwidth in bandwidth/number of antennas tradeoff.)
  - keep existing software and hardware infrastructure…painless upgrade.

Technology

- 256 MHz system clock rate:
  - FPGA and gate array tech. supports this.
  - Development tools (Mentor/Cadence) well-equipped for this speed/complexity.
  - Can de-scope to 128 MHz on PCB (with 256 MHz interconnects) if absolutely necessary.
- FIR filter:
  - Prototype in FPGA (power, $$). Convert to 0.18 μm gate array (AMIS). Should be able to get 1024 taps. ($200k NRE, $50 ea, 10k qty). Claim that they use 1/5th the number of gates for same function as Xilinx.
    - 2048-tap power estimate: 20 nW/MHz/gate * 300k gates * 256 MHz * 1.0 (switching fraction) = 1.5W

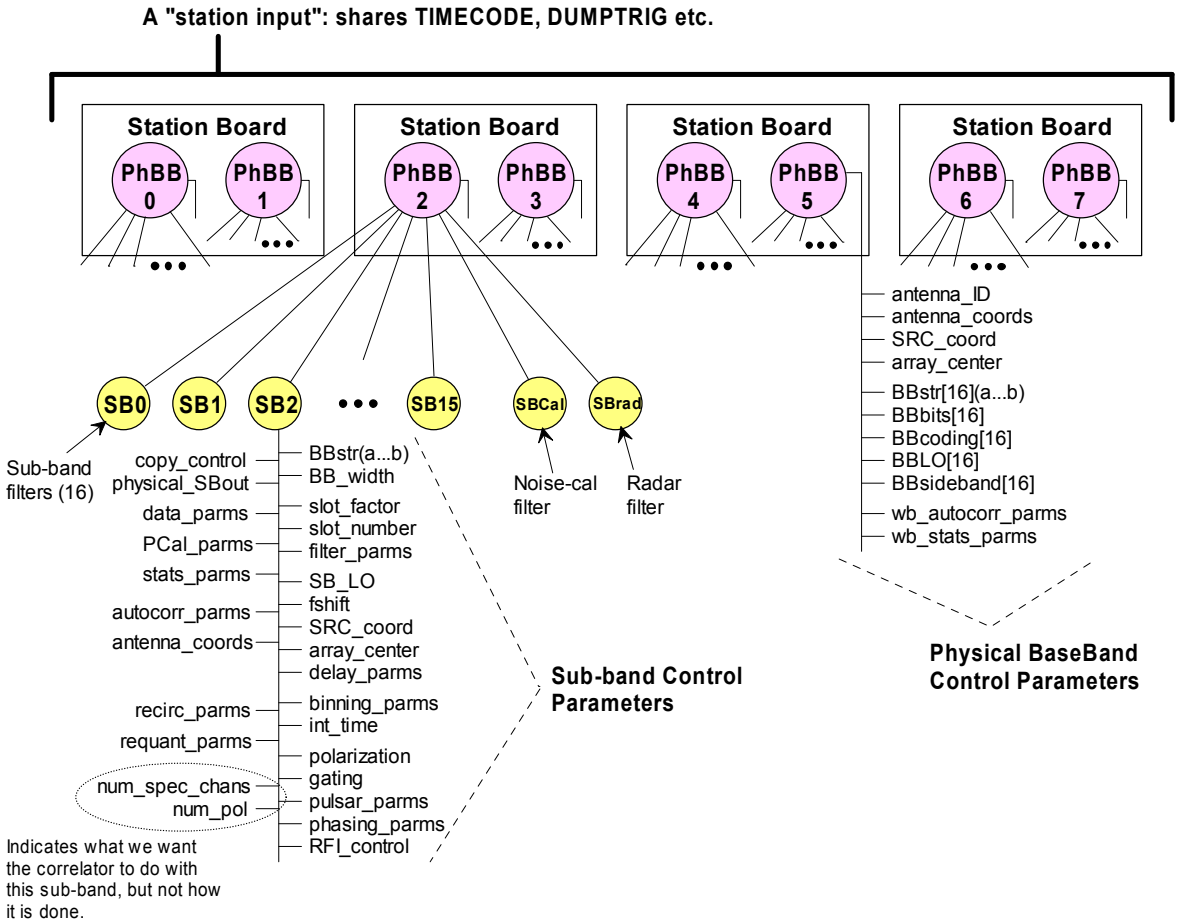
Technology

- Correlator chip:
  - **Original plan:** develop full-custom 0.18 μm standard cell from scratch ($900k NRE + $700k production).
  - **Current plan:** prototype with scaled-down (fewer lags) FPGA, convert to gate array or standard cell afterwards. *Pushes back technology freeze to latest possible date to take advantage of improvements…*
    - **Power**: 20 nW/MHz/gate * 0.5 million (hi-speed switching) gates * 256 MHz * 0.75 transition fraction = 1.9W (2.5W with 1.0 transition fraction)

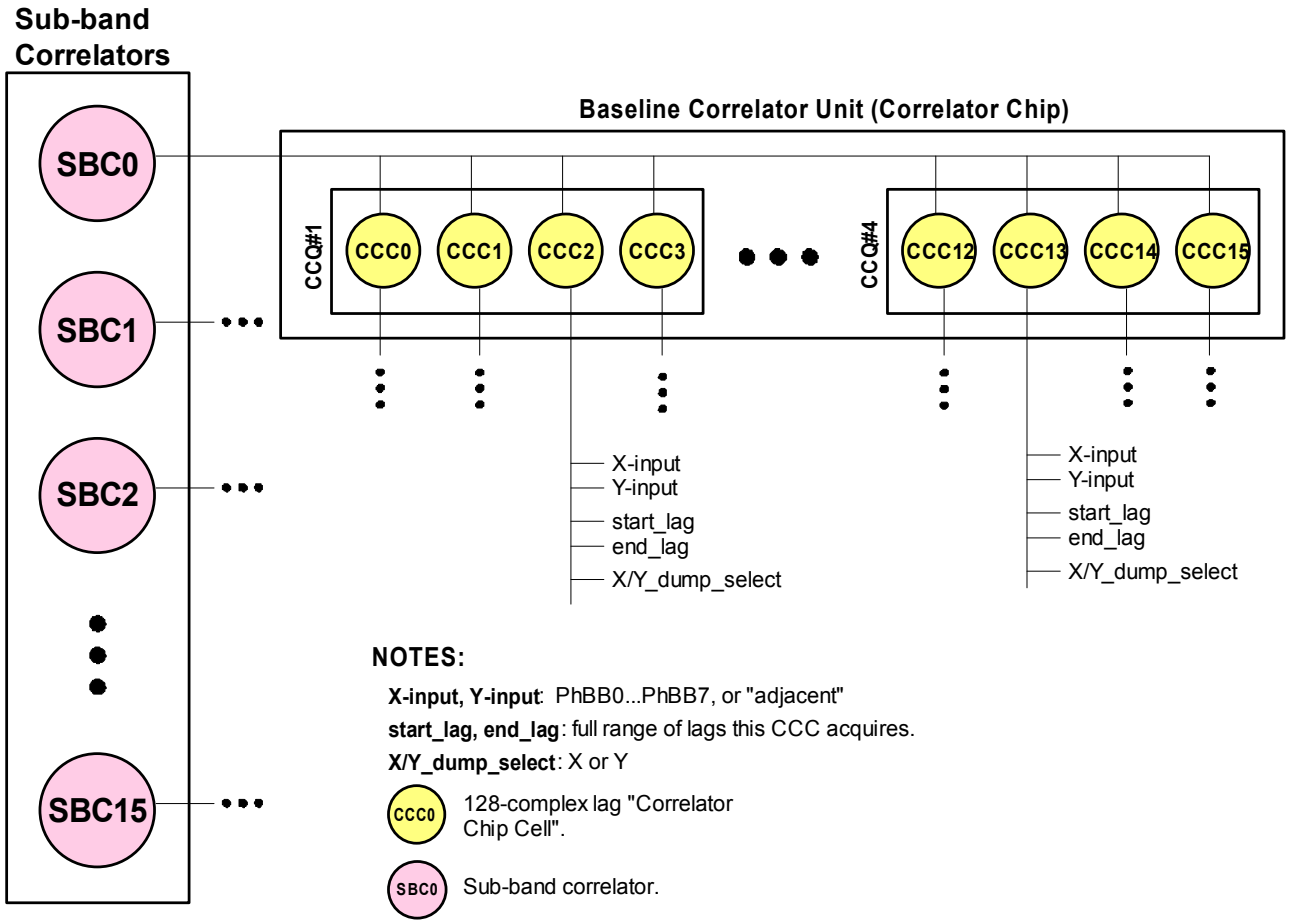
Software

- Use hierarchical approach (mirrors AMCS):
  - 1 SCC and 1 BCC (perhaps one platform).
  - Use NRAO MIBs on boards.
- Backend software/configs…

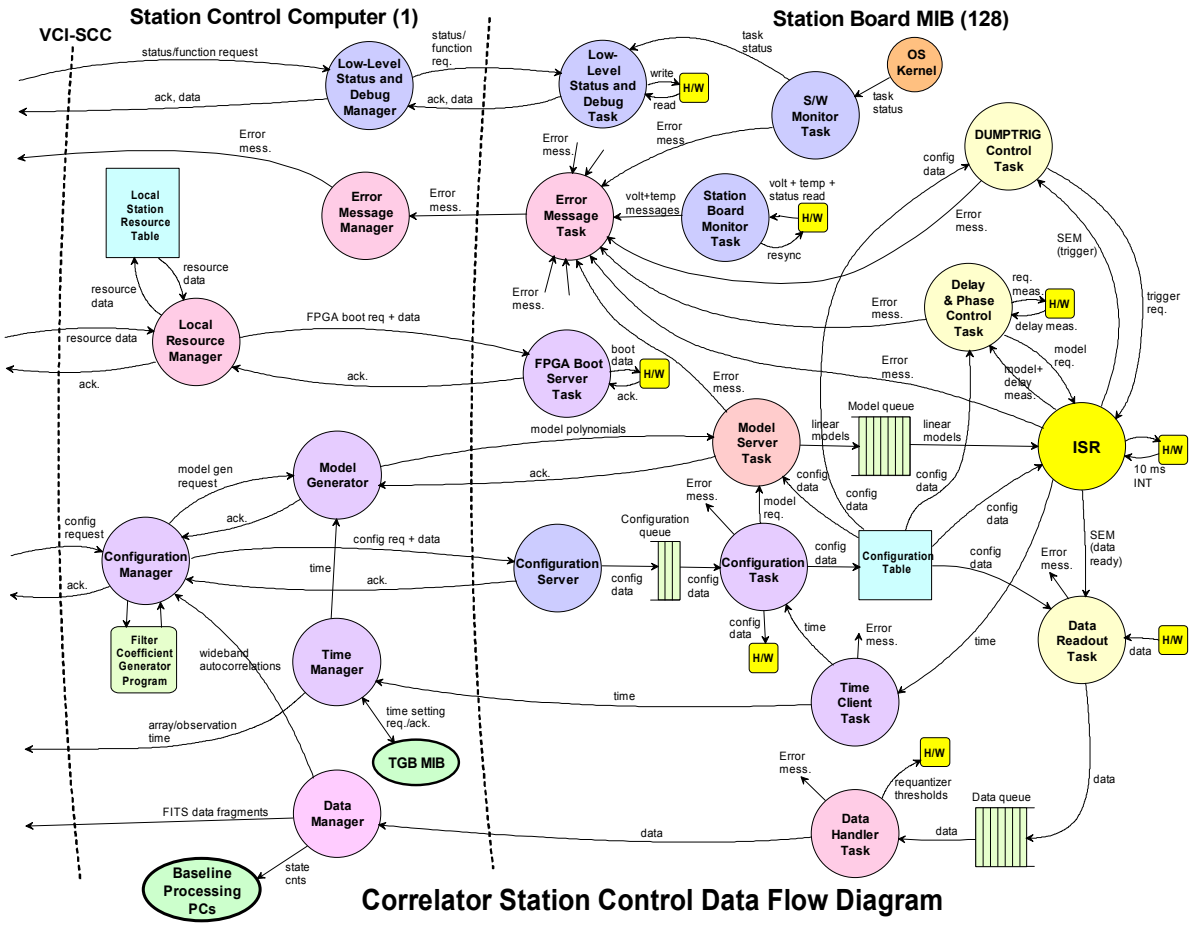
Software


A "station input": shares TIMECODE, DUMPTRIG etc.
Station Board
PhBB 0
PhBB 1
Station Board
PhBB 2
PhBB 3
Station Board
PhBB 4
PhBB 5
Station Board
PhBB 6
PhBB 7
SB0
SB1
SB2
SB15
SBCal
SBrad
Sub-band filters (16)
Noise-cal filter
Radar filter
copy_control
physical_SBout
data_parms
PCal_parms
stats_parms
autocorr_parms
antenna_coords
recirc_parms
requant_parms
num_spec_chans
num_pol
BBstr(a...b)
BB_width
slot_factor
slot_number
filter_parms
SB_LO
fshift
SRC_coord
array_center
delay_parms
binning_parms
int_time
polarization
gating
pulsar_parms
phasing_parms
RFI_control
Sub-band Control Parameters
antenna_ID
antenna_coords
SRC_coord
array_center
BBstr[16](a...b)
BBbits[16]
BBcoding[16]
BBLO[16]
BBsideband[16]
wb_autocorr_parms
wb_stats_parms
Physical BaseBand Control Parameters
Indicates what we want the correlator to do with this sub-band, but not how it is done.

Software

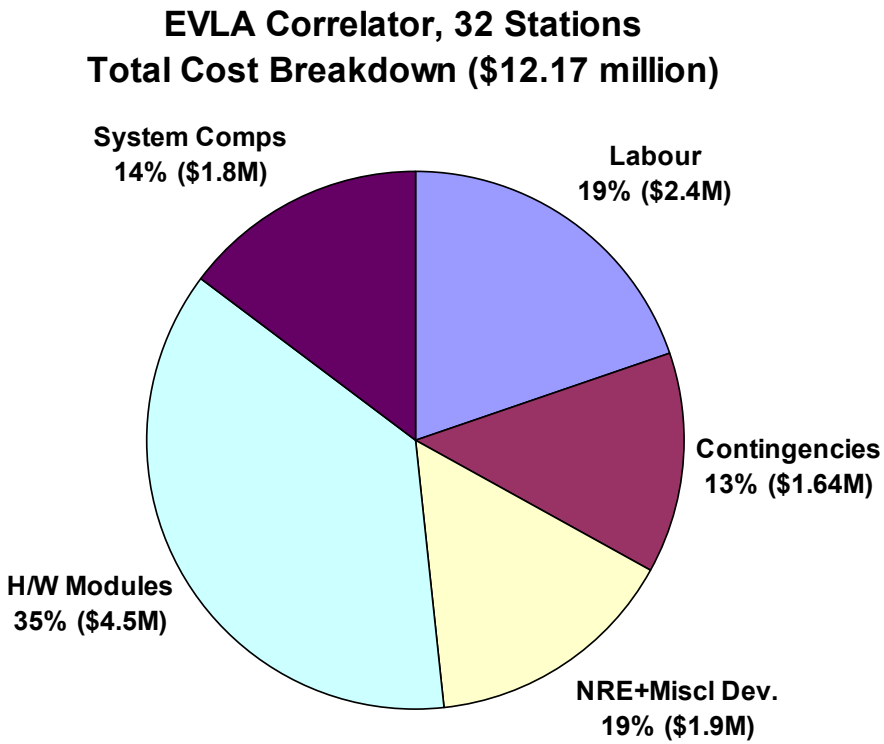

Sub-band Correlators
SBC0
SBC1
SBC2
SBC15
Baseline Correlator Unit (Correlator Chip)
CCC#1
CCC0
CCC1
CCC2
CCC3
CCC#4
CCC12
CCC13
CCC14
CCC15
X-input
Y-input
start_lag
end_lag
X/Y_dump_select
X-input
Y-input
start_lag
end_lag
X/Y_dump_select
NOTES:
X-input, Y-input: PhBB0...PhBB7, or "adjacent"
start_lag, end_lag: full range of lags this CCC acquires.
X/Y_dump_select: X or Y
CCC0
128-complex lag "Correlator Chip Cell".
SBC0
Sub-band correlator.

Software


Station Control Computer (1)
VCI-SCC
Station Board MIB (128)
status/function request
ack, data
Low-Level Status and Debug Manager
status/ function req.
ack, data
Low-Level Status and Debug Task
write
read
H/W
task status
S/W Monitor Task
OS Kernel
task status
Error mess.
Error Message Manager
Error mess.
Error Message Task
volt+temp messages
Station Board Monitor Task
volt + temp + status read
resync
DUMPTRIG Control Task
config data
Error mess.
SEM (trigger)
Local Station Resource Table
resource data
resource data
Local Resource Manager
resource data
ack.
FPGA boot req + data
ack.
FPGA Boot Server Task
boot data
ack.
Error mess.
Delay & Phase Control Task
req. meas.
delay meas.
trigger req.
model req.
model+ delay meas.
Model Server Task
model polynomials
ack.
Model queue
linear models
linear models
ISR
10 ms INT
model gen request
Model Generator
ack.
config request
Configuration Manager
ack.
config req + data
time
ack.
Configuration Server
Configuration queue
config data
Configuration Task
config data
Configuration Table
config data
SEM (data ready)
Error mess.
Filter Coefficient Generator Program
wideband autocorrelations
Time Manager
time setting req./ack.
TGB MIB
array/observation time
time
Time Client Task
Data Readout Task
data
FITS data fragments
Data Manager
state cnts
Baseline Processing PCs
Error mess.
requantizer thresholds
Data queue
Data Handler Task
data
Correlator Station Control Data Flow Diagram

Budget

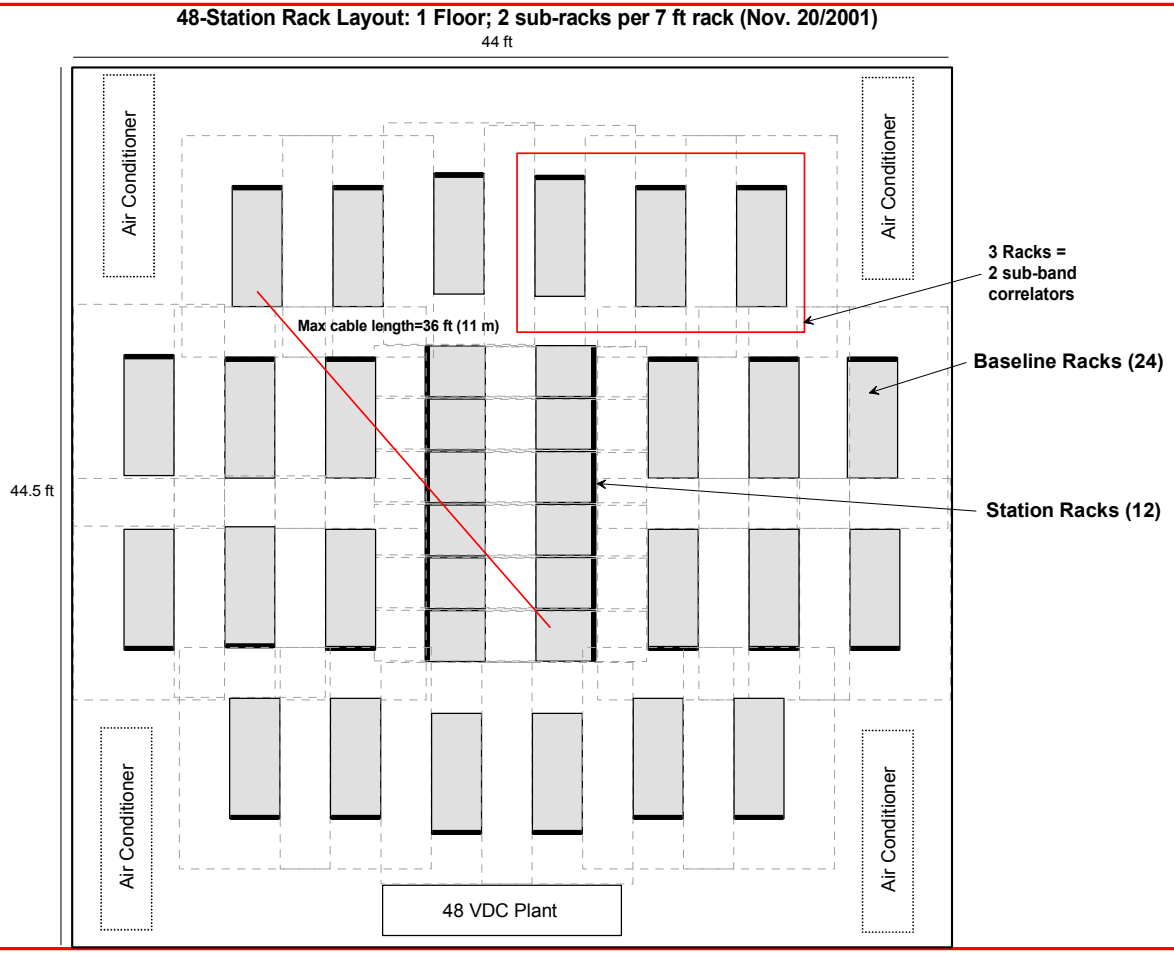
Could shave ~$1.3 million off this budget with cheaper cables and AMIS gate array for FIR (& corr chip).



Schedule

Date	Milestone
Nov. 2/2001	Conceptual Design Review (**CoDR**). Design frozen.
Q1, 2002	New personnel in place. Design tools in place. Training and design work begins.
Q1, 2004	Critical User Manuals in place. Device driver code can be written.
Q2, 2004	Preliminary Design Review (**PDR**). Designs ready for prototype fabrication.
Q1, 2005	Prototype test at the VLA starts.
Q2, 2005	Prototype test at the VLA complete.
Q3, 2005	Critical design review (**CDR**). Prototype testing complete. Ready for procurement of production components and full production.
Q2, 2006	Production model test and burn-in, system integration and test in Penticton, and rack and cable installation begins at the VLA.
Q4, 2006	Begin full installation at the VLA. Earliest possible start of installed correlator testing.
Q2, 2007	**Earliest possible "beta" science data**. (Middle of full installation schedule.)
Q1, 2008	Correlator commissioning. Correlator fully on-line for observing. Continuing debug support available.
Q1, 2009	End of project. End of NRC debug support. Full handover to NRAO complete.

Installation



Summary

- Wideband, high-performance, flexible.
- Expandable, re-configurable.
- Painless upgrade path.
- (0→10k+ km baselines).
- $10 - $12 million (32 stations; another ~$6 million for 48 stations).
- Start installation ~2006.
- First “beta” science ~2007.
- Completion 2008-2009.