EVLA M&C Transition System Software Critical Design Review

December 5-6, 2006

WIDAR Correlator Board Component Software

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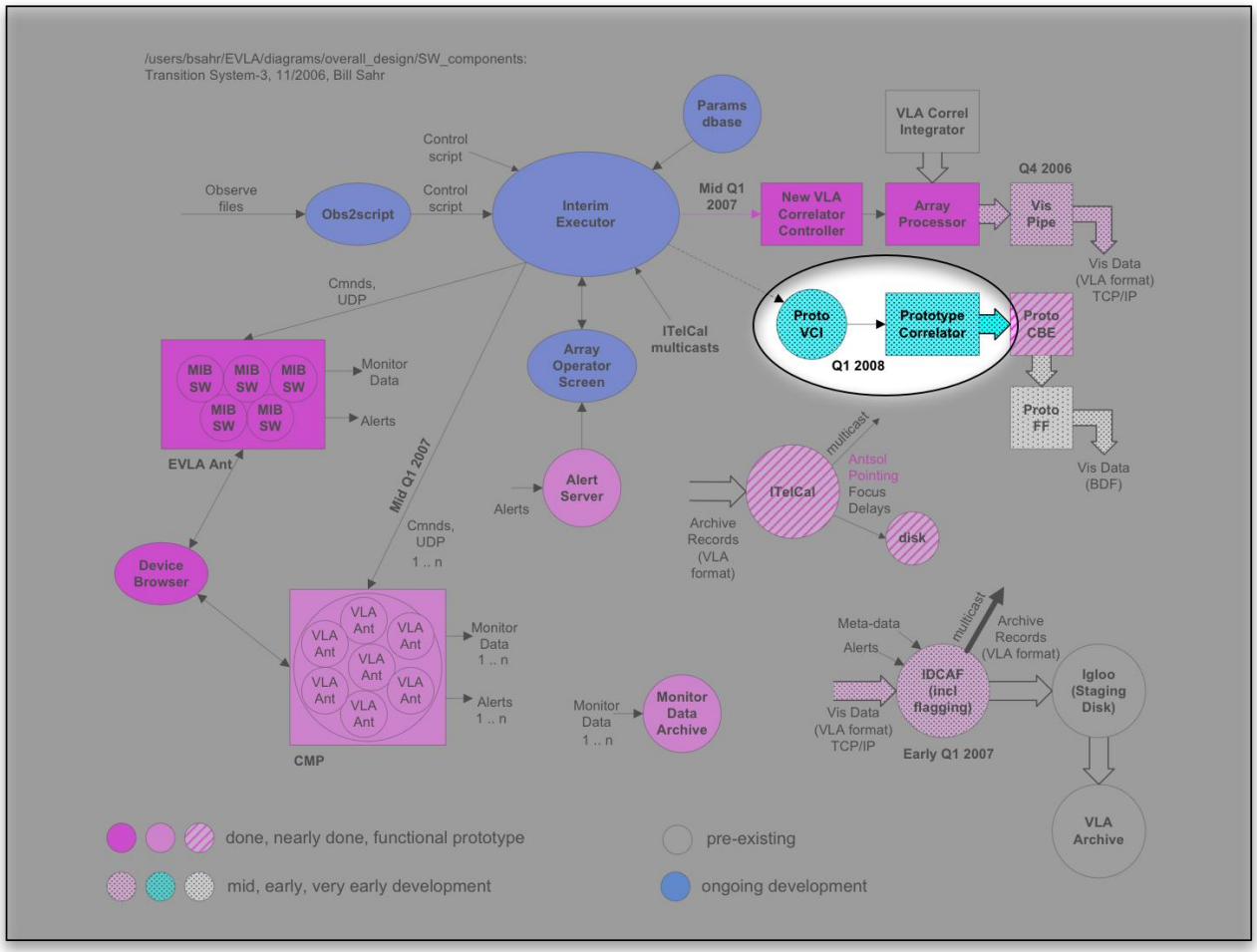
WIDAR board component software

Normal operation of the WIDAR Correlator in the EVLA will be done through the Virtual Correlator Interface (VCI).

During the installation and initial phases of operation however, some of the control, monitor and testing will be done at lower, board and individual component levels.

The purpose of this discussion is not for the review of the design of the board-level software but for review of its interface for initial integration of WIDAR into the EVLA system.

Place in the System



Discussion Content

- Overview of Correlator (Physical Description)
- S/W Requirements References
- Network ‘Middleware’
- CMIB (Server-side) Software
- GUI (Client-side) Software

WIDAR Physical Description

Racks in the WIDAR System:

- 2 Control Racks (one is hot standby) each:
  - 2 CPCCs (Correlator Power Control Computers)
  - 3 CMIB Boot Servers
    - MCCC functionality may reside on one of these
- 3 CBE Racks
  - Containing ≈ 50 Blade Servers
- 24 Correlator Racks
  - Contain the correlator electronics
  - The boards of interest for this discussion are the Station and Baseline boards.

WIDAR Physical Description (cont.)

A 32-station correlator:

24 Correlator Racks
- 16 Baseline
- 8 Station

X

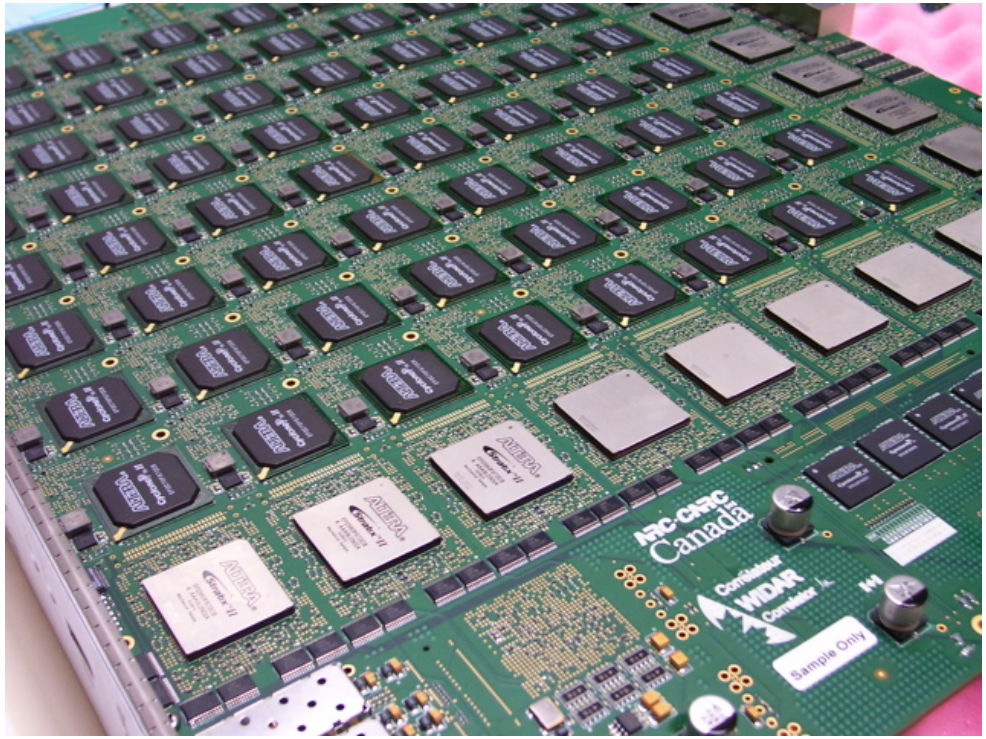
Boards per Rack
- 10
- 16

=

160 Baseline Boards
128 Station Boards

WIDAR Physical Description (cont.)

WIDAR Physical Description (cont.)



Each board contains dozens of configurable devices

- Correlator Chips, FIR Filter FPGA's, Recirculator FPGA's, LTA FPGAs, etc.

Boards		Devices/board		Total Devices
160 Baseline	X	146	=	23360
128 Station		47		6016

≈ 30,000 devices to be configured/monitored

WIDAR Physical Description (cont.)

Each Station and Baseline board contains a PC-104 computer

- Correlator Module Interface Board (CMIB)
- 166-MHz Intel Pentium processor
- Linux OS
- >= 128 Mbytes RAM
- no disk or FLASH
- 100 Mbit Ethernet

S/W Requirements

WIDAR Board S/W Requirements

The WIDAR document site:

http://www.drao-ofr.hia-iha.nrc-cnrc.gc.ca/science/widar/private

- General CMIB and UI performance:
  - RFS* Document A25204N0001, “Software Requirements for Testing of the Board Prototypes”, Sonja Vrcic, Bruce Rowen.
  - TVP** A25081N0001, Baseline Board Prototypes, B. Carlson
  - TVP A25040N0003, Station Board Test and Verification Plan, D. Fort
  - RFS A25220N0000 Prototype Board User Interface Description, K. Ryan
  - User Manual A25200N0011, Programmer’s Guide to the EVLA Correlator User Interface System, K. Ryan
- Specific Requirements for S/W-H/W interaction:
  - User Manual A25290N0000, Programmer's Guide to Correlator System Timing, Synchronization, Data Products, and Operation
  - Various other RFS documents, one for each of the FPGA’s and Correlator Chips

*Requirements and Functional Specification
**Test and Verification Plan

WIDAR Board S/W Requirements (cont.)

Very generally:

- CMIB S/W
  - Provide board initialization
  - Load FPGA personalities
  - Perform constant real-time monitor/control of board hardware
  - Provide specific board ‘functionality’
  - Provide an interface to that functionality for external applications
- User Interface S/W
  - Provide various levels of access to hardware
    - Whole board configuration
    - Individual device (FPGA, Correlator Chip) configuration
    - Peeking/poking individual registers within a device

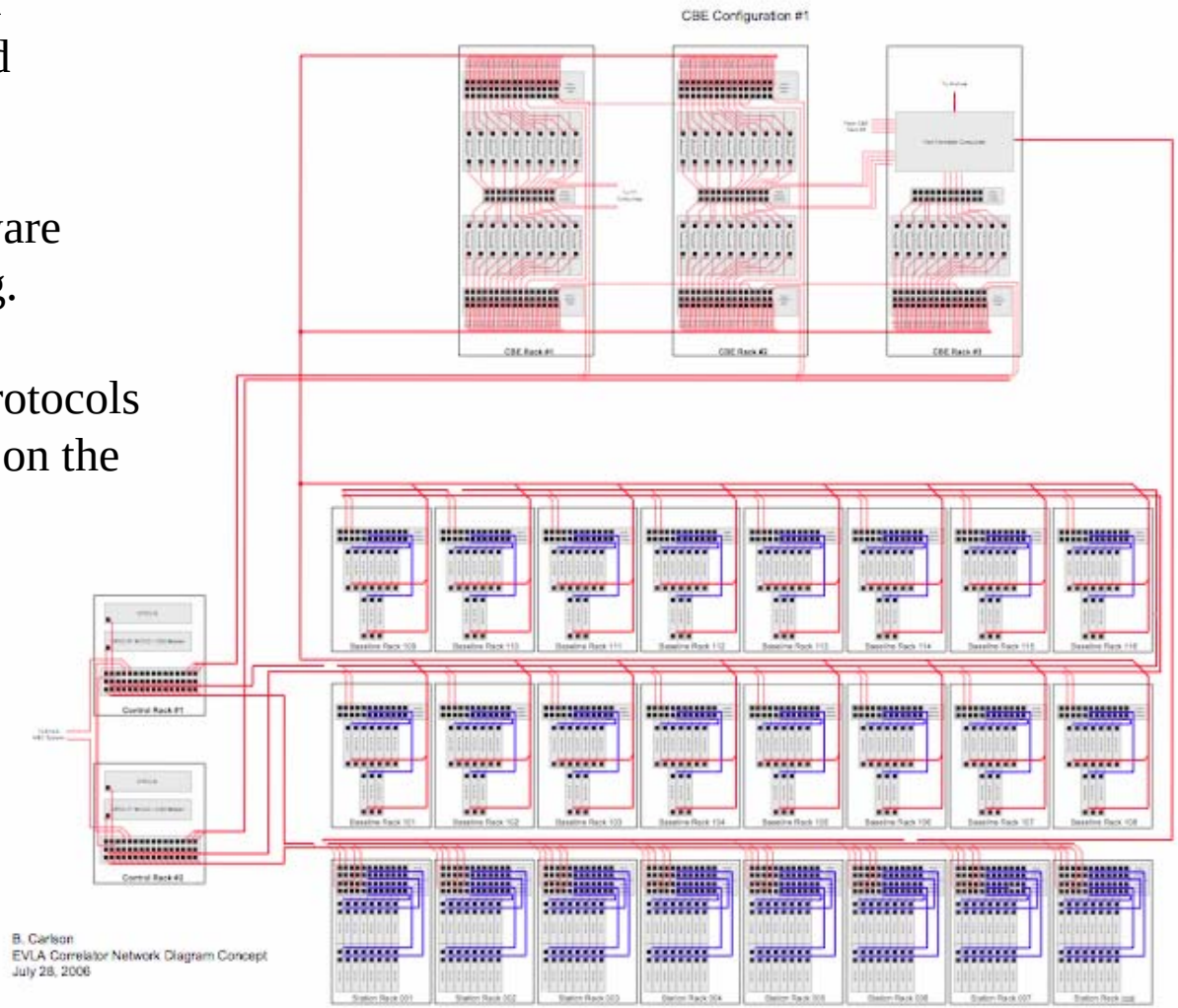
Communication Middleware

Middleware Description

• Every computer, even embedded, is connected via IP/Ethernet.

• COTS network hardware
  • switches, cabling.

• All communication protocols are the same ones used on the Internet.



Middleware Description (cont.)

A natural middleware candidate for this type of infrastructure is one based on the Internet and, more specifically, the World Wide Web.

REST (Representational State Transfer) is an architectural style created to describe the World Wide Web

"REST provides a set of architectural constraints that, when applied as a whole, emphasizes scalability of component interactions, **generality of interfaces**, [and] independent deployment of components."

R. Fielding, Architectural Styles and the Design of Network-based Software Architectures, PhD. Disertation, University of California, Irvine, 2000.

Middleware Description (cont.)

REST is Client/Server based
In WIDAR:

- Servers are the remote computers and processes representing the system that is to be M&C'd.
  - CMIBs are the servers of correlator board/chip-level M&C.
  - Every WIDAR server (including CMIBs) will have a Web Site.

- Clients are the UI's and other M&C'ing applications
  - Client s/w can be hosted on any machine connected to the Internet.
  - UI's can be specially created GUIs or standard Web browsers.

The WIDAR Correlator will sport almost
300 individual Web sites.

Middleware Description (cont.)

"REST components perform actions on a resource by using a representation to capture the current or intended state of that resource and transferring that representation between components."

In WIDAR, resources are:

- Hardware
  - a chip, a board, a register, the whole correlator
- Data
  - configuration files, correlator data files
  - streaming data

Fielding

Middleware Description (cont.)

REST uses two well-defined industry standards to communicate these resource representations between client and server:

- The URI - to specify the resource
  - (the URL is a subset of the URI)
- HTTP - to transport its representation

In a manner opposite of RPC architectures, REST is

- "resource-centric rather than method-centric".
- "it defines a small global set of verbs (the HTTP Methods: GET, POST, PUT, etc) and applies them to a potentially infinite set of nouns (URIs)."

P.James, http://www.peej.co.uk/articles/rest.html

Middleware Description (cont.)

WIDAR hardware representations are conveyed in XML

- It describes the *state* of the component
  - configuration parameters, error counts, statistical counts, register values

M & C of WIDAR consists of communicating XML messages of current and intended states between its components.

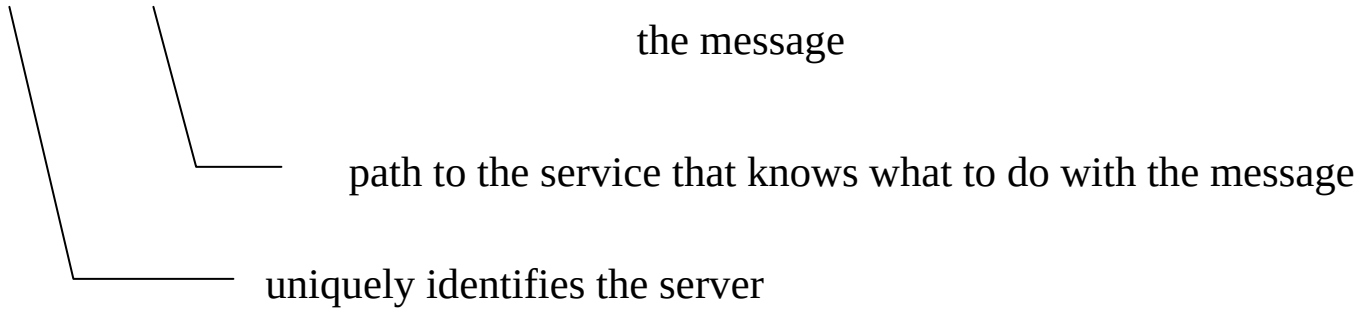
An XML message can be simple:

```
<lta id='x1y2'><state register=''/></lta>
```

Middleware Description (cont.)

The XML can be placed inside a URL and sent via HTTP GET:

```
http://cmib1/mah?<lta id='x1y2'><state register=''/></lta>
```

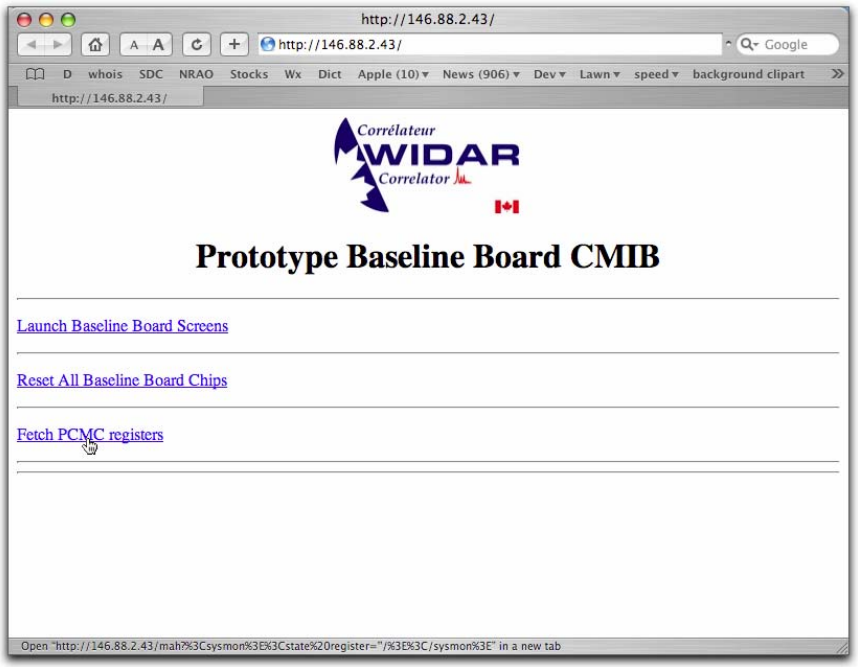


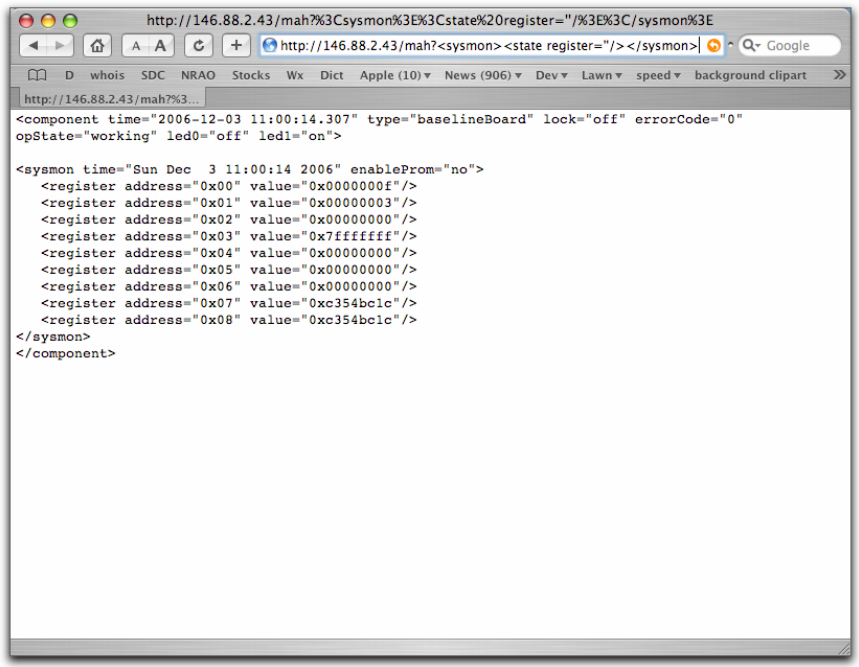
- The URL above is what a GUI sends to a CMIB to retrieve the values of an LTA's register set.
- It can also be entered into a standard web browser (or clicked on as a link) to display the registers …

Middleware Description (cont.)

An HTML link to fetch the PCMC's register set:

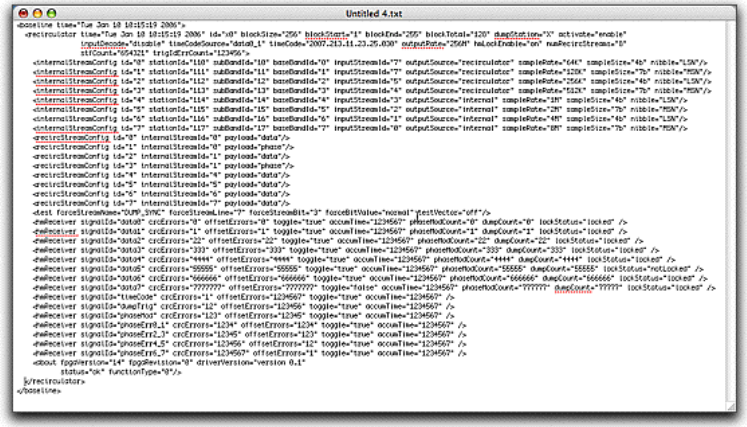
```
<a href="mah?<sysmon><state register=''/></sysmon>">Fetch PCMC registers</a>
```

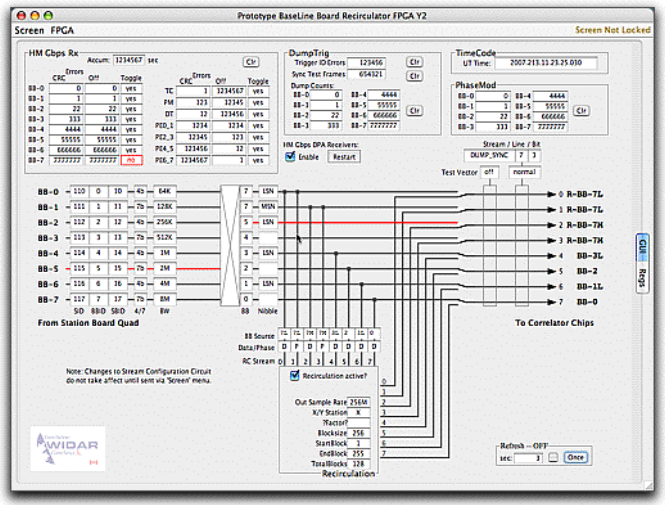




XML is also stored in *configuration files*.

GUIs can read and write the files and …





- once loaded they provide a graphical representation of the XML *in the context of the hardware*
- the settings can be modified in the GUI (pressing buttons, etc.) and sent back to the file or to the hardware itself.

… GUIs can read and write XML back and forth to hardware

Recirculator FPGA

Middleware Description (cont.)

Configuration files reside on the servers

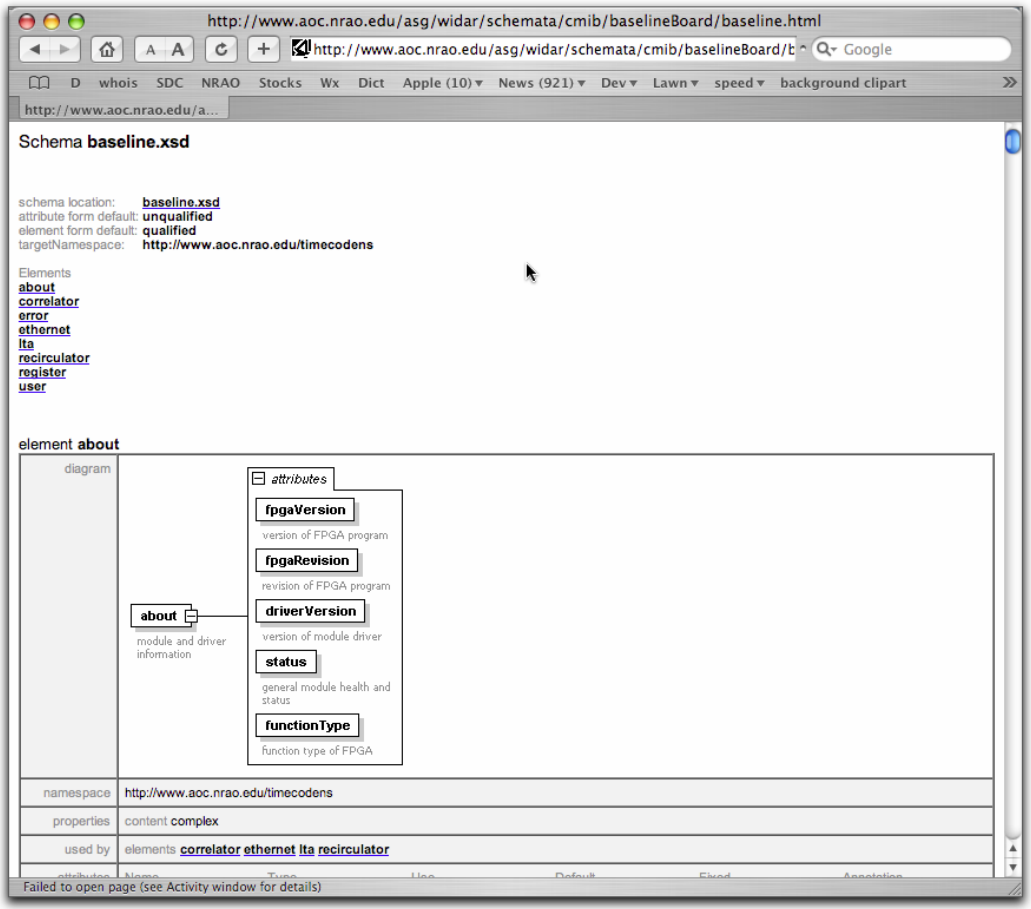
- This allows loading them by communicating only their name over the network rather than sending the whole file.

Board-level GUIs provide means to load configuration files into all of a board's devices in one operation.

Middleware Description (cont.)

Each WIDAR component ‘API’ is defined by XML schemata

- At: http://www.aoc.nrao.edu/asg/widar/schemata/

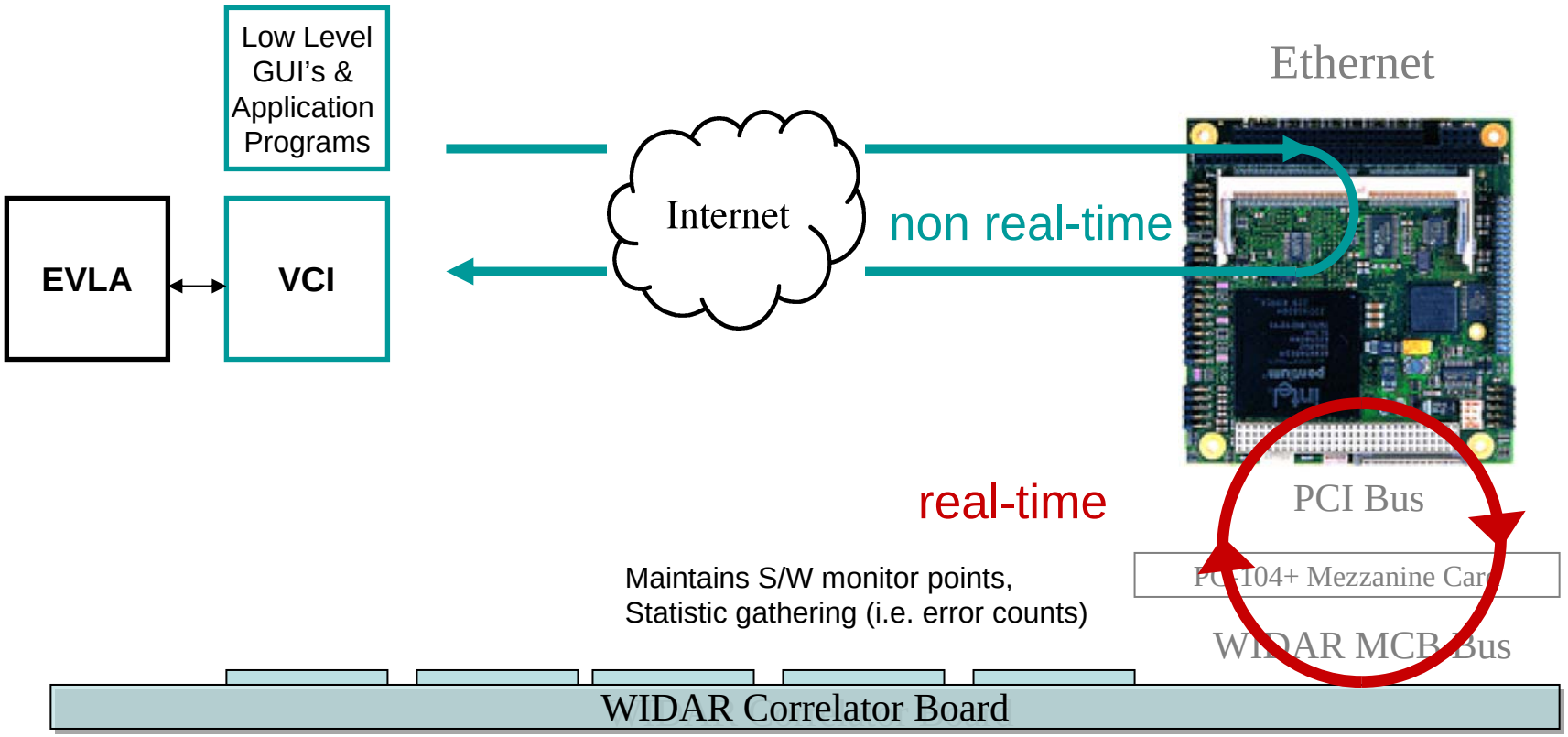


CMIB Software

Bruce Rowen / Kevin Ryan

CMIB Software Description

CMIBs maintain constant real-time control of their attached board and provide an on-demand, non-real-time interface to external users.



CMIB Software Description (cont.)

- Off the shelf Linux.
- At boot time, a file system is mounted (via NFS) from one of the CMIB server machines.
- Layers of application software:

CMIB Software Description (cont.)

Server-side external interface software

- Apache's Tomcat off-the-shelf web server

Ethernet

HTTP Web Server

Web Application 'Business Logic'

Module Access Handlers (MAH)

Hardware Device Drivers

PCI Bus

PC-104+ Mezzanine Card

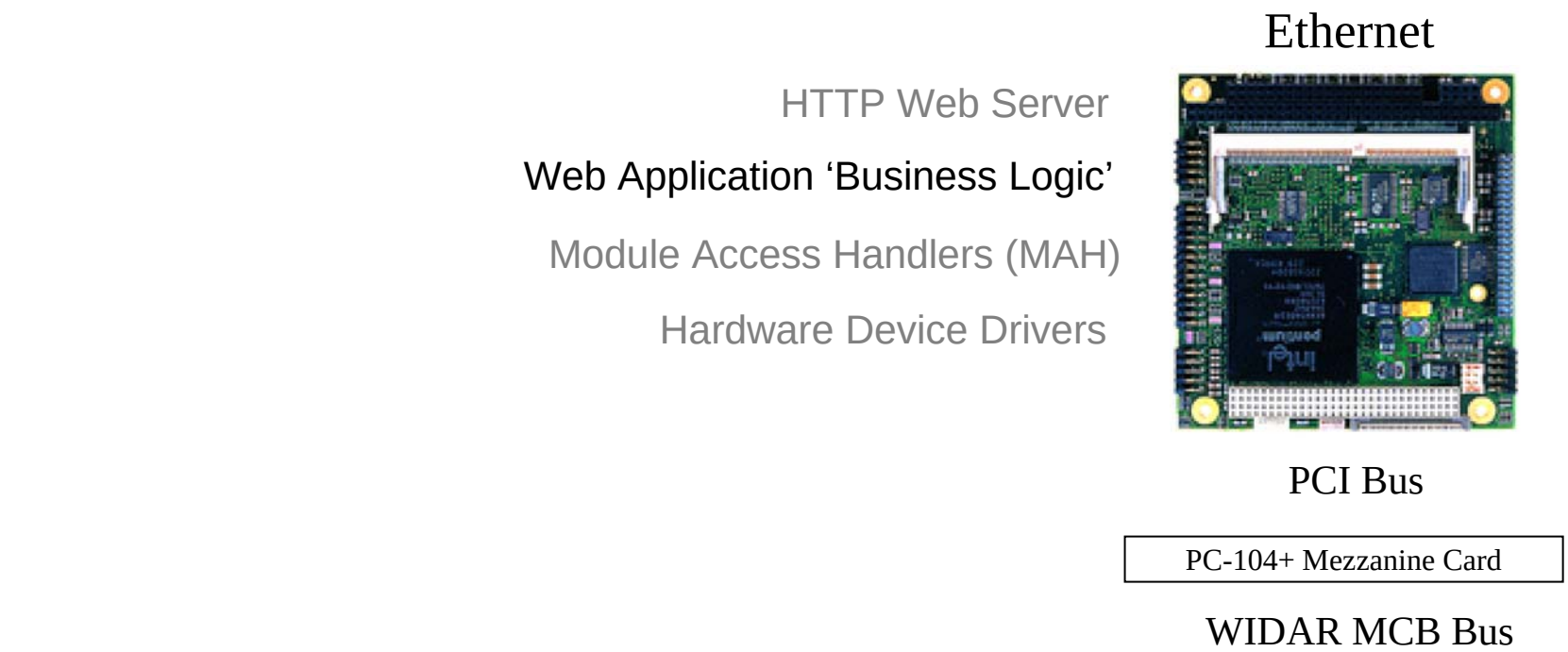
WIDAR MCB Bus

WIDAR Correlator Board

CMIB Software Description (cont.)

Server-side external interface software

- Web-based interface to client applications
- Device Driver like interface to MAHs (similar to file or Unix pipe I/O)
- Java Servlets and JSPs
- Web site (static web pages)



CMIB Software Description (cont.)

MAHs run in Linux User space

- XML interface to next higher level
  - Translates XML to IOCTL calls
- Provides three levels of h/w access:
  - *Register* (I/O directly with an FPGA/Correlator Chip)
  - *Basic Function* (mnemonic access to FPGA functions)
  - *Abstract Function* (generic configuration and control, hides FPGA structure)

HTTP Web Server

Web Application 'Business Logic'

Module Access Handlers (MAH)

Hardware Device Drivers

PCI Bus

PC-104+ Mezzanine Card

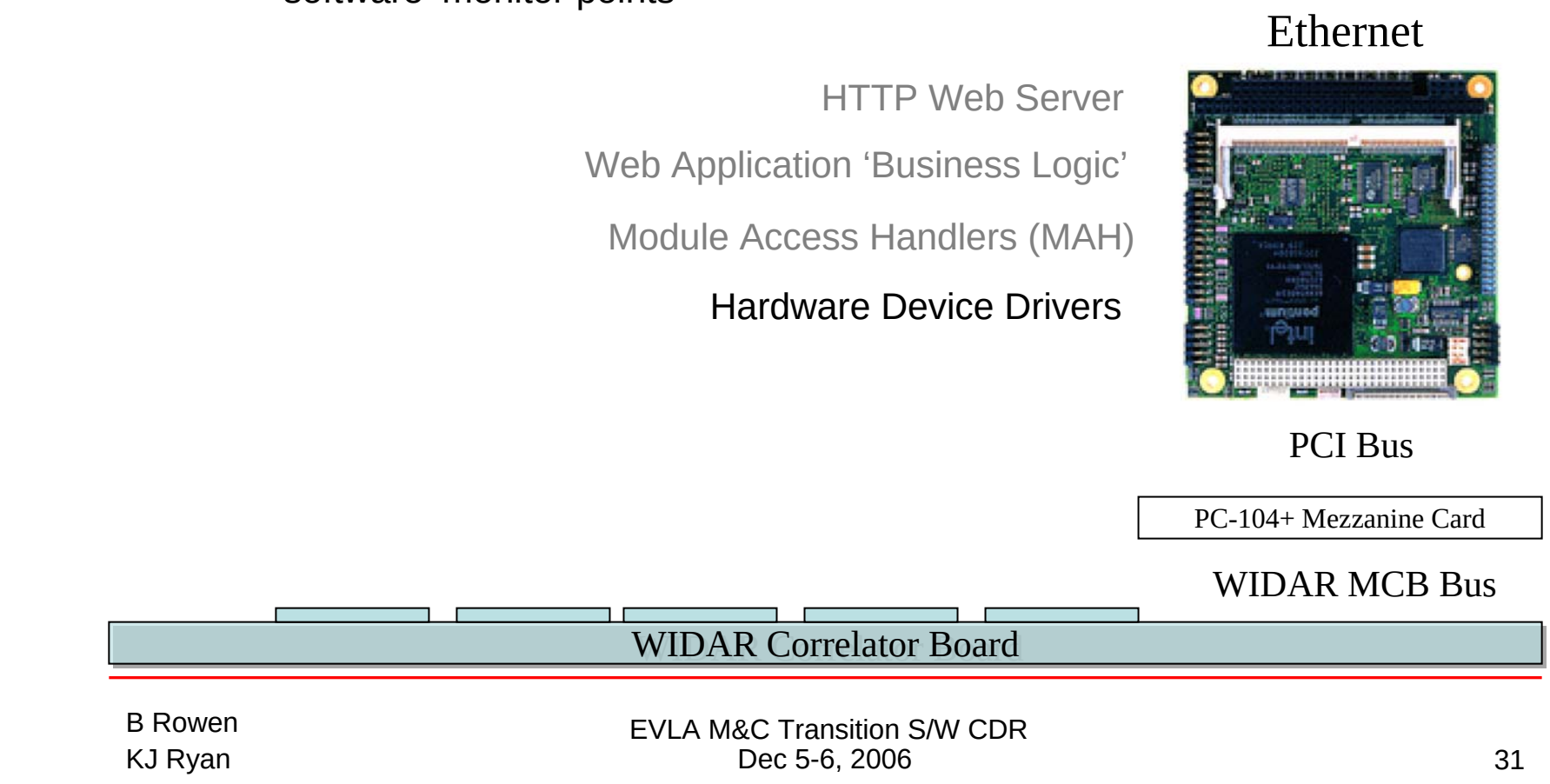
WIDAR MCB Bus

WIDAR Correlator Board

CMIB Software Description (cont.)

Real-time software that runs in Linux Kernal space

- 10 millisecond interrupts
- IOCTL interface to MAH layer
- Memory mapped I/O to h/w via PCI bus
- Provides low-level control/monitor
  - ‘software’ monitor points



Board-Level GUIs

Sonja Vrcic / Kevin Ryan

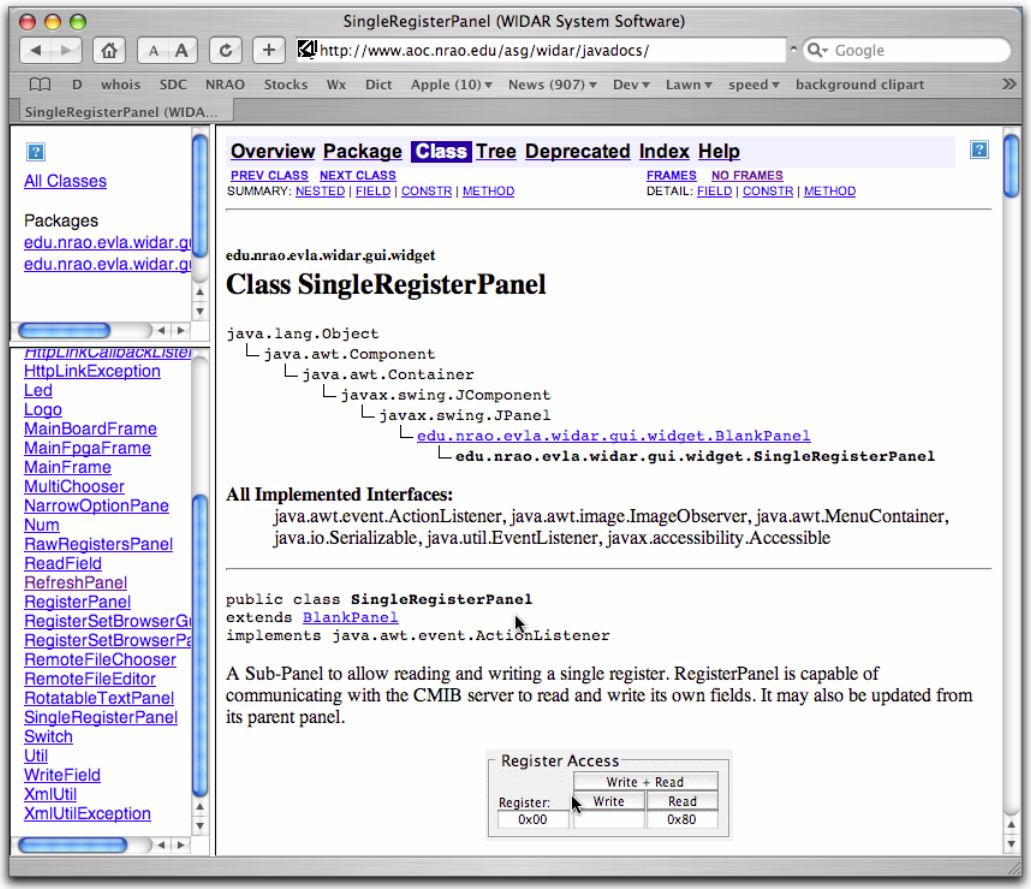
GUI Software Description

GUI's:

- Operate on Windows, U/Linux and Mac OS-X,
- Operate over the Internet,
  - We are currently using them for initial debug and test of the recently arrived prototype Baseline Board in Penticton, BC, Canada.
- Are created using Java's Swing components,
- Are served to clients from AOC's Web Server,
- Are launched using Java Web Start.
  - A user simply points his browser to a CMIB's web site and clicks on the application's link.
  - This assures that the client is using the most up-to-date version.
  - If the client has the latest version, no downloading is necessary.

GUI Software Description (cont.)

Software common to GUIs such as reusable sub-panels, XML parsing and HTTP communication, are packaged separately and their API documented on a web site with Javadoc.



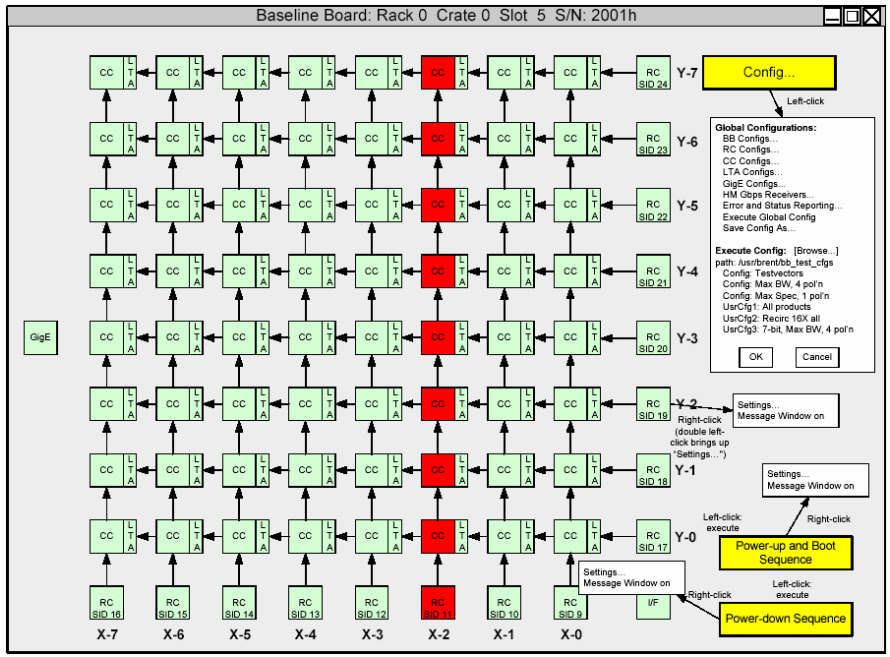
GUI Software Description (cont.)

Station Board and Baseline Board GUIs:

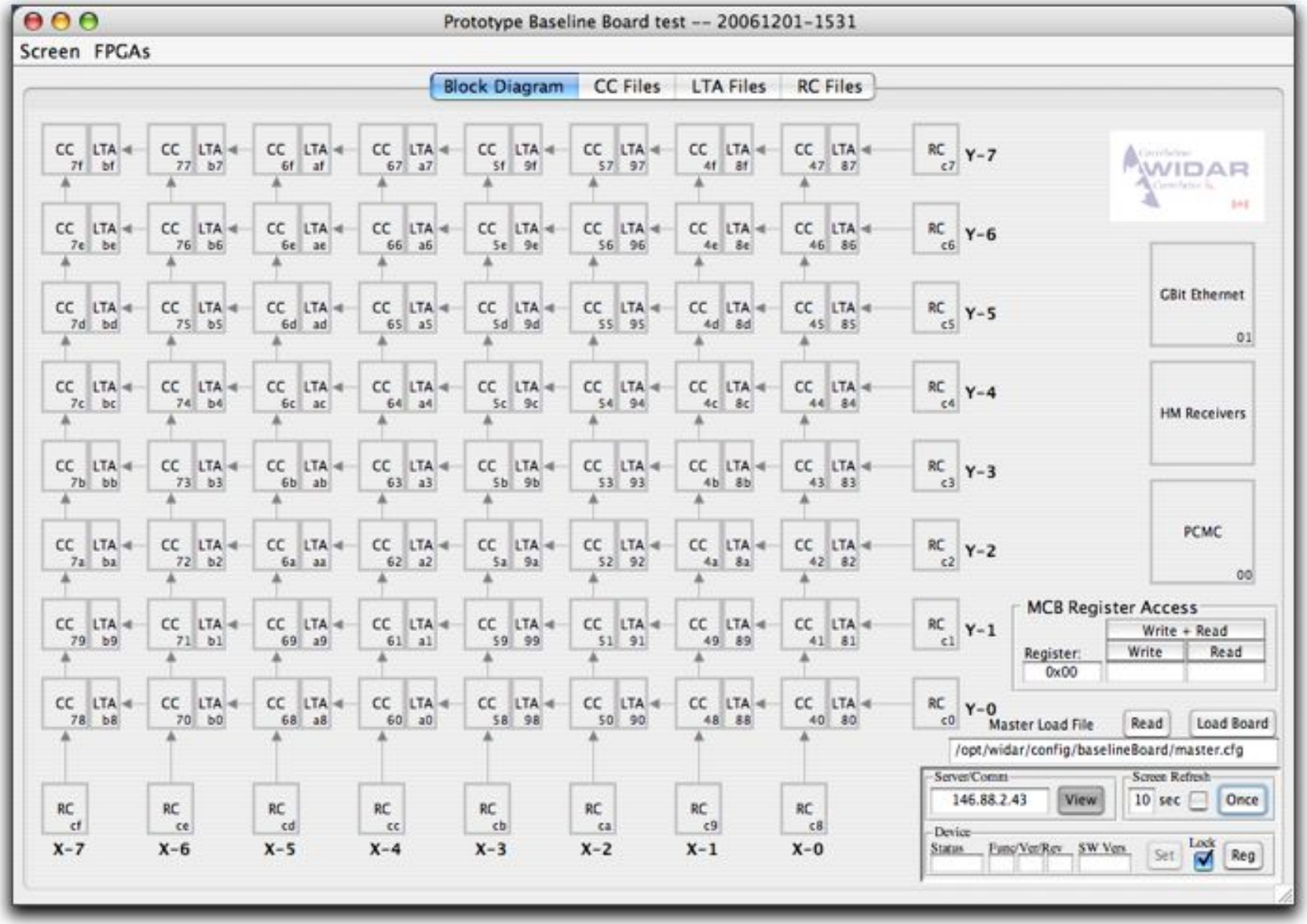
- Consist of an overall board block diagram,
  - Depicting its various sub-components (referred to as ‘devices’ or simply ‘chips’).
- and at least one chip-level GUI for each of the board’s sub-components.
  - That show the ‘inside’ of the device,
  - Are launched by clicking on the chip’s icon on the board block diagram GUI,
  - Provide at least one panel showing the device graphically and also a panel providing lower-level access to the device’s register set.

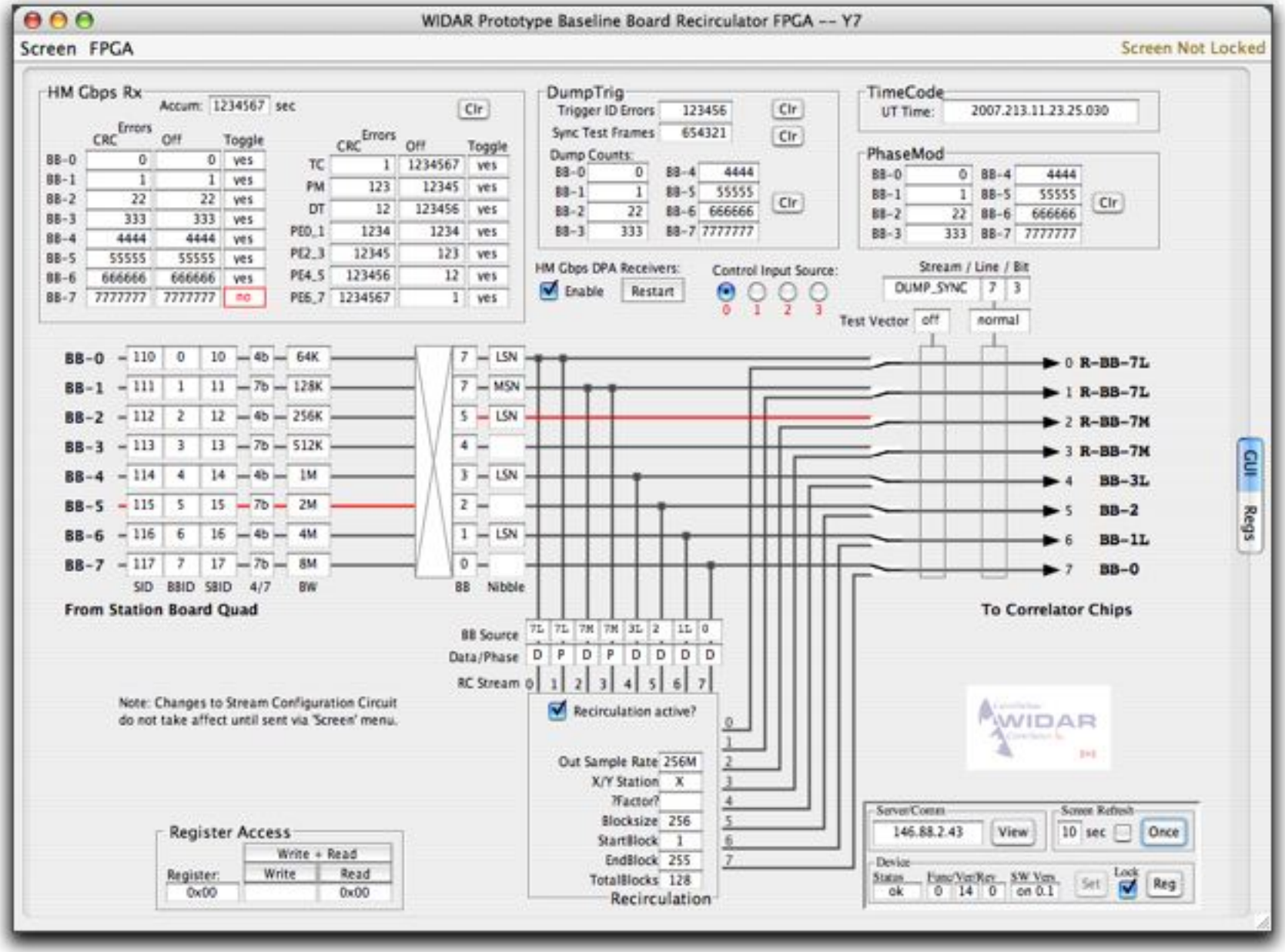
GUI Software Description (cont.)

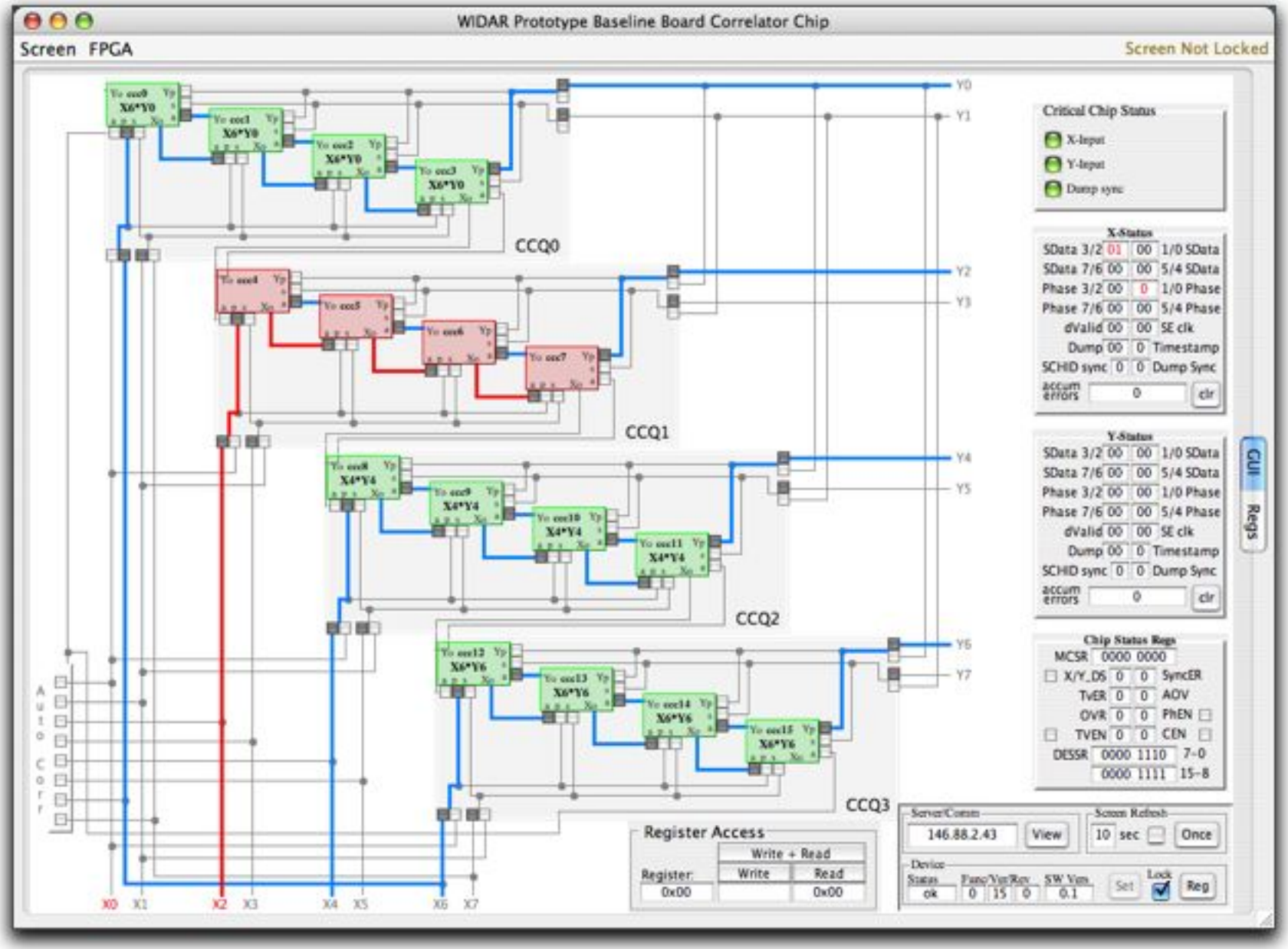
Engineers in Penticton provided detailed diagrams and functional requirements/specifications for the GUIs.

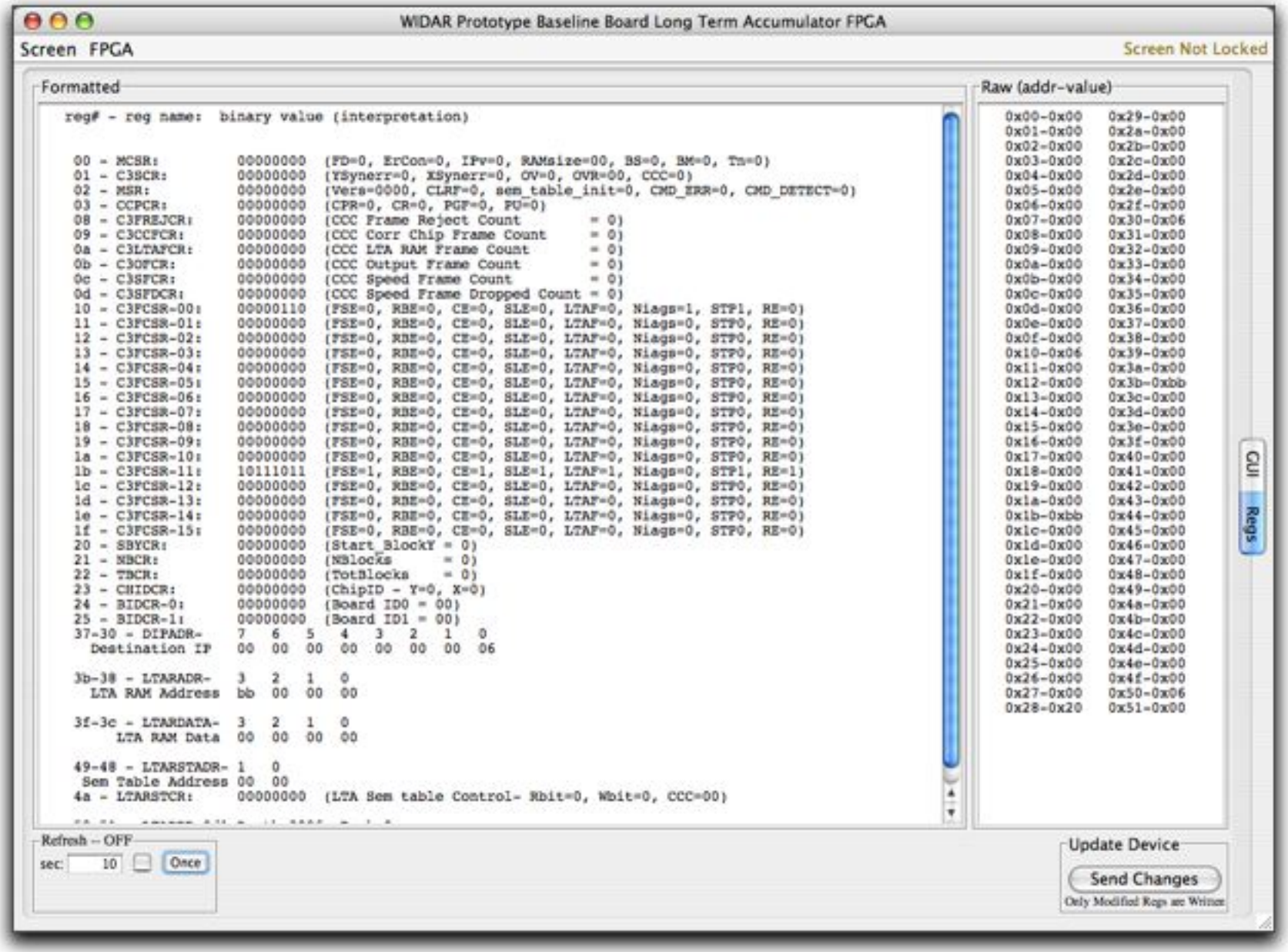


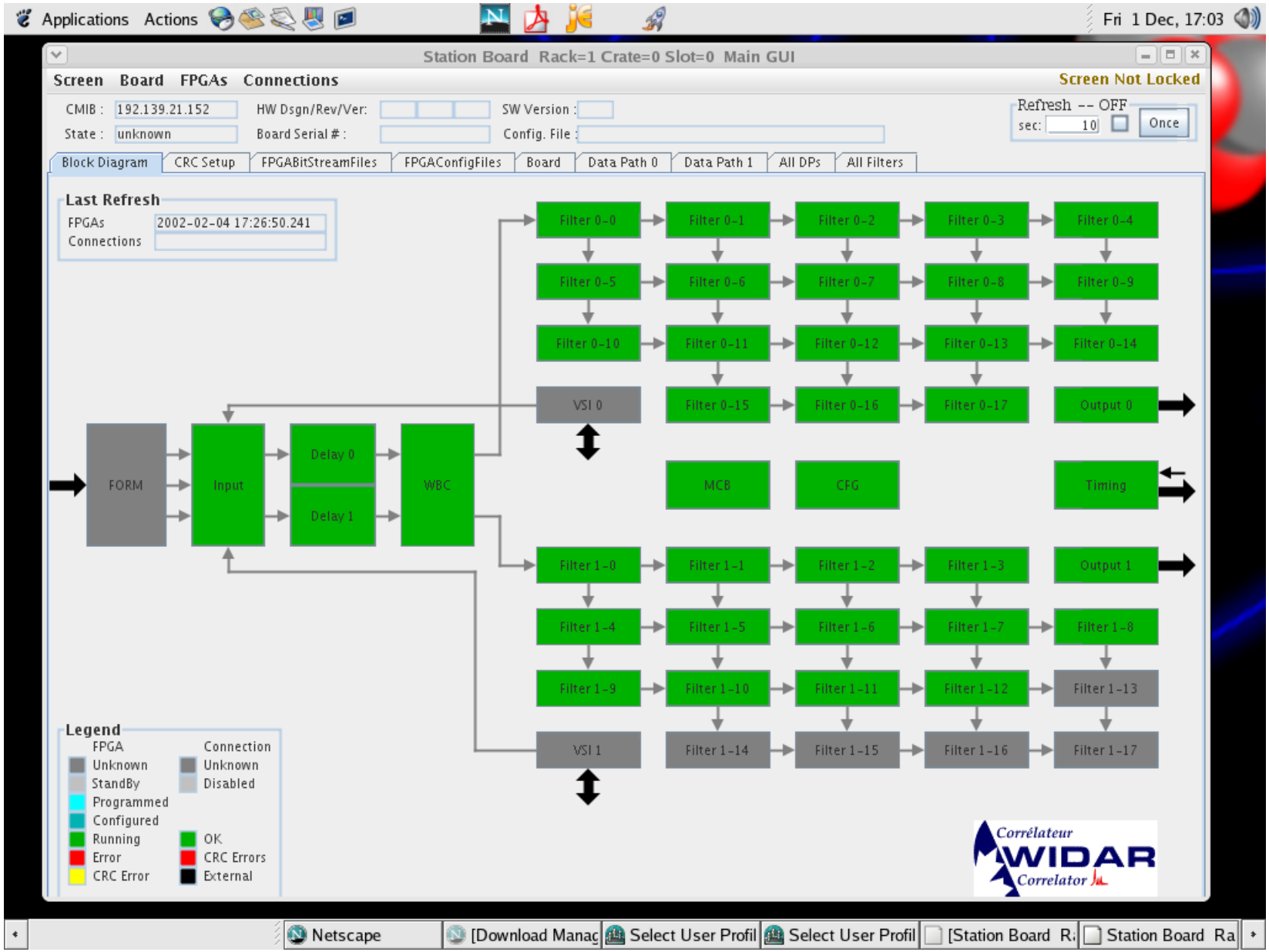
As the prototype boards are undergoing initial testing, the GUIs are also thoroughly being 'wrung-out' for correctness and for modification as necessary.


Prototype Baseline Board test -- 20061201-1531
Screen FPGAs
Block Diagram
CC Files
LTA Files
RC Files
Y-7
Y-6
Y-5
Y-4
Y-3
Y-2
Y-1
Y-0
X-7
X-6
X-5
X-4
X-3
X-2
X-1
X-0
GBit Ethernet
HM Receivers
PCMC
MCB Register Access
Write + Read
Register:
Write
Read
0x00
Master Load File
Read
Load Board
/opt/widar/config/baselineBoard/master.cfg
Server/Comm
146.88.2.43
View
Screen Refresh
10 sec
Once
Device
Status
Fans/Ver/Rev
SW Vers
Set
Lock
Reg


WIDAR Prototype Baseline Board Recirculator FPGA -- Y7
Screen FPGA
Screen Not Locked
HM Gbps Rx
Accum: 1234567 sec
Clr
DumpTrig
Trigger ID Errors 123456
Sync Test Frames 654321
Dump Counts:
TimeCode
UT Time: 2007.213.11.23.25.030
PhaseMod
HM Gbps DPA Receivers:
Enable
Restart
Control Input Source:
Stream / Line / Bit
DUMP_SYNC 7 3
Test Vector off normal
From Station Board Quad
To Correlator Chips
BB Source
Data/Phase
RC Stream
Recirculation active?
Out Sample Rate 256M
X/Y Station X
?Factor?
Blocksize 256
StartBlock 1
EndBlock 255
TotalBlocks 128
Recirculation
Note: Changes to Stream Configuration Circuit
do not take affect until sent via 'Screen' menu.
Register Access
Register:
Write + Read
Write
Read
0x00
GUI
Regs


WIDAR Prototype Baseline Board Correlator Chip
Screen FPGA
Screen Not Locked
CCQ0
CCQ1
CCQ2
CCQ3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
X0
X1
X2
X3
X4
X5
X6
X7
Auto Corr
Critical Chip Status
X-Input
Y-Input
Dump sync
X-Status
SData 3/2 01 00 1/0 SData
SData 7/6 00 00 5/4 SData
Phase 3/2 00 0 1/0 Phase
Phase 7/6 00 00 5/4 Phase
dValid 00 00 SE clk
Dump 00 0 Timestamp
SCHID sync 0 0 Dump Sync
accum errors 0 clr
Y-Status
SData 3/2 00 00 1/0 SData
SData 7/6 00 00 5/4 SData
Phase 3/2 00 00 1/0 Phase
Phase 7/6 00 00 5/4 Phase
dValid 00 00 SE clk
Dump 00 0 Timestamp
SCHID sync 0 0 Dump Sync
accum errors 0 clr
GUI
Regs
Chip Status Regs
MCSR 0000 0000
X/Y_DS 0 0 SyncER
TvER 0 0 AOV
OVR 0 0 PhEN
TVEN 0 0 CEN
DESSR 0000 1110 7-0
0000 1111 15-8
Register Access
Write + Read
Register: Write Read
0x00 0x00
Server/Comm
146.88.2.43 View
Screen Refresh
10 sec Once
Device
Status Fanc/Ver/Rev SW Ver
ok 0 15 0 0.1
Set Lock Reg


WIDAR Prototype Baseline Board Long Term Accumulator FPGA
Screen FPGA
Screen Not Locked
Formatted
reg# - reg name: binary value (interpretation)
00 - MCSR: 00000000 (FD=0, ErCon=0, IPv=0, RAMsize=00, BS=0, BM=0, Tn=0)
01 - C3SCR: 00000000 (YSynerr=0, XSynerr=0, OV=0, OVR=00, CCC=0)
02 - MSR: 00000000 (Vers=0000, CLRF=0, sem_table_init=0, CMD_ERR=0, CMD_DETECT=0)
03 - CCPCR: 00000000 (CPR=0, CR=0, PGF=0, PU=0)
08 - C3FREJCR: 00000000 (CCC Frame Reject Count = 0)
09 - C3CCFCR: 00000000 (CCC Corr Chip Frame Count = 0)
0a - C3LTAFCR: 00000000 (CCC LTA RAM Frame Count = 0)
0b - C3OFCR: 00000000 (CCC Output Frame Count = 0)
0c - C3SFCR: 00000000 (CCC Speed Frame Count = 0)
0d - C3SFDCR: 00000000 (CCC Speed Frame Dropped Count = 0)
10 - C3FCSR-00: 00000110 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=1, STP1, RE=0)
11 - C3FCSR-01: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
12 - C3FCSR-02: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
13 - C3FCSR-03: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
14 - C3FCSR-04: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
15 - C3FCSR-05: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
16 - C3FCSR-06: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
17 - C3FCSR-07: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
18 - C3FCSR-08: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
19 - C3FCSR-09: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
1a - C3FCSR-10: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
1b - C3FCSR-11: 10111011 (FSE=1, RBE=0, CE=1, SLE=1, LTAF=1, Niags=0, STP1, RE=1)
1c - C3FCSR-12: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
1d - C3FCSR-13: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
1e - C3FCSR-14: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
1f - C3FCSR-15: 00000000 (FSE=0, RBE=0, CE=0, SLE=0, LTAF=0, Niags=0, STP0, RE=0)
20 - SBYCR: 00000000 (Start_BlockY = 0)
21 - NBCR: 00000000 (NBlocks = 0)
22 - TBCR: 00000000 (TotBlocks = 0)
23 - CHIDCR: 00000000 (ChipID - Y=0, X=0)
24 - BIDCR-0: 00000000 (Board ID0 = 00)
25 - BIDCR-1: 00000000 (Board ID1 = 00)
37-30 - DIPADR- 7 6 5 4 3 2 1 0
Destination IP 00 00 00 00 00 00 00 06
3b-38 - LTARADR- 3 2 1 0
LTA RAM Address bb 00 00 00
3f-3c - LTARDATA- 3 2 1 0
LTA RAM Data 00 00 00 00
49-48 - LTARSTADR- 1 0
Sem Table Address 00 00
4a - LTARSTCR: 00000000 (LTA Sem table Control- Rbit=0, Wbit=0, CCC=00)
Raw (addr-value)
0x00-0x00 0x29-0x00
0x01-0x00 0x2a-0x00
0x02-0x00 0x2b-0x00
0x03-0x00 0x2c-0x00
0x04-0x00 0x2d-0x00
0x05-0x00 0x2e-0x00
0x06-0x00 0x2f-0x00
0x07-0x00 0x30-0x06
0x08-0x00 0x31-0x00
0x09-0x00 0x32-0x00
0x0a-0x00 0x33-0x00
0x0b-0x00 0x34-0x00
0x0c-0x00 0x35-0x00
0x0d-0x00 0x36-0x00
0x0e-0x00 0x37-0x00
0x0f-0x00 0x38-0x00
0x10-0x06 0x39-0x00
0x11-0x00 0x3a-0x00
0x12-0x00 0x3b-0xbb
0x13-0x00 0x3c-0x00
0x14-0x00 0x3d-0x00
0x15-0x00 0x3e-0x00
0x16-0x00 0x3f-0x00
0x17-0x00 0x40-0x00
0x18-0x00 0x41-0x00
0x19-0x00 0x42-0x00
0x1a-0x00 0x43-0x00
0x1b-0xbb 0x44-0x00
0x1c-0x00 0x45-0x00
0x1d-0x00 0x46-0x00
0x1e-0x00 0x47-0x00
0x1f-0x00 0x48-0x00
0x20-0x00 0x49-0x00
0x21-0x00 0x4a-0x00
0x22-0x00 0x4b-0x00
0x23-0x00 0x4c-0x00
0x24-0x00 0x4d-0x00
0x25-0x00 0x4e-0x00
0x26-0x00 0x4f-0x00
0x27-0x00 0x50-0x06
0x28-0x20 0x51-0x00
GUI
Regs
Refresh -- OFF
sec: 10
Once
Update Device
Send Changes
Only Modified Regs are Written


Applications Actions
Fri 1 Dec, 17:03
Station Board Rack=1 Crate=0 Slot=0 Main GUI
Screen Board FPGAs Connections
Screen Not Locked
CMIB : 192.139.21.152
State : unknown
HW Dsgn/Rev/Ver:
Board Serial # :
SW Version :
Config. File :
Refresh -- OFF
sec: 10
Once
Block Diagram
CRC Setup
FPGABitStreamFiles
FPGAConfigFiles
Board
Data Path 0
Data Path 1
All DPs
All Filters
Last Refresh
FPGAs 2002-02-04 17:26:50.241
Connections
Filter 0-0
Filter 0-1
Filter 0-2
Filter 0-3
Filter 0-4
Filter 0-5
Filter 0-6
Filter 0-7
Filter 0-8
Filter 0-9
Filter 0-10
Filter 0-11
Filter 0-12
Filter 0-13
Filter 0-14
VSI 0
Filter 0-15
Filter 0-16
Filter 0-17
Output 0
FORM
Input
Delay 0
Delay 1
WBC
MCB
CFG
Timing
Filter 1-0
Filter 1-1
Filter 1-2
Filter 1-3
Output 1
Filter 1-4
Filter 1-5
Filter 1-6
Filter 1-7
Filter 1-8
Filter 1-9
Filter 1-10
Filter 1-11
Filter 1-12
Filter 1-13
VSI 1
Filter 1-14
Filter 1-15
Filter 1-16
Filter 1-17
Legend
FPGA
Unknown
StandBy
Programmed
Configured
Running
Error
CRC Error
Connection
Unknown
Disabled
OK
CRC Errors
External
Corrélateur
WIDAR
Correlator
Netscape
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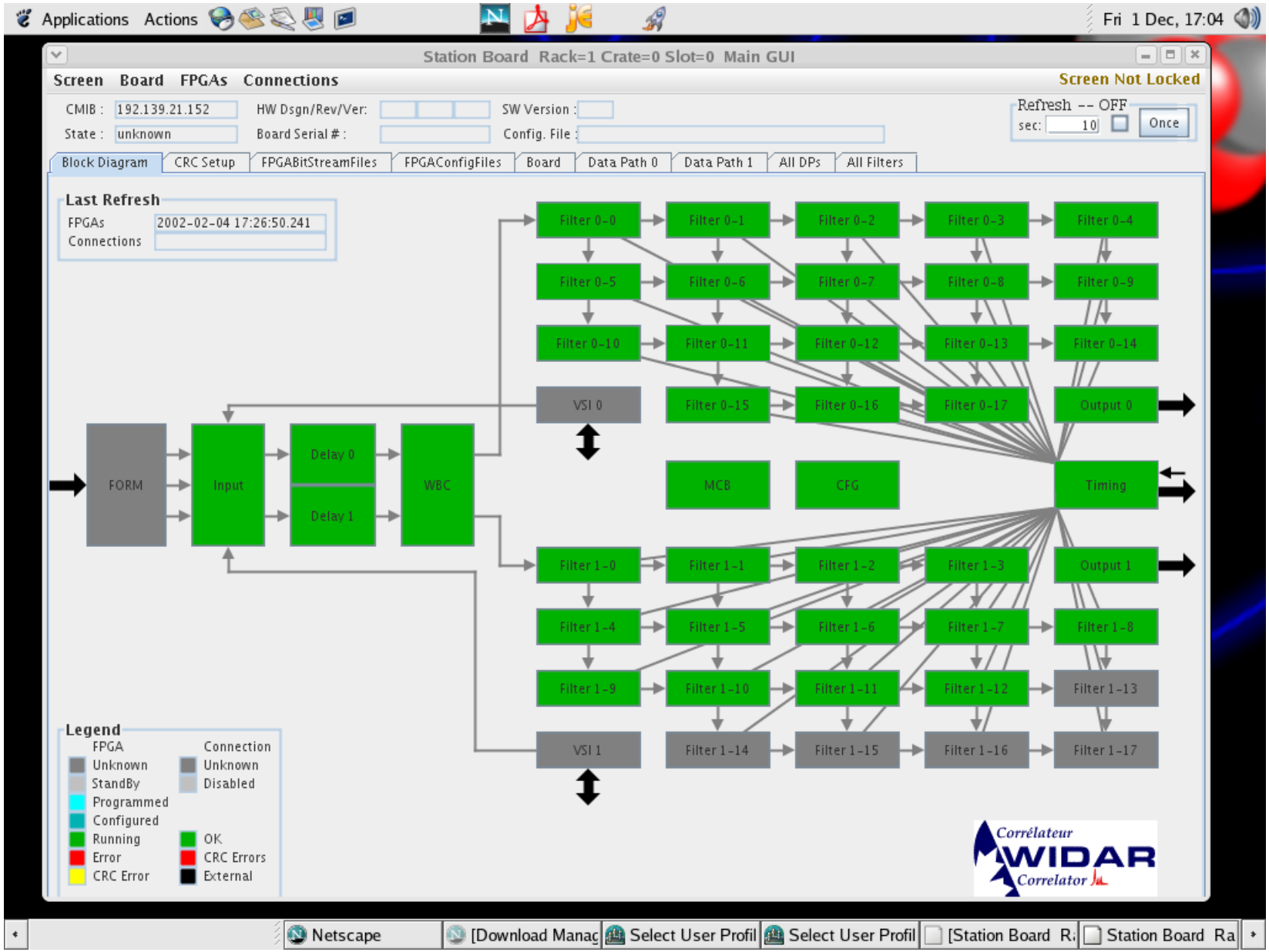
[Station Board R
Station Board Ra


Applications Actions
Fri 1 Dec, 17:04
Station Board Rack=1 Crate=0 Slot=0 Main GUI
Screen Board FPGAs Connections
Screen Not Locked
CMIB : 192.139.21.152
State : unknown
HW Dsgn/Rev/Ver:
Board Serial # :
SW Version :
Config. File :
Refresh -- OFF
sec: 10
Once
Block Diagram
CRC Setup
FPGABitStreamFiles
FPGAConfigFiles
Board
Data Path 0
Data Path 1
All DPs
All Filters
Last Refresh
FPGAs 2002-02-04 17:26:50.241
Connections
FORM
Input
Delay 0
Delay 1
WBC
VSI 0
VSI 1
MCB
CFG
Timing
Output 0
Output 1
Filter 0-0
Filter 0-1
Filter 0-2
Filter 0-3
Filter 0-4
Filter 0-5
Filter 0-6
Filter 0-7
Filter 0-8
Filter 0-9
Filter 0-10
Filter 0-11
Filter 0-12
Filter 0-13
Filter 0-14
Filter 0-15
Filter 0-16
Filter 0-17
Filter 1-0
Filter 1-1
Filter 1-2
Filter 1-3
Filter 1-4
Filter 1-5
Filter 1-6
Filter 1-7
Filter 1-8
Filter 1-9
Filter 1-10
Filter 1-11
Filter 1-12
Filter 1-13
Filter 1-14
Filter 1-15
Filter 1-16
Filter 1-17
Legend
FPGA
Unknown
StandBy
Programmed
Configured
Running
Error
CRC Error
Connection
Unknown
Disabled
OK
CRC Errors
External
Corrélateur
WIDAR
Correlator
Netscape
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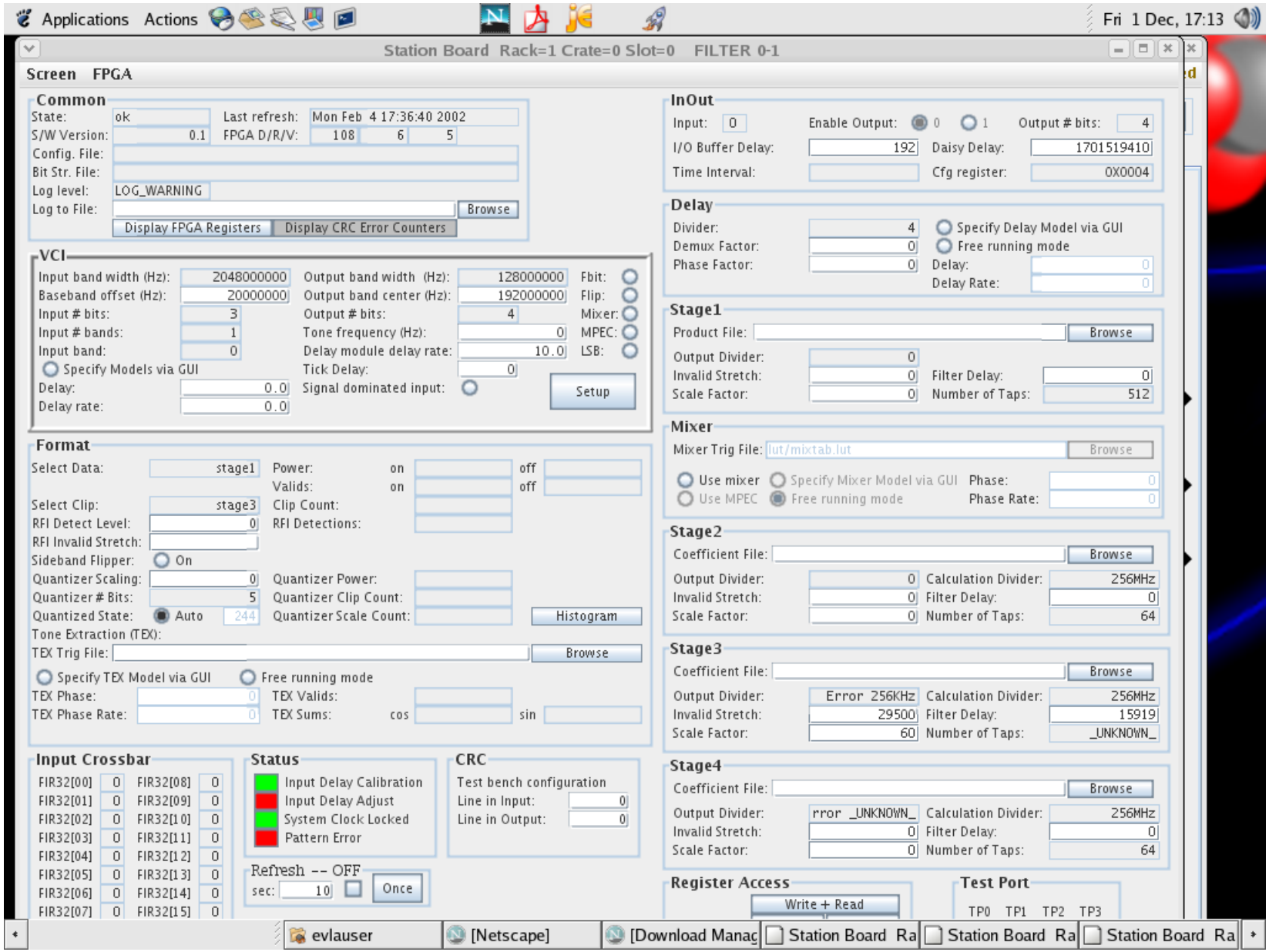
Applications Actions
Fri 1 Dec, 17:13
Station Board Rack=1 Crate=0 Slot=0 FILTER 0-1
Screen FPGA
Common
State: ok
Last refresh: Mon Feb 4 17:36:40 2002
S/W Version: 0.1
FPGA D/R/V: 108 6 5
Config. File:
Bit Str. File:
Log level: LOG_WARNING
Log to File:
Browse
Display FPGA Registers
Display CRC Error Counters
VCI
Input band width (Hz): 2048000000
Baseband offset (Hz): 20000000
Input # bits: 3
Input # bands: 1
Input band: 0
Specify Models via GUI
Delay: 0.0
Delay rate: 0.0
Output band width (Hz): 128000000
Output band center (Hz): 192000000
Output # bits: 4
Tone frequency (Hz): 0
Delay module delay rate: 10.0
Tick Delay: 0
Signal dominated input:
Fbit:
Flip:
Mixer:
MPEC:
LSB:
Setup
Format
Select Data: stage1
Power: on off
Valids: on off
Select Clip: stage3
Clip Count:
RFI Detect Level: 0
RFI Detections:
RFI Invalid Stretch:
Sideband Flipper: On
Quantizer Scaling: 0
Quantizer Power:
Quantizer # Bits: 5
Quantizer Clip Count:
Quantized State: Auto 244
Quantizer Scale Count:
Histogram
Tone Extraction (TEX):
TEX Trig File:
Browse
Specify TEX Model via GUI
Free running mode
TEX Phase: 0
TEX Phase Rate: 0
TEX Valids:
TEX Sums: cos sin
Input Crossbar
FIR32[00] 0 FIR32[08] 0
FIR32[01] 0 FIR32[09] 0
FIR32[02] 0 FIR32[10] 0
FIR32[03] 0 FIR32[11] 0
FIR32[04] 0 FIR32[12] 0
FIR32[05] 0 FIR32[13] 0
FIR32[06] 0 FIR32[14] 0
FIR32[07] 0 FIR32[15] 0
Status
Input Delay Calibration
Input Delay Adjust
System Clock Locked
Pattern Error
Refresh -- OFF
sec: 10
Once
CRC
Test bench configuration
Line in Input: 0
Line in Output: 0
InOut
Input: 0
Enable Output: 0 1
Output # bits: 4
I/O Buffer Delay: 192
Daisy Delay: 1701519410
Time Interval:
Cfg register: 0X0004
Delay
Divider: 4
Demux Factor: 0
Phase Factor: 0
Specify Delay Model via GUI
Free running mode
Delay: 0
Delay Rate: 0
Stage1
Product File:
Browse
Output Divider: 0
Invalid Stretch: 0
Scale Factor: 0
Filter Delay: 0
Number of Taps: 512
Mixer
Mixer Trig File: lut/mixtab.lut
Browse
Use mixer
Use MPEC
Specify Mixer Model via GUI
Free running mode
Phase: 0
Phase Rate: 0
Stage2
Coefficient File:
Browse
Output Divider: 0
Invalid Stretch: 0
Scale Factor: 0
Calculation Divider: 256MHz
Filter Delay: 0
Number of Taps: 64
Stage3
Coefficient File:
Browse
Output Divider: Error 256KHz
Invalid Stretch: 29500
Scale Factor: 60
Calculation Divider: 256MHz
Filter Delay: 15919
Number of Taps: _UNKNOWN_
Stage4
Coefficient File:
Browse
Output Divider: rror _UNKNOWN_
Invalid Stretch: 0
Scale Factor: 0
Calculation Divider: 256MHz
Filter Delay: 0
Number of Taps: 64
Register Access
Write + Read
Test Port
TP0 TP1 TP2 TP3
evlauser
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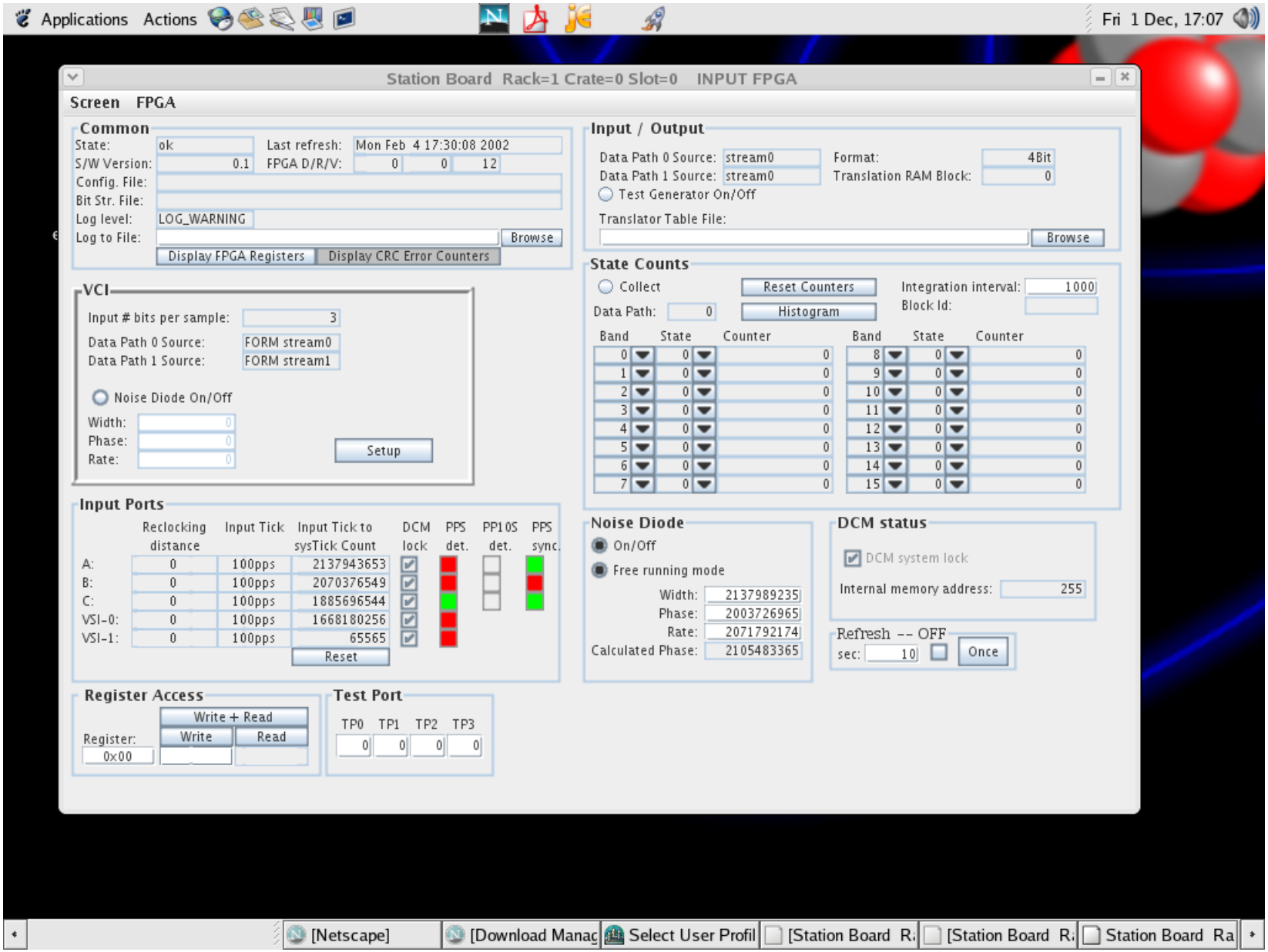
Applications Actions
Fri 1 Dec, 17:07
Station Board Rack=1 Crate=0 Slot=0 INPUT FPGA
Screen FPGA
Common
State: ok
Last refresh: Mon Feb 4 17:30:08 2002
S/W Version: 0.1
FPGA D/R/V: 0 0 12
Config. File:
Bit Str. File:
Log level: LOG_WARNING
Log to File:
Browse
Display FPGA Registers
Display CRC Error Counters
VCI
Input # bits per sample: 3
Data Path 0 Source: FORM stream0
Data Path 1 Source: FORM stream1
Noise Diode On/Off
Width:
Phase:
Rate:
Setup
Input Ports
Reclocking distance
Input Tick
Input Tick to sysTick Count
DCM lock
PPS det.
PP10S det.
PPS sync
A: 0 100pps 2137943653
B: 0 100pps 2070376549
C: 0 100pps 1885696544
VSI-0: 0 100pps 1668180256
VSI-1: 0 100pps 65565
Reset
Register Access
Write + Read
Register:
Write
Read
0x00
Test Port
TP0 TP1 TP2 TP3
0 0 0 0
Input / Output
Data Path 0 Source: stream0
Format: 4Bit
Data Path 1 Source: stream0
Translation RAM Block: 0
Test Generator On/Off
Translator Table File:
Browse
State Counts
Collect
Reset Counters
Integration interval: 1000
Data Path: 0
Histogram
Block Id:
Band State Counter
Noise Diode
On/Off
Free running mode
Width: 2137989235
Phase: 2003726965
Rate: 2071792174
Calculated Phase: 2105483365
DCM status
DCM system lock
Internal memory address: 255
Refresh -- OFF
sec: 10
Once
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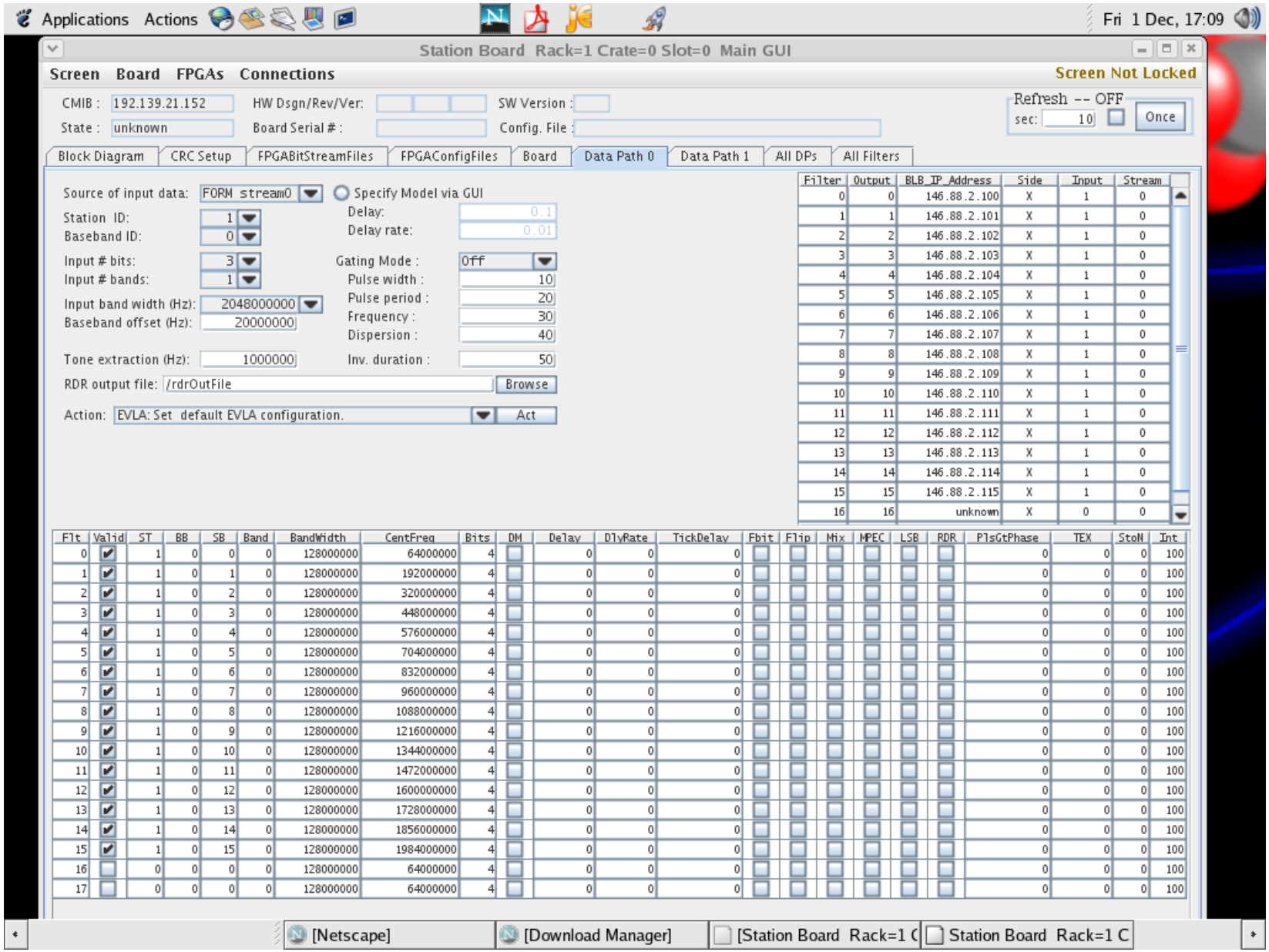
Applications Actions
Fri 1 Dec, 17:09
Station Board Rack=1 Crate=0 Slot=0 Main GUI
Screen Board FPGAs Connections
Screen Not Locked
CMIB : 192.139.21.152
HW Dsgn/Rev/Ver:
SW Version :
State : unknown
Board Serial # :
Config. File :
Refresh -- OFF
sec: 10
Once
Block Diagram
CRC Setup
FPGABitStreamFiles
FPGAConfigFiles
Board
Data Path 0
Data Path 1
All DPs
All Filters
Source of input data: FORM stream0
Specify Model via GUI
Station ID: 1
Baseband ID: 0
Delay: 0.1
Delay rate: 0.01
Input # bits: 3
Input # bands: 1
Gating Mode : Off
Pulse width : 10
Pulse period : 20
Input band width (Hz): 2048000000
Baseband offset (Hz): 20000000
Frequency : 30
Dispersion : 40
Tone extraction (Hz): 1000000
Inv. duration : 50
RDR output file: /rdrOutFile
Browse
Action: EVLA: Set default EVLA configuration.
Act
Filter Output BLB_IP_Address Side Input Stream
0 0 146.88.2.100 X 1 0
1 1 146.88.2.101 X 1 0
2 2 146.88.2.102 X 1 0
3 3 146.88.2.103 X 1 0
4 4 146.88.2.104 X 1 0
5 5 146.88.2.105 X 1 0
6 6 146.88.2.106 X 1 0
7 7 146.88.2.107 X 1 0
8 8 146.88.2.108 X 1 0
9 9 146.88.2.109 X 1 0
10 10 146.88.2.110 X 1 0
11 11 146.88.2.111 X 1 0
12 12 146.88.2.112 X 1 0
13 13 146.88.2.113 X 1 0
14 14 146.88.2.114 X 1 0
15 15 146.88.2.115 X 1 0
16 16 unknown X 0 0
Flt Valid ST BB SB Band BandWidth CentFreq Bits DM Delay DlyRate TickDelay Fbit Flip Mix MPEC LSB RDR PlsGtPhase TEX StoN Int
0 1 0 0 0 128000000 64000000 4 0 0 0 0 0 0 0 0 0 0 0 100
1 1 0 1 0 128000000 192000000 4 0 0 0 0 0 0 0 0 0 0 0 100
2 1 0 2 0 128000000 320000000 4 0 0 0 0 0 0 0 0 0 0 0 100
3 1 0 3 0 128000000 448000000 4 0 0 0 0 0 0 0 0 0 0 0 100
4 1 0 4 0 128000000 576000000 4 0 0 0 0 0 0 0 0 0 0 0 100
5 1 0 5 0 128000000 704000000 4 0 0 0 0 0 0 0 0 0 0 0 100
6 1 0 6 0 128000000 832000000 4 0 0 0 0 0 0 0 0 0 0 0 100
7 1 0 7 0 128000000 960000000 4 0 0 0 0 0 0 0 0 0 0 0 100
8 1 0 8 0 128000000 1088000000 4 0 0 0 0 0 0 0 0 0 0 0 100
9 1 0 9 0 128000000 1216000000 4 0 0 0 0 0 0 0 0 0 0 0 100
10 1 0 10 0 128000000 1344000000 4 0 0 0 0 0 0 0 0 0 0 0 100
11 1 0 11 0 128000000 1472000000 4 0 0 0 0 0 0 0 0 0 0 0 100
12 1 0 12 0 128000000 1600000000 4 0 0 0 0 0 0 0 0 0 0 0 100
13 1 0 13 0 128000000 1728000000 4 0 0 0 0 0 0 0 0 0 0 0 100
14 1 0 14 0 128000000 1856000000 4 0 0 0 0 0 0 0 0 0 0 0 100
15 1 0 15 0 128000000 1984000000 4 0 0 0 0 0 0 0 0 0 0 0 100
16 0 0 0 0 128000000 64000000 4 0 0 0 0 0 0 0 0 0 0 0 100
17 0 0 0 0 128000000 64000000 4 0 0 0 0 0 0 0 0 0 0 0 100
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[Station Board Rack=1 C
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