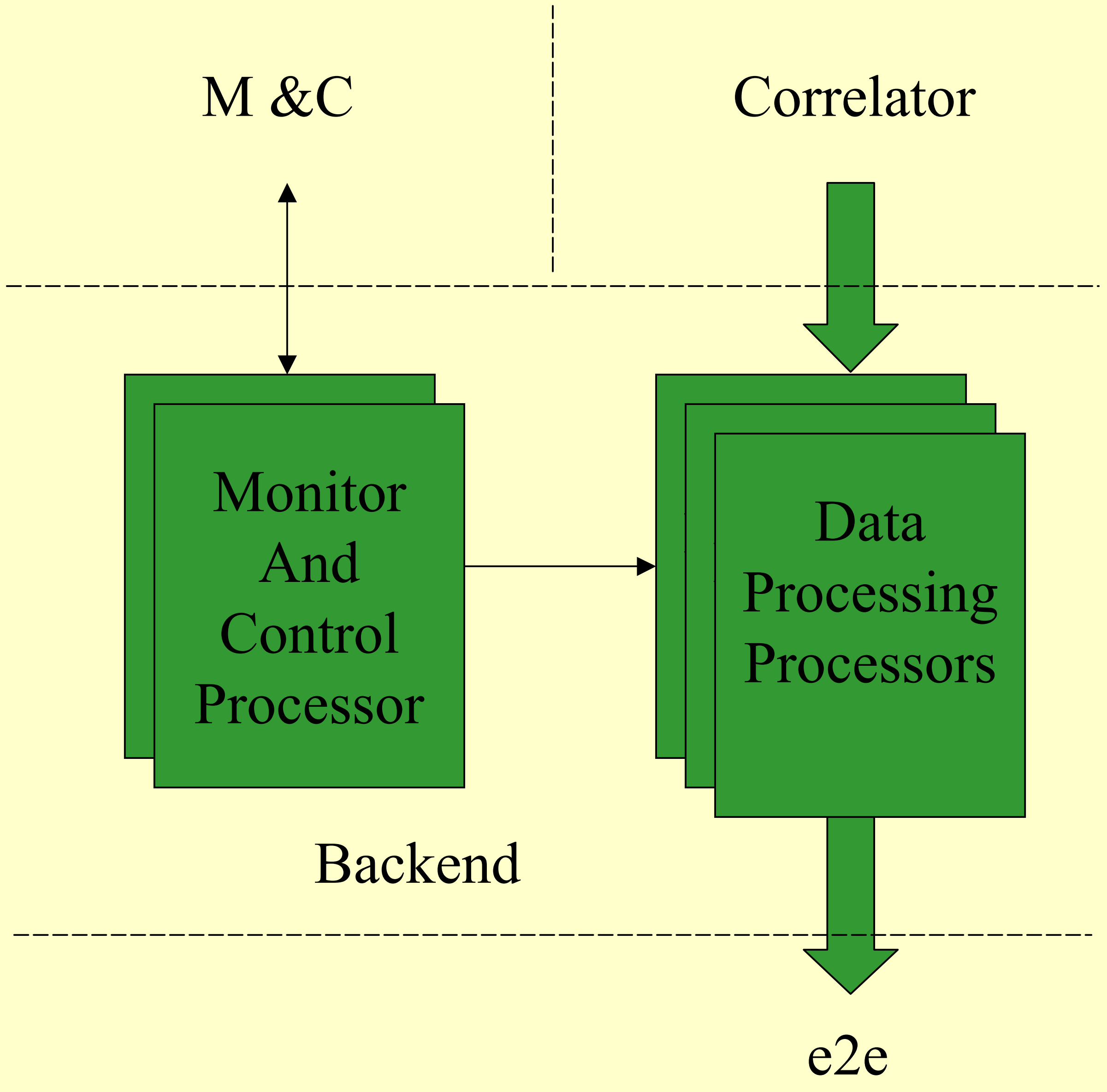
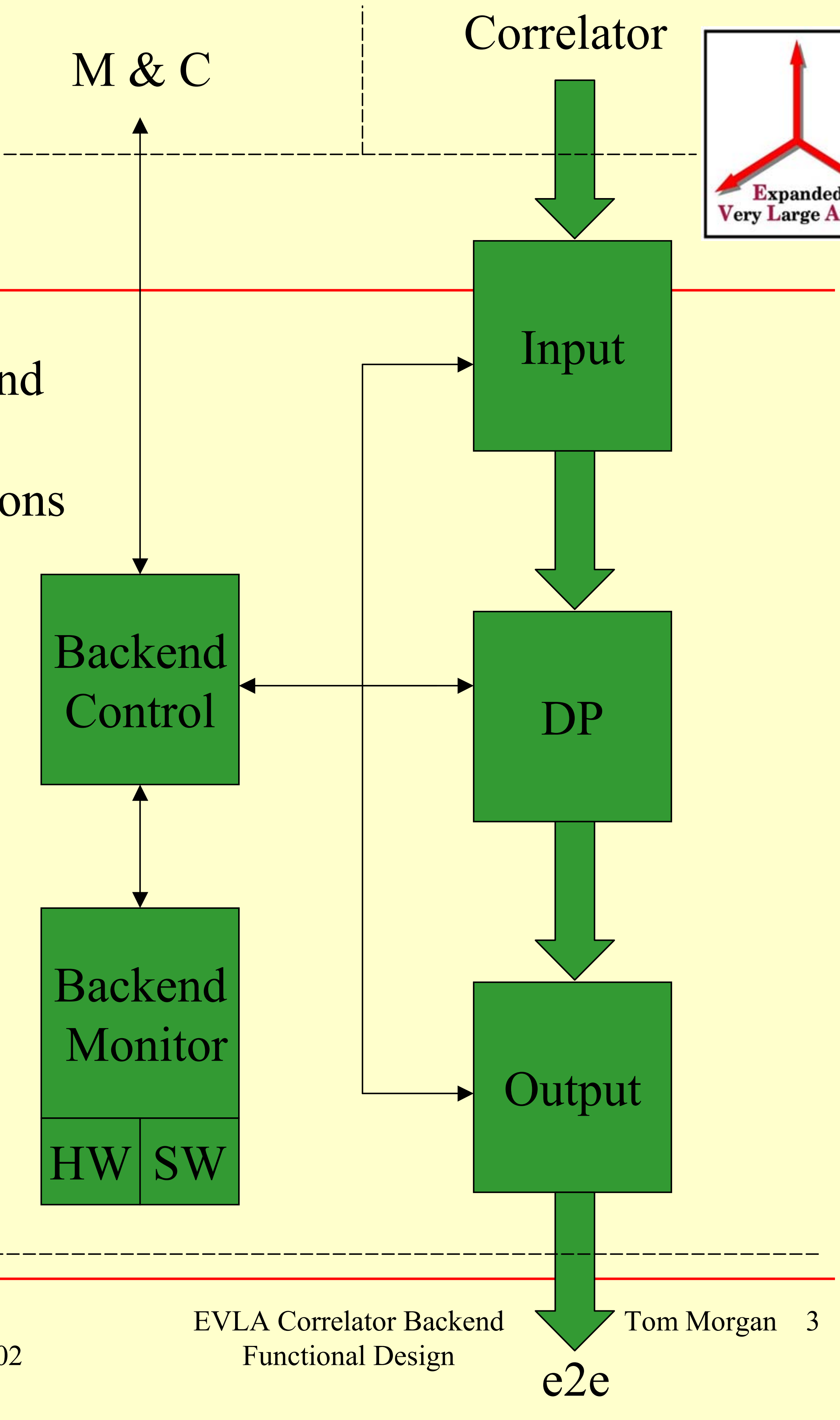
Backend Preliminary Functional Design

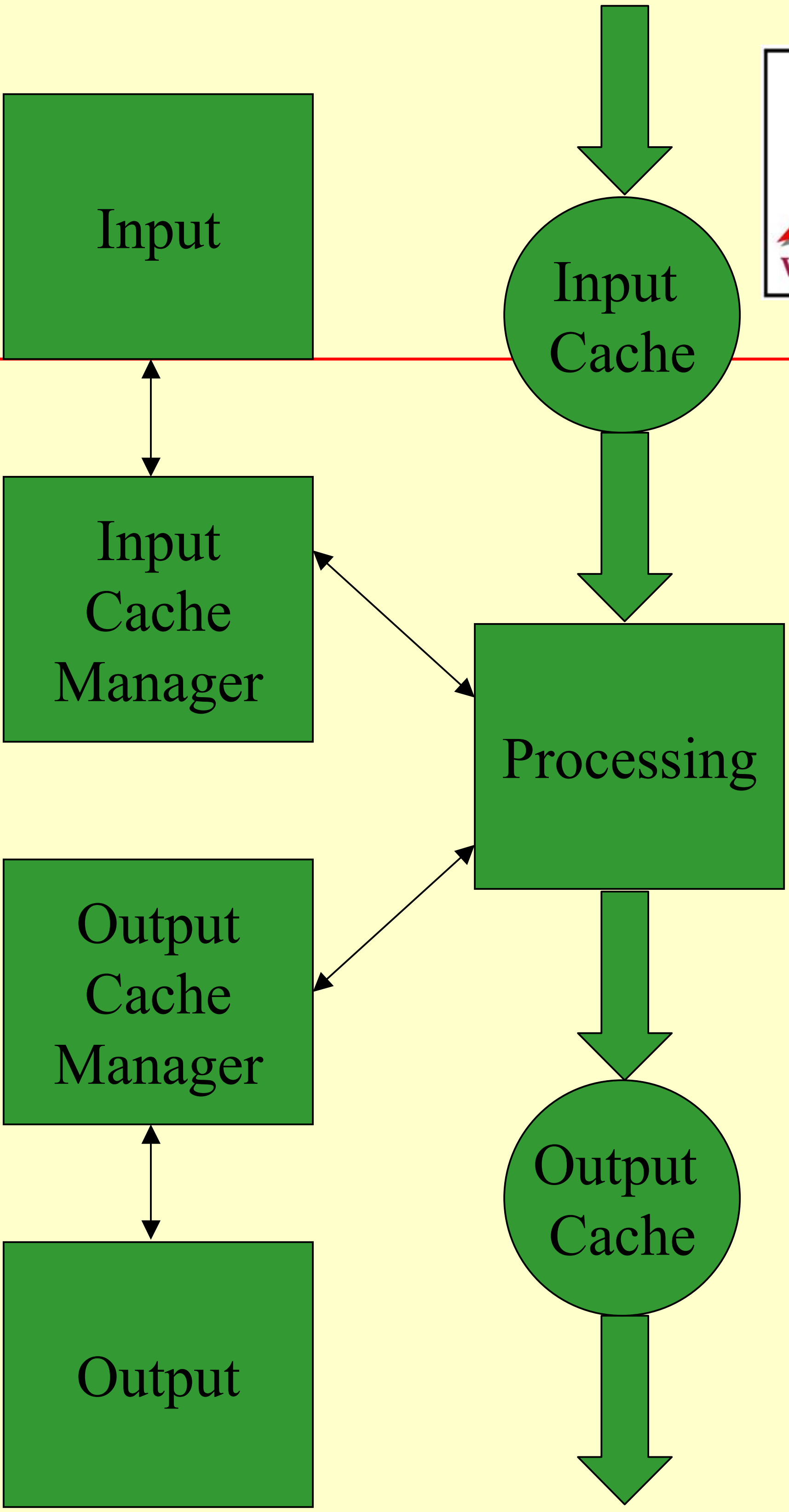
BACKEND CLUSTER ORGANIZATION



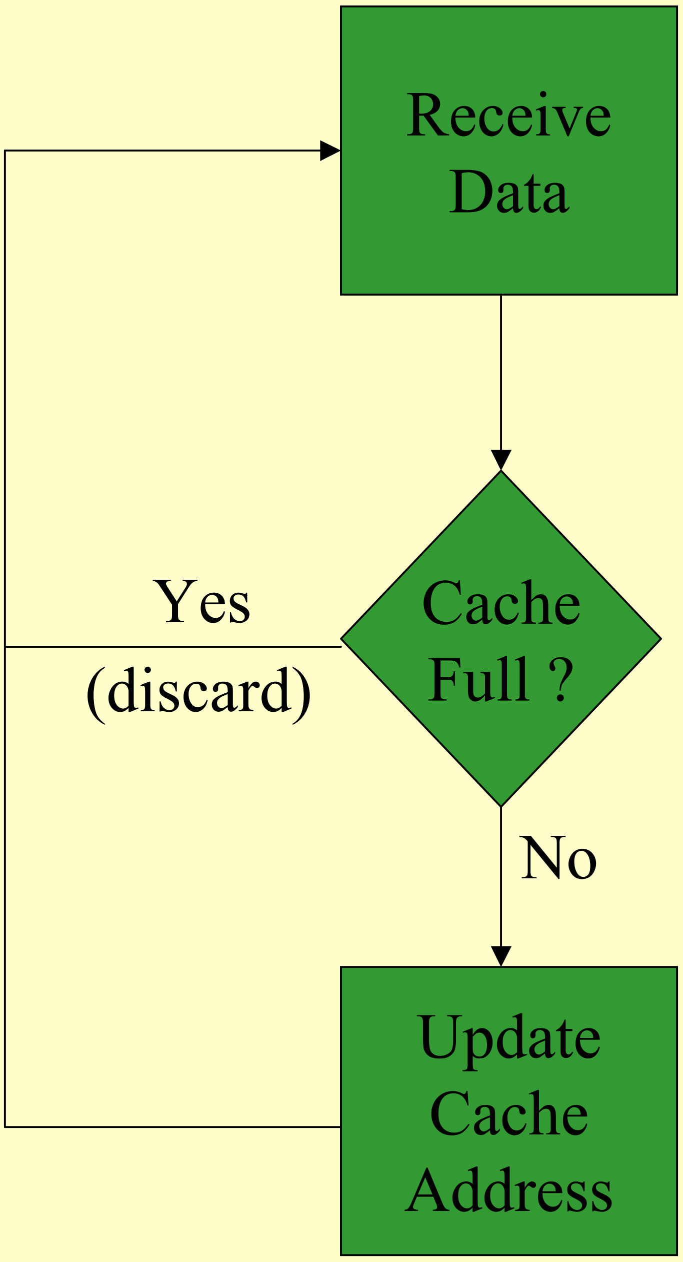
Backend Major Functions



Five DP Node Processes, Control And Data Flows



Input Process



Input

- Provides Large Memory Area for Depositing Incoming Lag Frame Data
- Signals When Segment is Full
- Immediately Moves to Next Segment
- Discards New Input When Memory is Full
- Bare Minimum Overhead

Input Cache

- Three Shared Memory Data Structures
- Accessible by Input, Input Cache Manager and DP Processes
- Input Cache Lag Frame Store
- Cache Segment List
- Lag Set Tables

INPUT CACHE
LAG FRAME STORE

Frame Index	LTA Frame Data
1	
2	
. . .	. . .
1000	
1001	
1002	
. . .	. . .
2000	
2001	
2002	
. . .	. . .
2999	Lag Set N 1, Frame 1
3000	Lag Set N+1, Frame 1
3001	Lag Set N, Frame 3
3002	Lag Set N, Frame 2
3003	Lag Set N+1, Frame 2
3004	Lag Set N+1, Frame 3
. . .	. . .
3017	Lag Set N, Frame 6
3018	Lag Set N+3, Frame 1
3019	Lag Set N, Frame 5
3020	Lag Set N+3, Frame 2
. . .	. . .
4000	
4001	
. . .	. . .
10000	

Segment 1

Segment 2

Segment 3

Segment 4

Segments 4 to 10

Lag Frame Store

- Written only by Input Process
- Read by Input Cache Manager and DP Processes
- Divided into a Limited number of Large Segments
- Input Writes to Entire Segment at One Time

LAG SET TABLE

(8 lag frames X 128 lags per frame = 1024 lags per lag set)

Lag Set Number	Integration Block	Skip Count	Lag Count	Lag Frame Indices							
1											
2											
3											
. . .	. . .	. . .	. . .				. . .				
N	K	1	8	2999	3002	3001	3003	3007	3008	3019	3017
N+1	K+1	0	8	3000	3004	3005	3006	3011	3012	3013	3014
N+2	K	0	4	3009	3010	3015	3016				
N+3	K+1	0	2	3018	3020						
. . .	. . .	. . .					. . .				

SEGMENT LIST

Segment Number	Frame Count
1	0
2	119
3	1000
4	1000
5	1000
6	0
7	0
8	0
9	0
10	0

Segment List

- Contains Status Data (Frame Count) on Lag Frame Store Segments
- Written by Input and DP
- Read by Input, Input Cache Manager and DP
- Frame Count Value of Zero Means Available for New Input
- Non-Zero Status Means in DP or Awaiting DP

Lag Set Table

- Sorted Addresses of Lag Frames Making-up a Single Lag Set
- Written Only by Input Cache Manager
- Read Only by DP
- Integration Block, Skip Count and Lag Count Auxiliary Data Columns

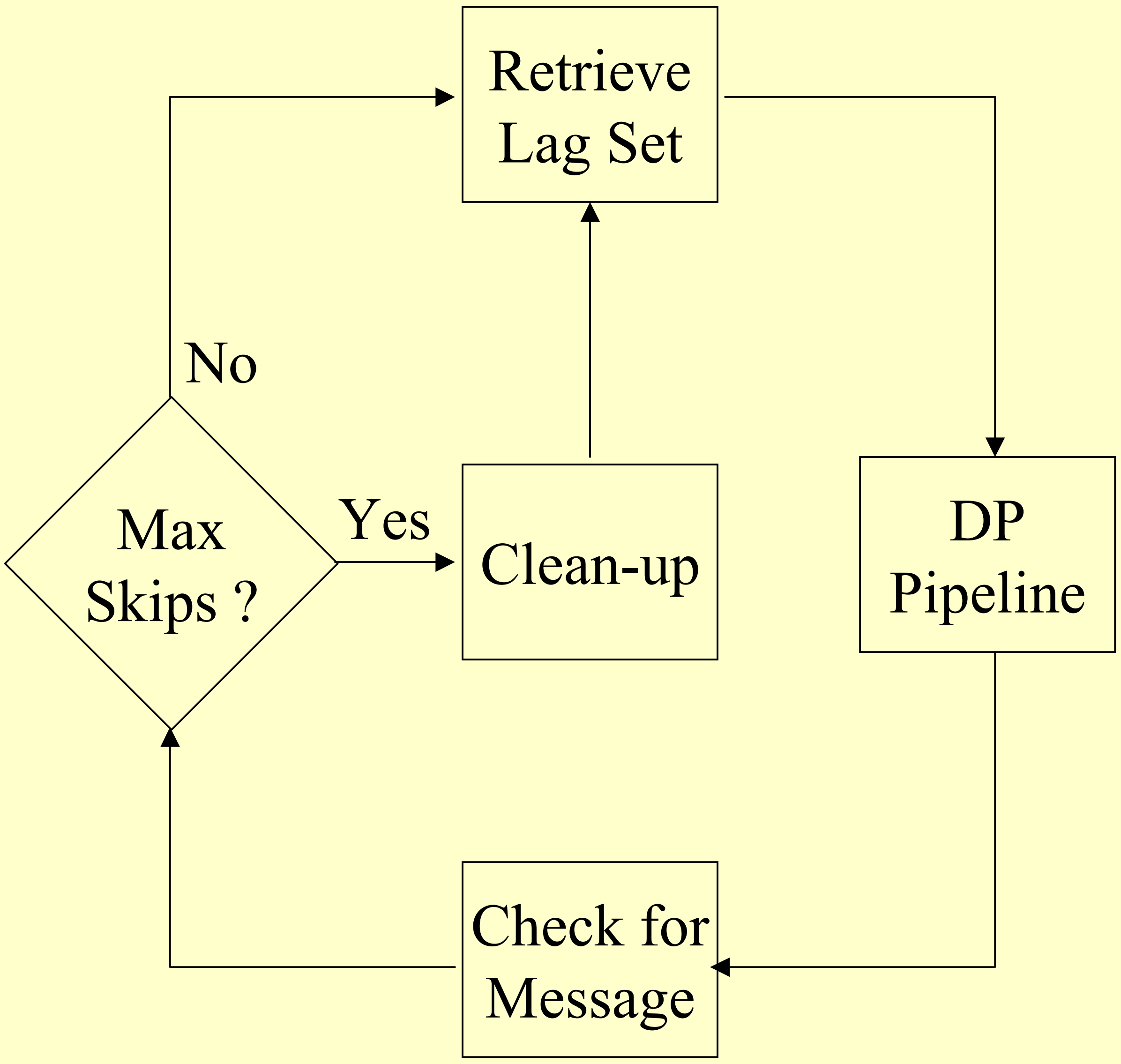
Lag Set Table

- Integration Block Identifies all Lag Sets in the Same Integration Sequence
- Skip Count Registers Number of Times a Lag Set has been Passed by
- Lag Count Maintains a Record of the Number of Indices That Have Been Sorted into the Table

Input Cache Manager

- Reads Lag Frames From Lag Frame Store
- Updates Lag Frame Index Entries in Lag Set Table
- Updates Lag Set, Lag Count Entries
- Monitors Number of Segments Available for Input

Data Processing Loop



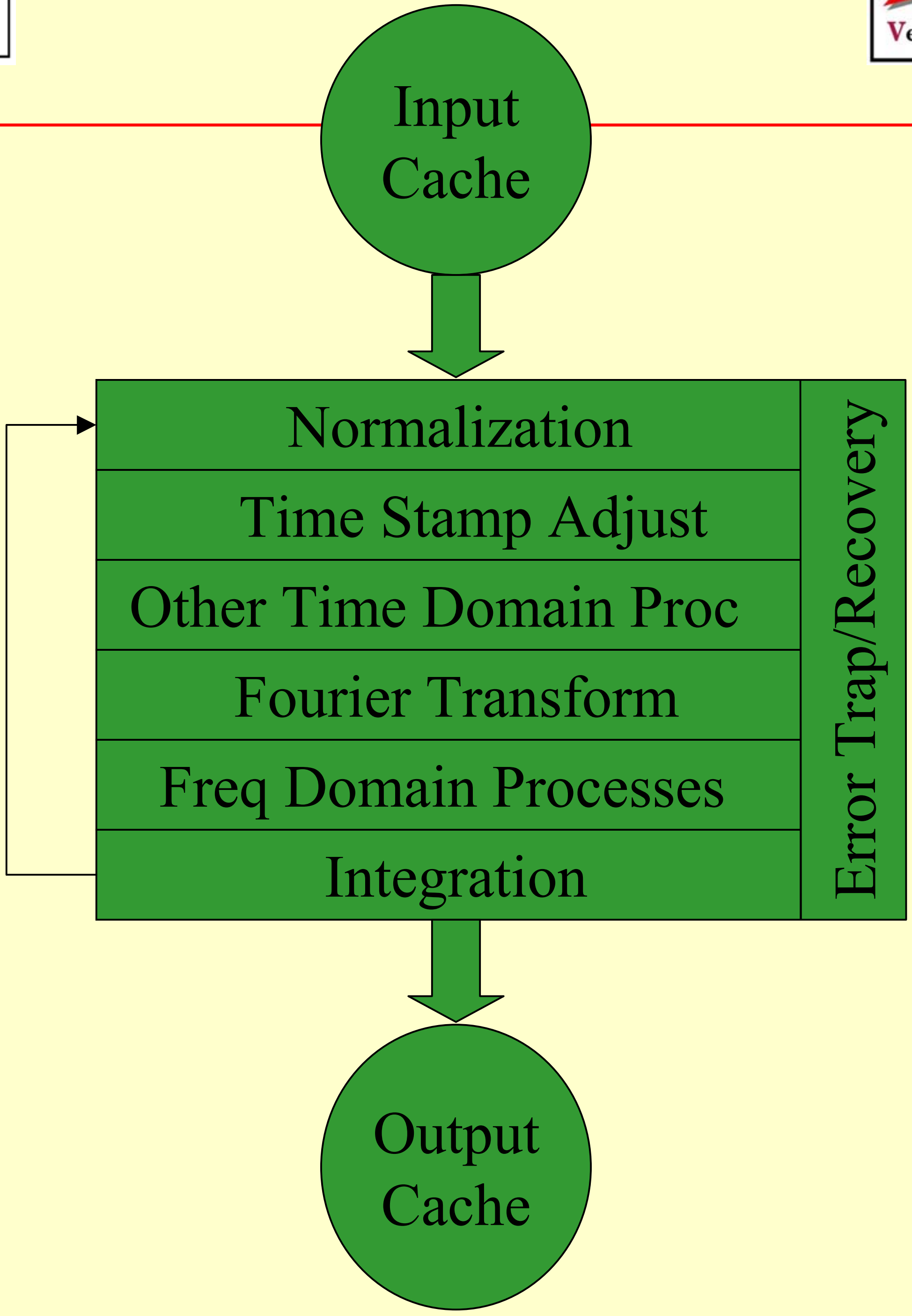
Data Processing Overview

- Read Lag Frames Using Lag Set Table Indices
- Check for Availability of Auxiliary Data
- DP Pipeline
- Incoming Message Check
- Clean-up of Skipped Lag Sets

Lag Frame Read

- Access Only Lag Sets with Full Lag Counts
- Access Only Lag Sets with Available State Counts
- Lag Frame Index Points to Lag Frame Store Location
- Indices Are In Order of Assembly
- Increment Skip Count for Those That Do Not Yet Qualify

Processing Pipeline Detail



DP Pipeline

- Apply Normalization
- Update Time Stamps (Recirculation)
- Possible Additional Time Domain Applications
- Fourier Transform (Complex-Complex, Power of 2 FFT)
- Possible Frequency Domain Applications
- Accumulate
- Move to Output Cache

Incoming Messages

- Mode Change
- State Counts
- Shutdown/Resume
- Always Received From BE Control

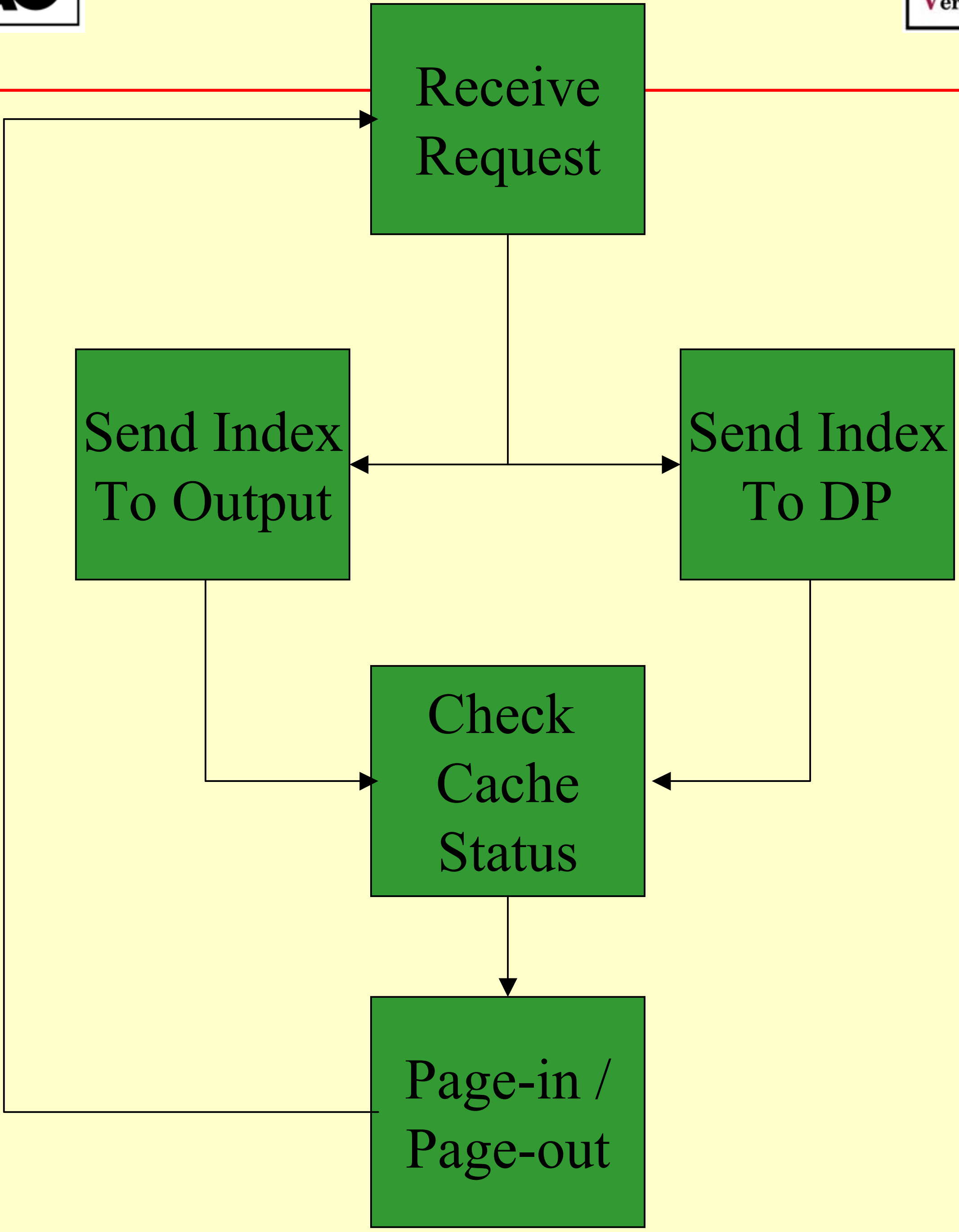
Cleanup

- Periodic Check of Skipped Lag Sets
- Process Those That are Now Ready
- Increment Skip Count for Those That are Still Not Ready
- Discard Those That are Too Old (Rare)

Output Cache

- Shared Memory Array
- Disk Backup for Paging
- Accessible by DP, Output and Output Cache Manager Processes

Output Cache Manager



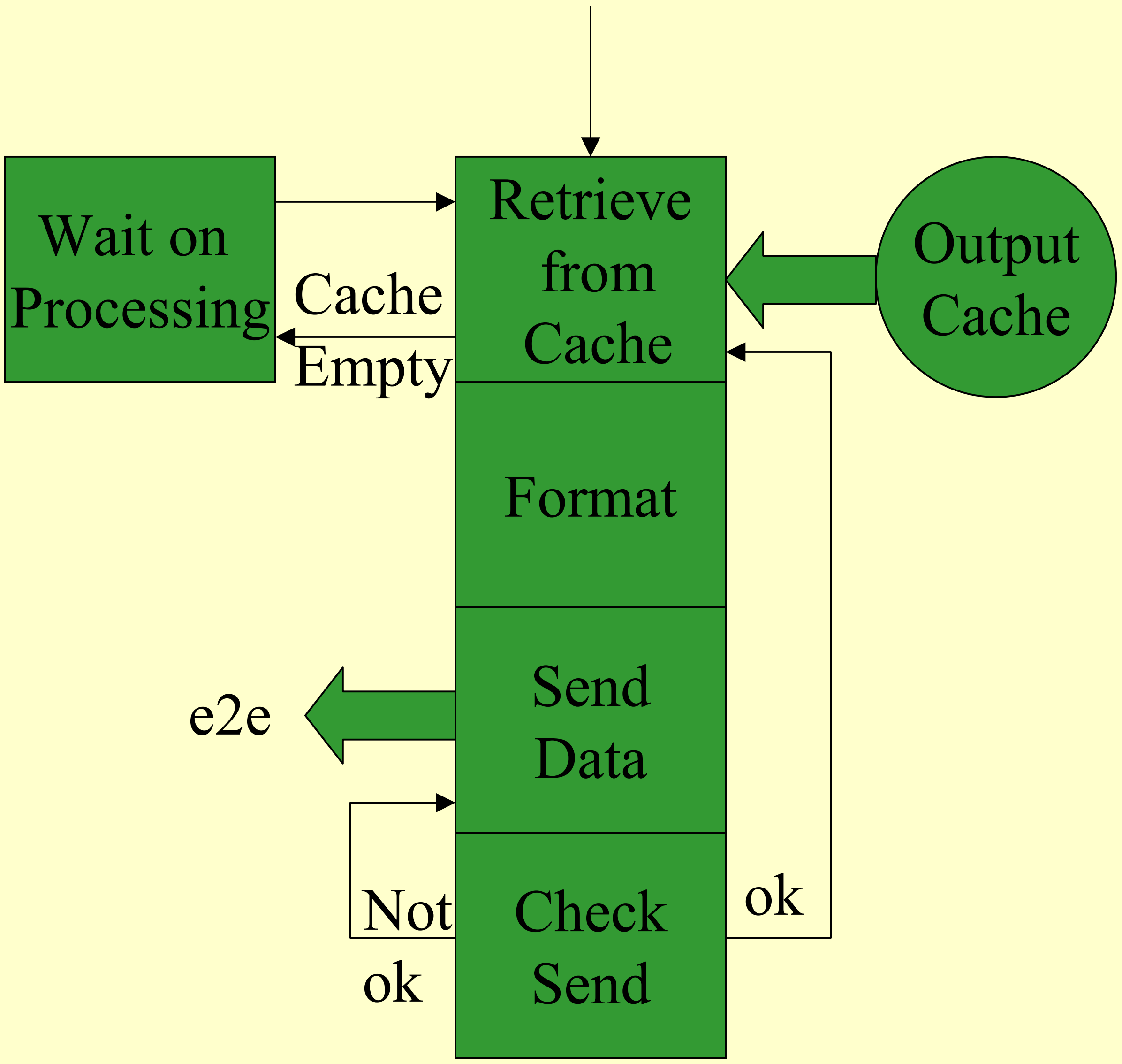
Output Cache Manager

- Receive Cache Index Request From DP
- Return Address of Next Free Location
- Receive Cache Index Request From Output
- Return Address of Next Data Going to e2e

Output Cache Manager

- Page-out Data When Memory Gets Full
- Page-in Data In Anticipation Of Retrieval for Output

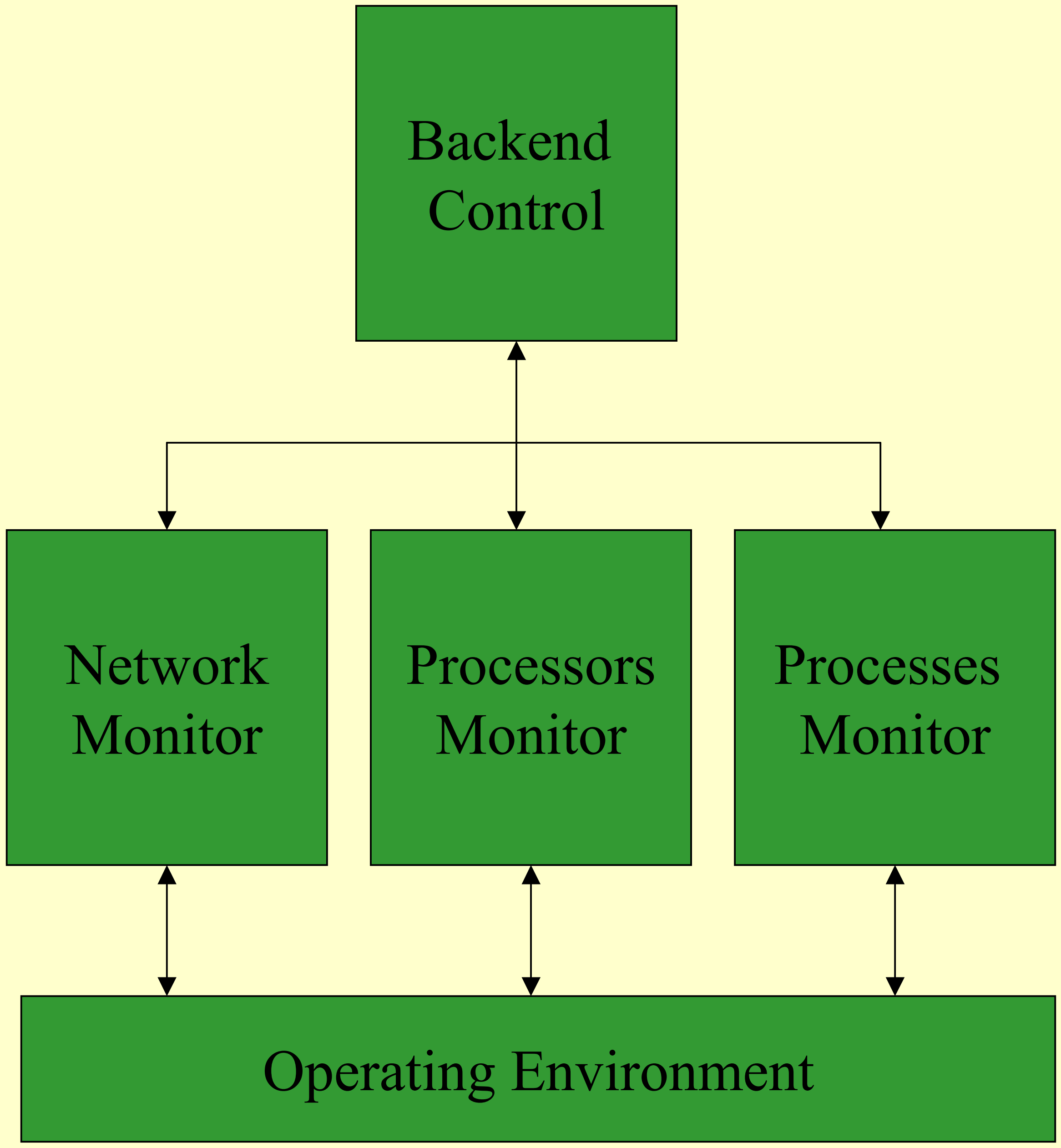
Output Function



Output

- Obtain Output Cache Index From Output Cache Manager
- Fetch Data From Output Cache
- Format
- Send to (Deposit into) e2e Archive

Backend M & C Functions



BE Control

- Message Intermediary Among BE Processes and M&C
- Three Classes of Incoming Messages
- Maintains Statistical Model of BE State

BE Control

- Class I Messages are Simply Routed to Proper Destination
- Class II Messages are Read for Updates to the Statistical Model and Routed to Proper Destination
- Class III Messages are Used to Generate Check and Repair, and Offload Requests

BE Monitor

- Status Checks
- Internal Network Restart
- Processor Reboot
- Process Kill and/or Restart
- Offload
- Failure, Error, Warning, Repair, Status, Offload Reports

Development Schedule

- 2Q 2002 – 4 Node Test Cluster
- 3Q 2002 – 8+ Node Cluster
- 4Q 2002 – Functional Prototype
- 4Q 2003 – Full Functionality
- 3Q 2004 – First Prototype Correlator Boards
- 4Q 2004 – Earliest BE Connect to Correlator Hardware