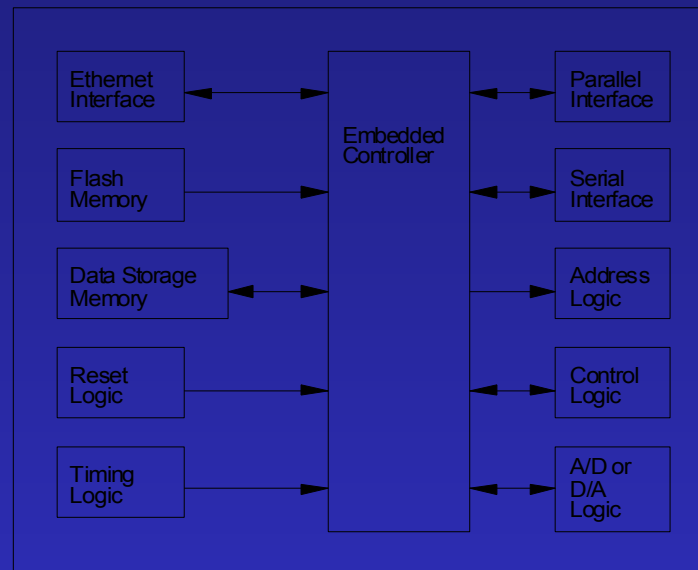
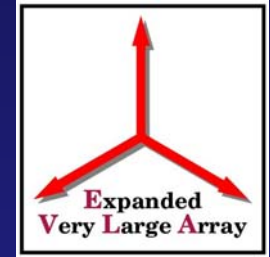


# EVLA Monitor and Control

## Module Interface Board (MIB) Design



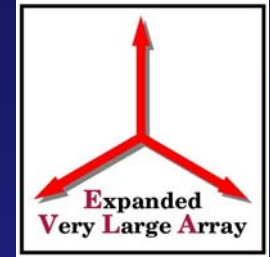
# MIB Block Diagram



**MIB Block Diagram**



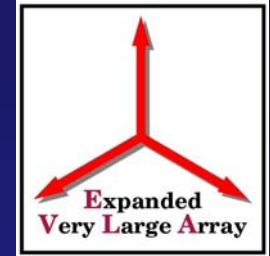
# Embedded Controller



- Infineon TRICore TC11IB
  - System On a CHIP
  - 12 MHZ External Clock
  - 1.5 MBytes RAM
  - Hardware/Software Resets
  - Watchdog Timer
  - Sleep Modes
  - Seven Thirty-Two Bit Timers



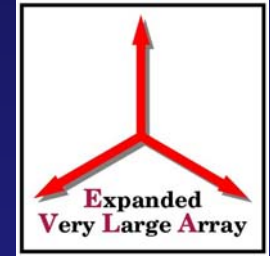
# Embedded Controller



- Infineon TC11IB – Interfaces
  - Media Independent Interface (MII)
  - PCI Bus – Version 2.2 @33MHz
  - MultiMediaCard Interface
  - Two Asynchronous Serial Ports
  - One Synchronous Serial Port (SPI)
  - Standard External Bus Interface



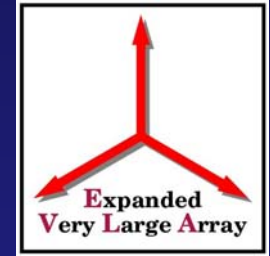
# Ethernet Interface



- Ethernet Interface – 100 MBit/second
  - Translation Chip – Intel LXT971A
  - Fiber Optic Transceiver – Infineon V23809-C8-C10



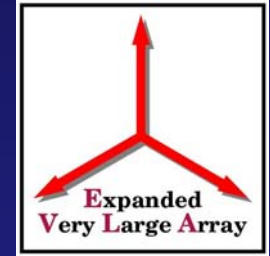
# Flash Memory



- Flash Memory – Checksum
  - Code Storage
    - ◆ MIB – Boots Main Operation Code
    - ◆ Device – Device Specific Code
  - Parameter Storage
    - ◆ MIB – Loads Slot ID and Parameters
    - ◆ Device – Device Parameters
  - All Code Documented



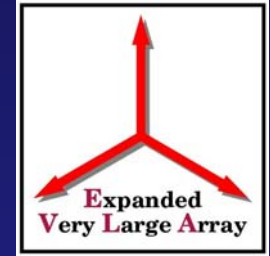
# Data Storage Memory



- Data RAM – Inside TC11IB
  - Code Storage
  - Parameter Storage
  - Communication Data Storage



# Reset Logic

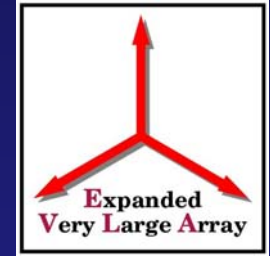


- Reset Logic
  - Power Supervisor – Maxim MAX706
  - Watchdog Protection – TC11IB
  - Devices Must Reset into Safe Condition





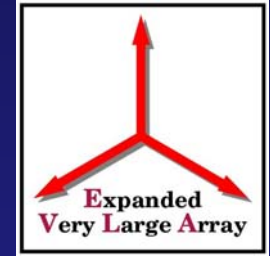
# Timing Logic



- Timing Logic
  - 19.2 Hz Timing Signal (Transition)
  - 1 PPS Timing Signal
  - 10 Second Timing Signal
  - 10 ms Timing Signal
  - Devices May Require Precise Timing
    - ◆ Hardware Timing



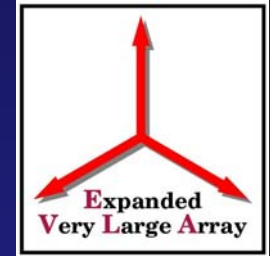
# Parallel Interface



- Parallel Interface
  - Thirty-Two Bits Transfer
  - PCI Bus
  - External Bus



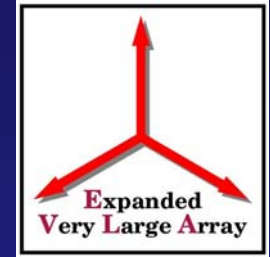
# Serial Interfaces



- Serial Interfaces
  - Asynchronous Ports
    - ◆ One Two Wire Port
    - ◆ One Modem Port
  - Synchronous Ports
    - ◆ SPI Port – UP to Sixteen Bits
    - ◆ How are Select Lines Provided?



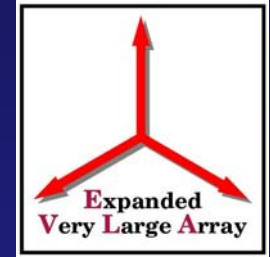
# Address Logic



- Address Logic
  - Memory Mapped Functions
  - Devices
    - ◆ Multiplexed Address/Data Bus
    - ◆ Separate Address/Data Bus



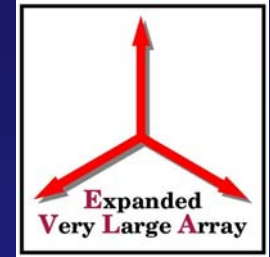
# Control Logic



- Control Logic
  - Peripheral Interfaces
    - ◆ Motorola or Intel or Both
  - NRAO Generated Interface
    - ◆ VLBA Model
    - ◆ Dual Port RAM Model



# A/D or D/A Logic



- A/D or D/A Logic
  - A/D Logic
    - ◆ Device
  - D/A Logic
    - ◆ Device