Panel Report: EVLA Monitor and Control Hardware Review

This report is in response to the findings of the EVLA M&C Hardware PDR Review Panel which are based on a top level presentation of the design plans conducted on March 13 at Socorro. The purpose of the review was to answer 3 principal questions:

1. Are the top level performance requirements complete and adequate?
2. Have the correct design solutions been selected for study and development during the EVLA design phase: Are there important alternate solutions that are not being studied?
3. Has an adequate procurement plan been identified for the subsystem?

Members of the Review Panel attending were the following:
Mick Brooks, ALMA
John Ford, GB
Jim Jackson, Hardware Systems Engineer
Gareth Hunt, Software Systems Engineer
Mike Revnell, substituting for Brent Carlson, Correlator Task Leader
Terry Cotter, LO/IF Task Leader
Steve Durand, Fiber Optics Task Leader
Paul Lilie, Receivers/Feeds Task Leader
Bill Sahr, Monitor and Controlasek Leader
George Peck, sub Task Leader for M&C Hardware

The format for this Response Report is to restate the question in the findings report and follow with the response. There is some combination
and re-organization of the questions in the Findings Report.

Part I The Responses.

1. The M&C Hardware project needs to develop a timeline to show when the mechanical configuration and electrical interface will be specified. A detailed plan must be in place to meet the target dates for the bench integration in January '03 and the test antenna in April of '03.

PHYSICAL INTERFACE (MIB)

Select MIB processor	DONE
Specify and purchase development board	2/14/02 - 4/15/02
Build prototype MIB	4/15/02 - 7/15/02
Issue MIB SPI applications memo	4/15/02
Responses due on MIB SPI applications	4/26/02
Write software for MIB to device interface	4/30/02 - 8/8/02
RTOS available for MIB testing	6/19/02

Test MIB prototype 7/15/02 - 9/27/02
Build MIBs for test antenna devices 9/27/02 - 12/27/02
Bench integration of all system devices 1/6/02 - 3/10/03
Test antenna evaluation 4/7/03 - 8/14/03
Revisions to MIB design 8/15/03 - 10/15/03
Begin quantity production of MIB 10/15/03

ANTENNA UTILITY MODULE
Specify and design antenna utility module 8/15/02 - 9/13/02
Build prototype module, applications 9/16/02 - 11/13/02
Responses on utility module applications 11/14/02 - 11/29/02
Test prototype utility module 12/02/02 - 2/18/03
Bench integration of utility module 2/18/03 - 3/7/03
Install prototype on test antenna 4/30/03

F14 TRANSITION MODULE
Specify and design F14 transition module 7/15/02 - 9/11/02
Build prototype F14 transition module 9/12/02 - 11/11/02
Add MIB and test prototype 11/12/02 - 2/13/03
Bench integration of F14 transition module 2/14/03 - 3/07/03
Evaluation on test antenna 4/07/03 - 8/14/03
Build production F14 transition modules 8/14/03

FRONT END INTERFACE MODULE
Specify and design module 4/26/02 - 9/11/02
Build prototype module 9/12/02 - 11/11/02
Add MIB and test prototype 11/12/02 - 2/13/03
Bench integration of module 2/14/03 - 3/07/03
Evaluation on test antenna 4/0/03 - 8/14/03
Build production modules 8/14/03

2. There must be enough people available to do the work for the hardware M&C project. The WBS shows the plan for personnel to support the project.

3. Details of the SPI interface must be specified in the electrical interface. An applications memo that specifies the details of the MIB SPI interface is to be issued on April 26, 2002. These details will be included when an electrical interface document for the MIB is issued.

4. Does a specification for a MIBIB (Module Interface Board Interface Board) need to be defined? We believe that such a board would be redundant, and is not needed. The MIB alone will handle all of the interface requirements between the EVLA modules and the Ethernet. The device interfaces

to the MIB will be specified in the electrical specifications document.

5. Several concerns were brought up about RFI. We plan to design the MIB and other M&C modules to meet any system RFI requirements that are in place. At this time, these requirements have not been specified. We plan to use design techniques that minimize RFI, such as using on-chip memory to run the code for the MIB processor, and terminating unused external bus lines on the TC11IB MIB processor chip. We plan to keep rise times as slow as is practical on the address and data lines, in order to minimize the impact of bounce on the data and address lines. When the MIB prototype is built, it will be tested in the chamber at the VLA site to determine the level of RFI emissions.

6. A coordinated development effort to allocate tasks between the hardware and software group is needed. The software group will implement a RTOS within the MIB. This RTOS will allow the hardware group to write code for the MIB in C and assembly language that monitors and controls the EVLA modules. The software group will write code for the MIB that interfaces the MIB to the Ethernet, and the rest of the computing system. Presently, the two groups interface at a weekly meeting every Tuesday. Additionally, other informal meetings take place as needed. It is hoped that good communication will help to keep the hardware and software groups at a similar pace. The hardware group will not slow down development effort to wait for the software. If the software and hardware groups can work at a similar pace, then we will not be forced to write our own temporary test software.

7. The software screens are to be implemented by the software group. Issues concerning the software screens could be raised at the M&C software PDR if they are not covered. The hardware group has a requirement that some screens will need to monitor/control multiple MIBs.

8. Where will the flagging software will be located? The hardware group will not be addressing this issue.

9. We plan to issue an ICD for each hardware M&C module. We will use a system-wide ICD format, if it exists. We expect to issue an ICD at the

time that the prototypes are being assembled. It is expected that individual designers of the M&C hardware will write the ICDs.

10. Several concerns were raised concerning the TC11IB Infineon chip. The TriCore architecture targets the following markets: communications, automotive, computer peripherals, industrial communications devices, motion control systems, and programmable logic control systems. The TC11IB is advertised as an industrial communications controller. It cannot be predicted how long the chip will be available. The TriCore architecture was introduced in 1999, and Infineon shows a roadmap for the architecture going to 2004 and beyond. The roadmap shows backward compatibility of the new TriCore architectures with the old. The TC11IB is part of the TriCore1 family. Preliminary information is now available on the TriCore2 family, but it appears that no products are yet available.

There is not presently a second source for the TC11IB. Infineon does, however, allow other semiconductor manufacturers to obtain licenses to manufacture products with the TriCore architecture, and Siemans plans to release a product this year. If the chip "founders", we would consider one of the alternative chips. The Lantronix DSTni (formerly EC-1) could work, but the on-board memory is limited. If we couldn't use the on-board memory, we could be forced to run the processor from off-chip memory. Altera has a programmable chip that could be used. The present version is limited in on-chip memory, but it is anticipated that future versions of the chip will include more on-chip memory. The schedule does provide for MIB redesign between 08/15/03 and 10/15/03. This is in case the initial experience with the test antenna shows that the design needs modification. There is not a replacement planned for the purpose of prolonging obsolescence of the MIB. It is expected that the lifetime of the EVLA electronics will be at least 25 years. Even if we plan to replace the MIB during construction, the MIB replacement would soon be obsolete. It may not be practical for NRAO to design a new MIB every time chips on the board become obsolete. A more practical approach for NRAO would be to purchase enough spare parts to support the board for a long time. The MIB is powerful enough to handle any expected enhancements to the EVLA. Obsolescence is first expected due to non-availability of parts.

11. Timing requirements for the MIB need more specific identification. This is largely a software issue. The MIB will receive one timing pulse,

possibly the 19.2 Hz. A timer on board the TC11IB, running at 12 MHZ, will keep time on the MIB. The resolution of this timer is 83 ns, but the resolution that will actually be used is a software issue. Commands received by the MIB will be time stamped with the execution time of the command. The command will be implemented within 100 us of the execution time.

12. Cost estimates to the MIB should reflect all costs, including external assembly. We plan to do this estimate at the time that a prototype board is being manufactured.

13. Reboot/reset needs need to be clarified. It is planned to use the power-on reset pin on the TC11IB chip. A power supervisor chip will drive this pin low if any of the voltages are out of spec. The TC11IB also can be reset by a command over the Ethernet to a certain register on the chip. There is an additional reset pin on the chip that could be used, if needed. If a global reset of a rack or an antenna is needed, this pin could be used, however there is no present plan to use this pin.

14. What is the global scheme for power failures? Which functions require power backup and for how long? It is currently planned that the 48 volt power supplies at the antenna be backed up. This would keep all monitor and control functions at the antenna running during a power failure. These power supplies should be backed up until the site power generators have had time to turn on and restore power. The control building monitor and control system also will be backed up, and remain on UPS until the generator has restored power. The duration of the UPS backup is a system requirement, and has not yet been specified.

15. Software revisions are to be accomplished by downloading flash RAM via the Ethernet. The flash RAM is to reside on the device, and its contents will be loaded to the MIB at power up. An application note will be issued telling the designers how to implement this flash RAM.

16. Requirements for the utility module must be defined. The fire alarm and the circuit breaker tripped monitor are to utilize the utility module. It is planned that the entire monitor and control system will be backed up. This will ensure that the operators know that the telescope is safe.

Thus, the utility module is no longer needed for backup monitor and control. It is anticipated that the utility module will serve as a "catch-all" module for monitor and control functions that do not fit in anywhere else. As shown above, the utility module will be specified in August and September of 2002.

17. Is there going to be an interface to auxiliary test equipment - mainly GPIB? It is planned that the Ethernet ports will be used to interface to auxiliary test equipment. Modern test equipment is now often made with an Ethernet port. If the test equipment being used has only GPIB, then an Ethernet-GPIB adapter can be used. These are available from companies such as oscilloscope manufacturers.

18. Will it be possible to develop a slot address without active components on the backplane? We will use an active component to determine slot address because the MIB can communicate with this device with only 4 wires. If we run wires to each slot to address the slot, it would involve more wires. It is not yet determined that the active components will go on the backplane. We do not yet know exactly what the modules will plug in to.

19. Are we satisfying the cooling requirements? We do not know the answer to this yet. We will get some idea when we get the TC11IB development board, and then we will check the MIB prototype to see if it emits enough heat to require module cooling.

20. Do we really need MIB to MIB communication? Direct MIB to MIB communication is not necessary, as long as the antenna computer could handle necessary communication between MIBs. If direct MIB to MIB communication is used, it would be used very sparingly.

21. Plan a "device side" and a "protocol side" for the MIB to simplify replacement/upgrade. The MIB interfaces to the device are being specified, and will be kept simple in order to make future updates/upgrades easier. If necessary, a software protocol will be developed between the MIB and the device, but presently the need for this has not come up.

22. Will the external bus on the TC11IB need to be extended off of the MIB? The external bus unit on the TC11IB could be used for parallel transfers.

It is currently planned to extend this bus off of the MIB, in case the speed utilized in parallel transfers is needed. It is not planned to use the PCI bus on the TC11IB, because it is not likely that the MIB will need to communicate with any device using PCI.

23. We will get an in-circuit emulator for the TC11IB, if one is available at a reasonable price.

24. Is bus memory management is always active, or only used when needed? The external bus unit (EBU) can be turned on and off. If we are not using the external bus, it can be turned off.

25. Data monitors will not have a destination target. Monitor data will be broadcast for anyone on the Ethernet who wants to listen.

26. Develop target dates for the integration of "orphan" systems into the EVLA monitor and control system. These "orphan" systems include HTRP, the PT link, and VLBI. We have not received clear direction that these systems should be integrated in to the EVLA monitor and control system. If we find out that this integration is needed, we will set dates for completion.

27. The F5 module will be replaced in the test antenna, and all other EVLA antennas. We must be sure that everything that is controlled in the current antennas by the F5 is controlled in the EVLA. This includes band switching control, IF filter control, FE attenuator balance, F3 LO set and readbacks, solar attenuation, K/Ku LO WG switch select, aux input for select VHF and UHF receivers, CAL, ALC, PEAK, GPT readbacks A2D, deicers (feed heaters), cal drive and control to all receivers and front ends, helium supply and return line pressure monitoring, and Iridium RFI filter control. We will review all functions of the F5 to be sure that nothing falls through the cracks. Most of the functions will be carried out by the new front end interface module that is being designed. The feed heaters will be controlled by the utility module.

28. How do we provide for lost packets on the Ethernet? It was said at the PDR that lost packets shouldn't be a problem for us. This is a software issue, and could be brought up at the software M&C PDR, if it isn't covered.

29. The protocol is needed urgently on the Ethernet side, as is the specification of the hardware interface. The protocol on the Ethernet side is a software issue. The specification of the hardware interface to the Ethernet is being developed at the present time.

30. Why don't we use a switch instead of a router at the control building? Routers route by IP address, and switches send data according to MAC address. Each EVLA antenna will have its own IP address. Either a switch or router could be used, but if a switch is used, it must be made to act like a router. The final decision on this issue should be deferred until about 2007, because it is impossible now to predict what hardware will be available at that time.

31. For the VOIP, will the phone number follow the antenna? Yes, it will.

32. For the VOIP, would voice priority affect the data, or would data priority affect the voice quality? If we do not try to prioritize anything, both data and voice will probably be fine. If there is a need to prioritize data or voice, it can be done in software.

33. Is it necessary to support both IPV4 and IPV6? The current standard is IPV4. It is likely that IPV6 will replace IPV4 as the standard. IPV6 is backwards compatible to IPV4. We should choose the best hardware without regard to this question. This is primarily a software (RTOS) question.

34. Will the software know if the MIB rebooted? The software needs to know if the MIB has rebooted, and the hardware design of the MIB will support this. Part of a module reset will be to send a message out over the Ethernet, so that the network will know that the module exists, is powered up, and is working. This message can be used also to indicate why the reset occurred.

35. Will monitor data stop being published from MIB if the client disappears? This is a software question. If the client terminates in a normal manner, then the monitor data will no longer be published. It is preferable that the monitor data stop even if the client terminates in an abnormal manner. This could be further addressed in the software M&C PDR.

36. What is the effect of hot swapping on MAC addresses? Can the MIB set its

own MAC and IP addresses? When a module is plugged in after a hot swap, it will go through its power up sequence. The device will read its slot number and antenna number from an active component associated with the particular slot. These numbers will make the final determination of MAC address and IP address. Then, the MIB that is associated with the module will send out a message over the Ethernet, so that the switch can find out that the module is present, and communicate with it.

37. Will separate MIBs be used for the ACU and FRM? Presently, it is planned to use one MIB for both, but if there is a compelling reason to use two MIBs, this can be done.

38. Will the 19.2 Hz update be sufficient for OTF mapping? It should be ok, as long as the antenna tracks smoothly.

39. FRM indexing should be saved centrally. This is ok.

40. What is the timeline for installing the prototype ACU/servo on the test antenna? The hardware effort will last through July or August, and the software effort will be ongoing until the installation on the test antenna in April '03.

Part II. Conclusions:

The top level performance requirements for the EVLA M&C design are complete and adequate assuming the responses to the questions are acceptable.

Correct design solutions have been selected, again assuming the responses to the questions are acceptable.

The procurement issues shown in the Findings Report are addressed.

For the Panel,

George Peck
M&C Hardware Task Leader