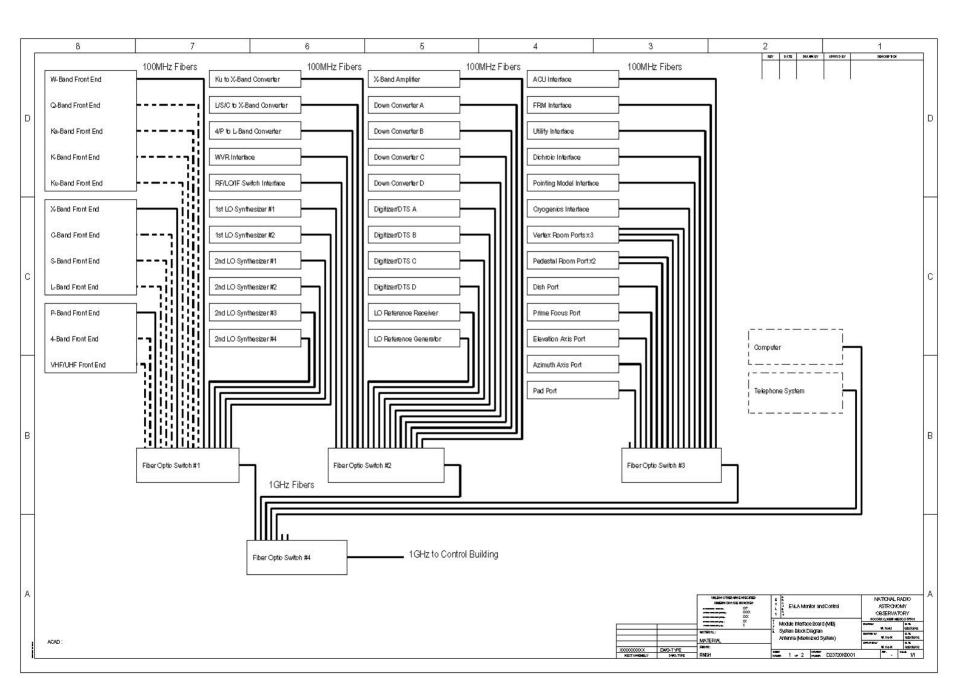
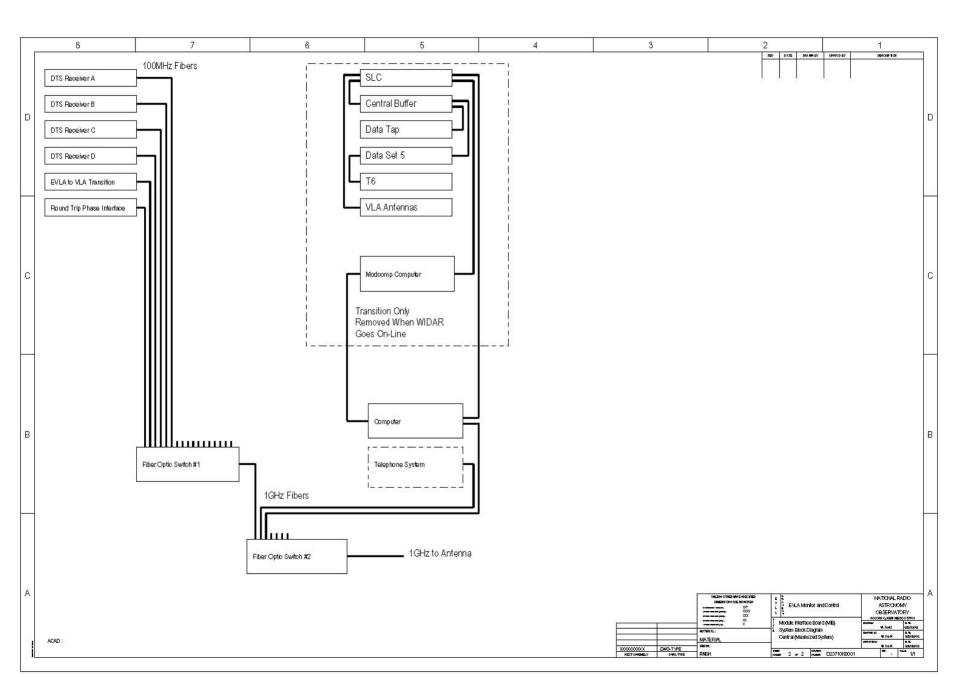
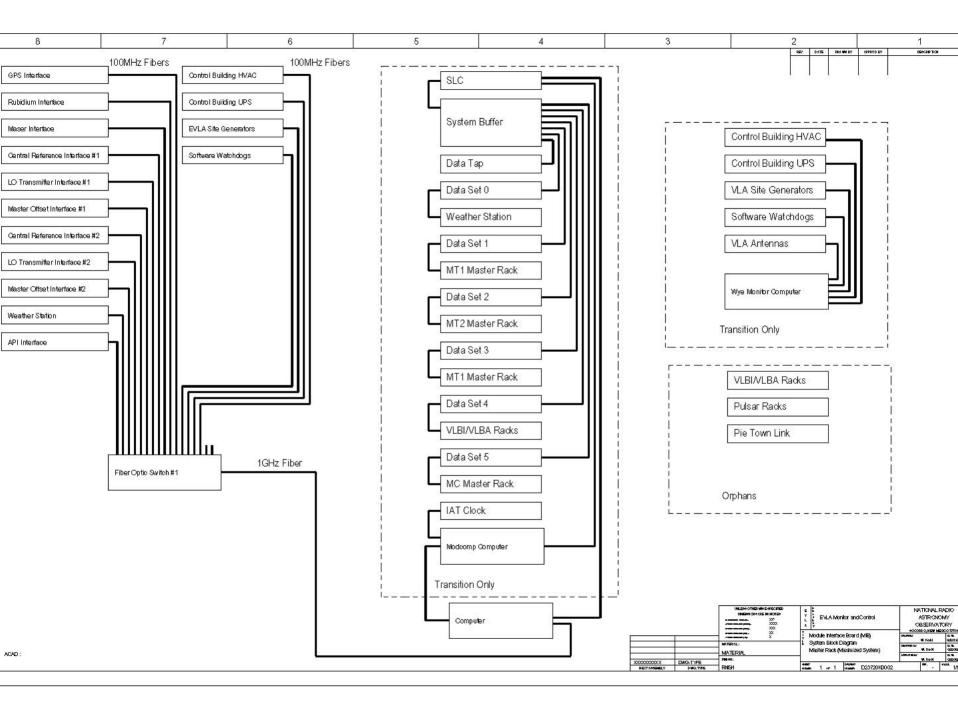


# APPLICATIONS AND DEVICE INTERFACE ISSUES

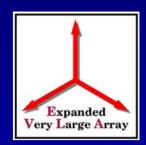




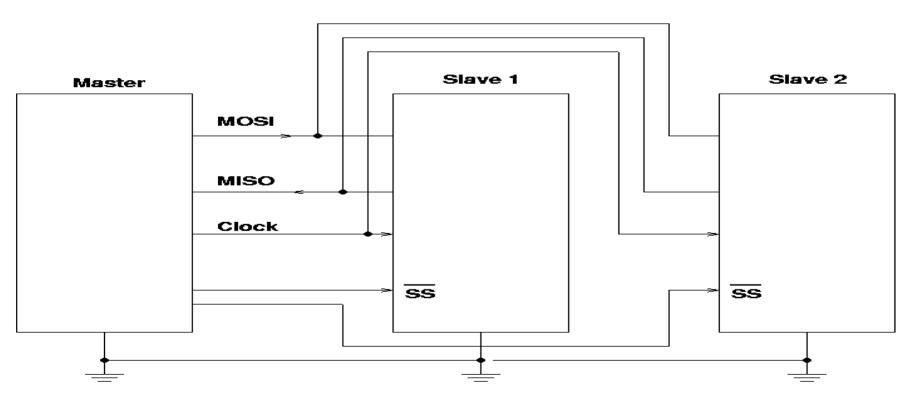




### SERIAL PERIPHERAL INTERFACE (SPI)



#### Synchronous Serial Communications



With select lines, one master can communicate with more than one slave



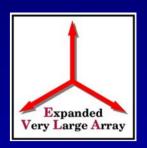
## SERIAL PERIPHERAL INTERFACE (SPI)



- Widely Used to Communicate With Many Devices (A/D & D/A Converters, Memory Chips, Temperature Sensors, Microprocessors, Etc.)
- Clock is Idle When Not Used



# MIB TO MIB COMMUNICATION



- Can Be Used As Needed Control Computer to MIB is Most Common
- Pointing Model Interface
- Front End to Cryo Communications
- Total Power to Down Converter Communications
- Utility Module



#### FRONT END M & C



- "F14 Like Module" In Rack Away From Receiver (To Reduce RFI) Contains MIB
- Each Module Interfaces to One or More Front Ends
- Single 25 Pin Connector Carries All Analog and Digital Signals to/from Receiver Card Cage



#### FRONT END M & C



- SPI Used for Digital Signals
- Analog Multiplexers to Select Three Analog Signals at a Time
- RFI Issues Must be Considered



# Monitor and Control Induced RFI



- Hardware Design to Conform to RFI Plan
- If Glitches Still Occur, Data Could be Flagged Bad
- We Could Plan Periodic Flagging of Data Throughout the Array (Infrequently) For Transactions That May Cause Glitches