Report: EVLA "Delta" LO/IF PDR

On April 17, 2002, the LO/IF Task Design Team presented design changes precipitated by concerns brought up during the LO/IF PDR presented in February 2002. This report summarizes the recommendations and comments from the Delta PDR. The changes will be incorporated into the LO/IF PDR summary report, once those interested have reviewed the information and had the opportunity to comment.

New Architecture for Synthesizers by Jim Muehlberg

The fundamental change to the LO synthesizer design is to permit 1 or 5 MHz steps. The additional resolution of the steps over the initial design presented in February will be needed during the transition. The new design is much the same as the one at Astron. The main difference is in the use of the DDS tuneable frequency synthesizers.

Some questions that came up during the review:

1. What is the phase performance of the DDS especially at the high multiplication rate proposed?

Answer: We'll have to experiment. The question relates to the "control loop" oscillator as it is called in the Astron design. Jim specified the DDS here due to ease of use. We can easily (!) implement a traditional VCO here.

2. What is the temperature sensitivity of the design?

Answer: Gie Han mentioned in his paper the sensitivity of the sampling mixer (phase v. temperature) was almost eliminated by biasing the diodes. I have provided for this in my design. We'll still need to experiment.

3. In general, performance characteristics of the proposed synthesizer design did not seem to be well understood. Do we need a fall back position?

Answer: Performance can be theorized but we need to build it. If we had a team of people working on the LO's we perhaps could afford the time to simulate, if we had the tools. The principle characteristics are short term phase stability (phase noise), long term phase stability and phase coherence between frequencies and those requirements are understood.

UX Converter by Paul Harden

Changes were shown to provide for the block conversion scheme proposed by FE and dropped the number of switches required from three to two.

Three sets of power monitors are proposed:

1. At the input, one per polarization. Especially important where there is RFI.
2. Input of downconverter.
3. Head of sampler for AGC.

Each monitor point will cost an estimated $1500 which drives interest in minimizing the number of points.

There was discussion over the location of amplifiers and filters though the general philosophy is to locate filters as early in the signal chain as possible.

System SNR and Headroom by Travis Newton

The presentation gave calculated values for SNR and headroom for different modules in the IF. In some cases, an SNR less than 20 dB was shown. 20 dB SNR is the minimum requirement at the input to the sampler to avoid losing data. Insufficient headroom may exist in the receiver assuming a gain block at input of T303 converter and gain block at input to T302 converter. It may be necessary to trade gain between receiver and the T303.

Some clarification may be needed to show what the signal level is 12 dB below the 1% compression point.

The rule of thumb used is :

P(-1%)=P(-1dB) - 12 dB and headroom reported is delta between signal level and P(-1%).

Regarding the question of intermod levels relative to signal levels, here is the details of the calculation:

Given a nominal value of IP3 (Third order intercept point) being 10 dB higher than P(-1dB), and using same rule of thumb of P(-1%)=P(-1 dB) - 12 dB, intermod levels will be 44 dB below P(-1%) level.

Via relationship: IMD=3*(Pin+Gain)-2*IP3 and Pin=Pout-Gain and Pout at point of interest is P(-1%)

If Pout is kept 20 dB below P(-1%) (definition of headroom=20dB)

Then: by same equation IMD=3*(Pin+Gain)-2*IP3

=3*(Pout-Gain+Gain)-2*(P(-1%)+12+10)

=3*(P(-1%)-20)-2*(P(-1%)+22)

=3*P(-1%) -60 -44 -2(P(-1%) =P(-1%)-104

or:

Intermods are 104 dB below P(-1%)

or 84 dB below carrier if signal kept 20 dB below P(-1%) level

Is the time constant of the power detectors sufficient to blank data in the correlator?

Need to know the distribution of peaks in the DME (1 - 1.2 GHz).

Tuning Scheme and new 4096 synthesizer

Scheme calls for 500 MHz steps in LO1 and 10 MHz steps in LO2. Cost will be $2500 for each 4096 MHz synthesizer; two per antenna.

May need more gain in front of mixer to get amplifier above the noise floor.

High multiplication rates of DDS in LO synthesizer may be less of a problem with the 4096 synthesizer.

Need to know more about switches. Will MMICs impact?

Prototype one?

For the panel

Clint Janes