DATA TRANSMISSION SYSTEM

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OUTLINE

- Top level specifications
- Basic architecture
- Fiber plant
- DTS module
- Digitizers
- Formatter
- Deformatter
- Transition converter

SPECIFICATIONS

- Deliver 16 GHz of bandwidth per antenna to the correlator. (4IF x 2POL x 2GHz)
- 8 digitizers at 3 bit resolution in wideband mode.
- 4 digitizers at 8 bit resolution in high resolution mode (4 GHz total bandwidth).

SPECIFICATIONS

- Digitizing at the antenna.....
- 98304000000 bits per second per antenna of payload data. >120 Gbits/sec per antenna total.
- Bit error rate 10^{-9} start of life, 10^{-6} end of life.
- Measured run 8 days with 0 errors ($<2x10^{-17}$).

FIBER PLANT

- Fiber burial is complete.
- Individual fiber runs from patch room to each antenna pad. 12 fibers per pad.
- Station fibers from patch room to correlator room.
- All west arm splices complete 4 pads terminated.

DTS MODULE

- Digitizing at the antenna is a fundamental architecture decision.
- Much digital hardware with fast edges makes RFI a crucial problem.

DTS MODULE

- Defense in depth from board to module to rack design.
- Digitizers and all associated electronics in a single module (4 per antenna).
- Shielding of module measured >80 dB.
- Except for front panel, identical to ALMA.

3 BIT DIGITIZER

- Use the ALMA module.
- Or we wait for industry to produce suitable components.
- Or undertake our own development project.
- We can wait, 4 GHz bandwidth per antenna is a significant operational capability. We can generate correlator test vectors in the deformatter.

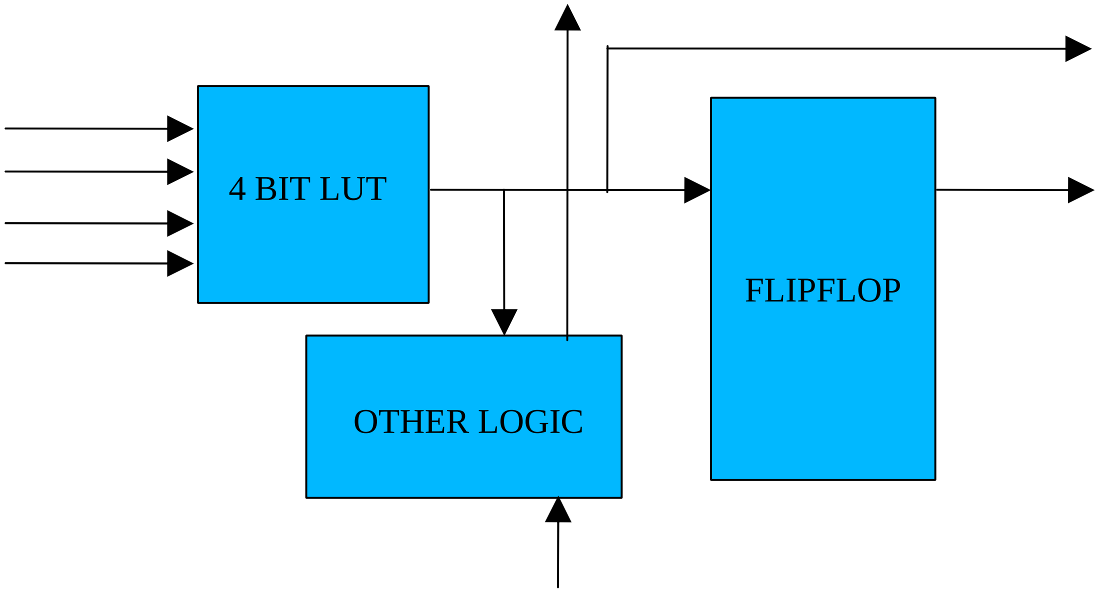
8 BIT DIGITIZER

- Two year old design uses two interleaved MAX104 parts.
- Perfectly fine dual 1 Gsa/sec digitizer.
- Phase mismatches cause significant images.
- Could, probably, be made to work with much labor.
- Works fine for transition application.

8 BIT DIGITIZER

- ATMEL have introduced a 10 bit 2 Gsa/sec part (TS83102G0B).
- New design in progress.
- Prototype quantities of major parts on order.
- Ready by late summer.

MODERN FPGAS



BASIC LOGIC ELEMENT

MODERN FPGAS

- Xilinx in formatter has 10,000
- Altera in deformatter has 19,500
- Example implementation costs:
  - – 8 bit adder 9 LE.
  - – 8 bit adder accumulator 9 LE.
  - – 16 bit counter 16 LE.
  - – 8 bit multiplier 0 LE.

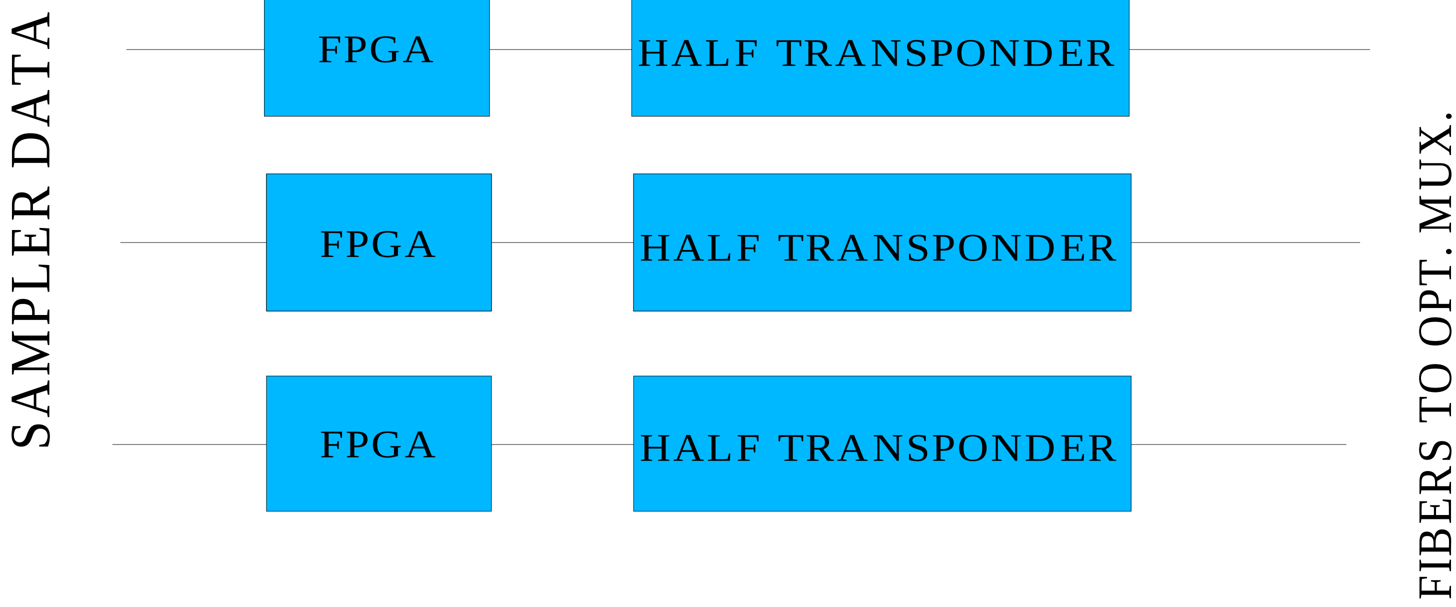
MODERN FPGAS

- Altera Stratix EP1S20:
- 80 9X9 bit multipliers (256 MHz).
- High speed (840Mb/s) serial I/O in pin logic.
- 1.7 Mb memory.

FORMATTER

- Accepts digitizer data, combines 128 payload bits with supervisory, timing, and parity into 160 bit frames.
- Processes 3 OC-192 channels (30 Gb/sec).
- New design using half transponder architecture delivered and undergoing test.
- Simplified design and construction compared to prototype.

FORMATTER

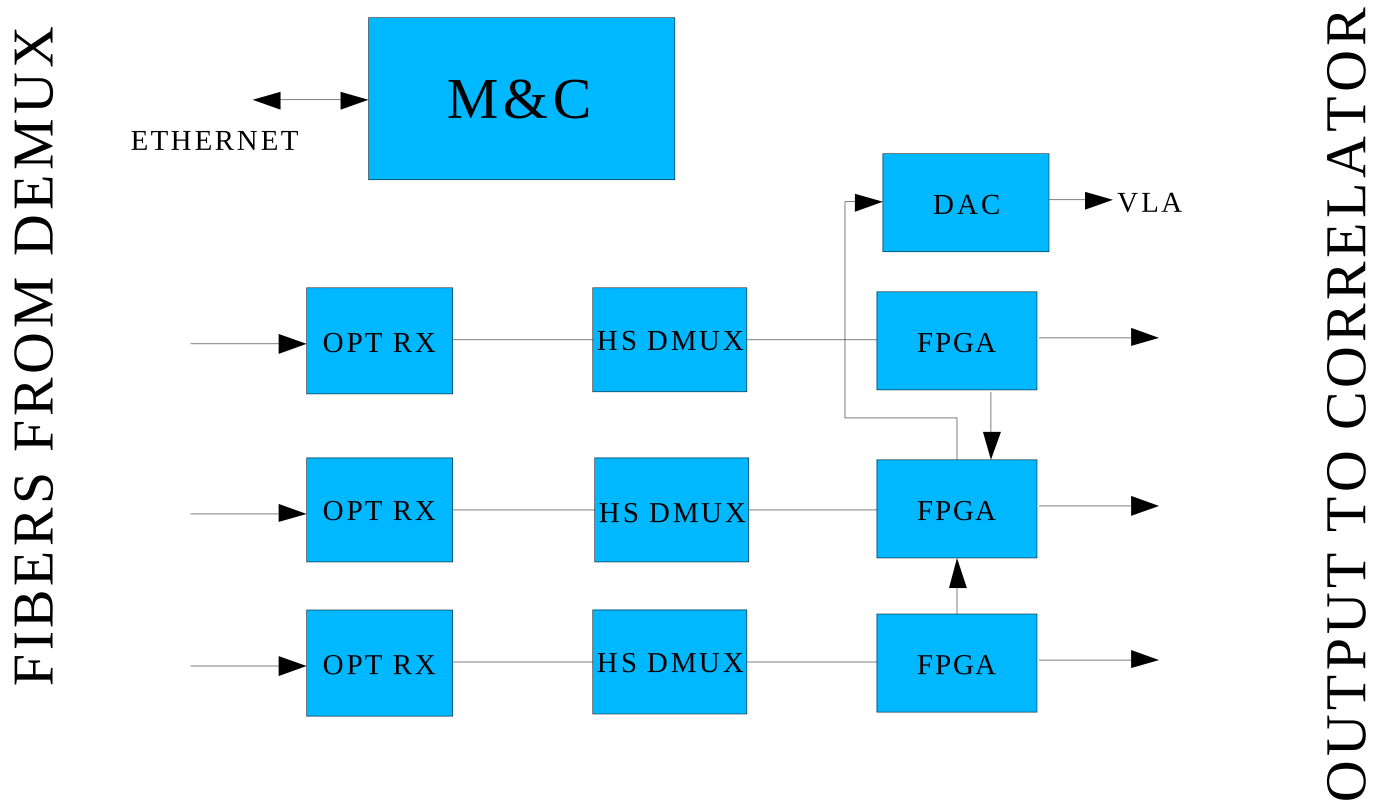


HALF TRANSPONDERS INCLUDE HIGH SPEED MULTIPLEXOR, MODULATOR AND LASER

DEFORMATTER

- Receives 3 OC-192 channels from formatter.
- Synchronizes to frame boundaries, aligns frames from 3 received channels.
- Repackages data and schedules delivery to correlator.
- Design meets ICD to WIDAR station card.
- Incorporates transition converter.

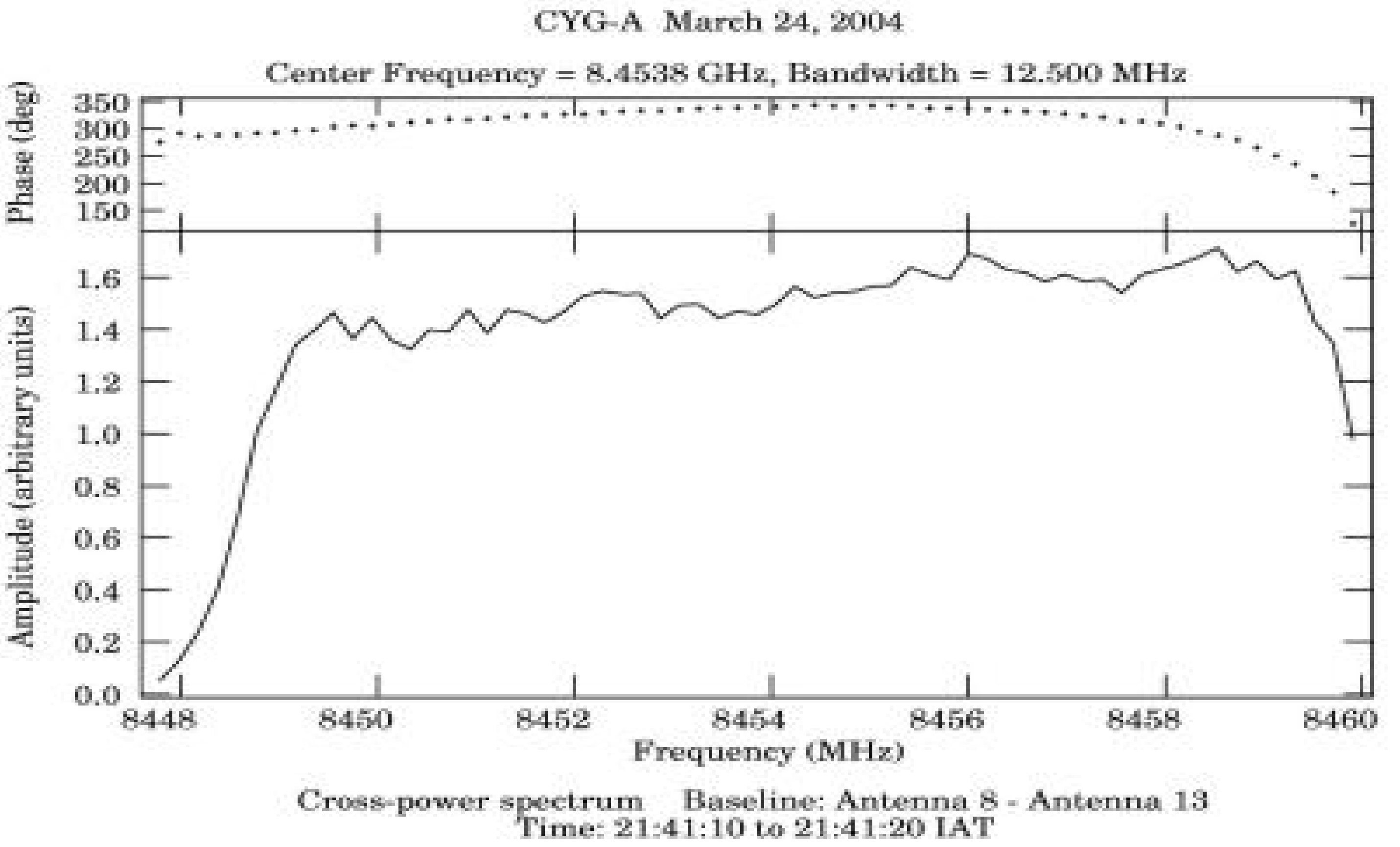
DEFORMATTER



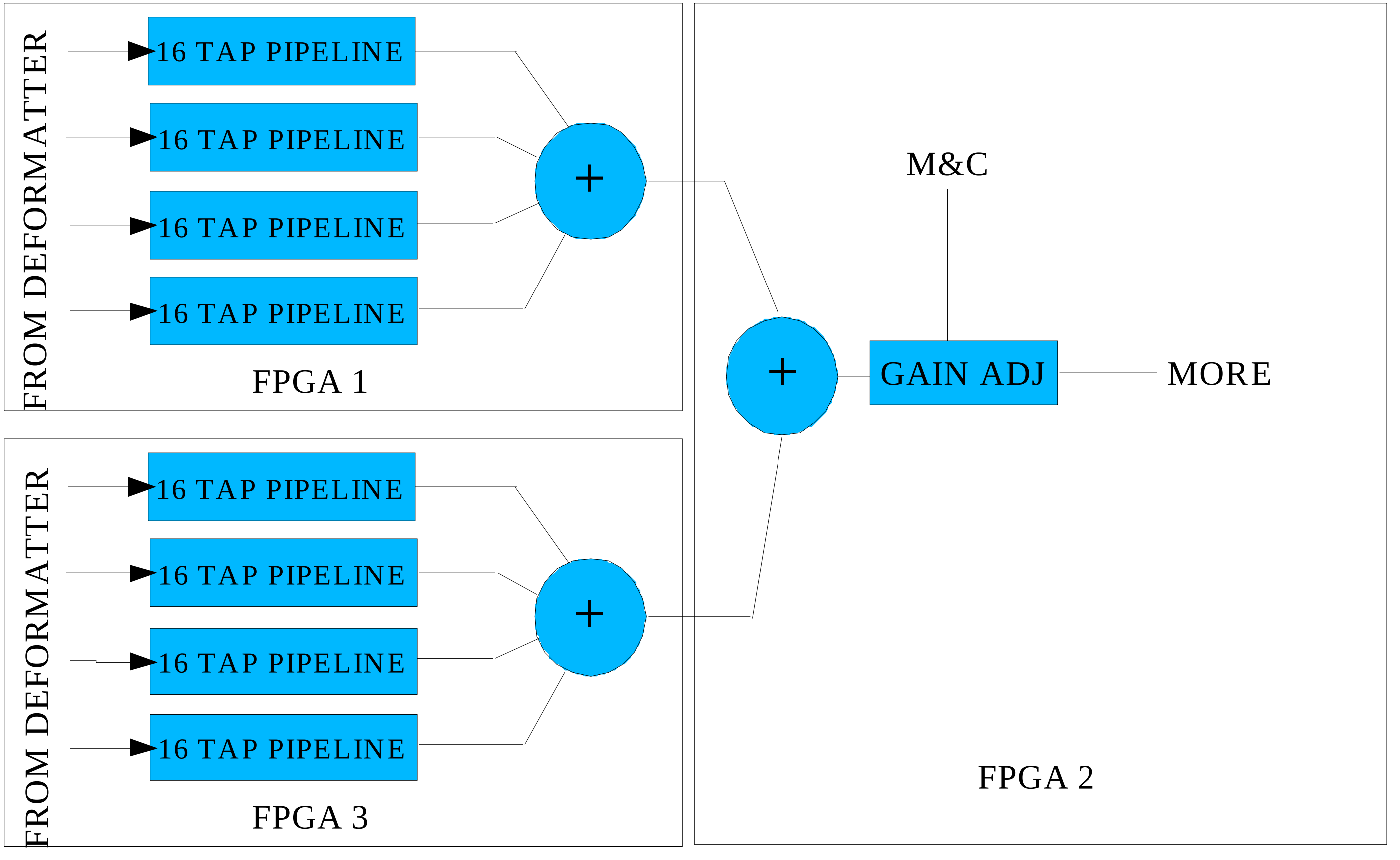
TRANSITION CONV.

- Filters 1 GHz bandwidh 8 bit data to 50 MHz
- Converts to analog which is introduced to VLA baseband filters.
- Must match phase characteristics of current VLA.

ANTENNA 13 VS VLA PHASE

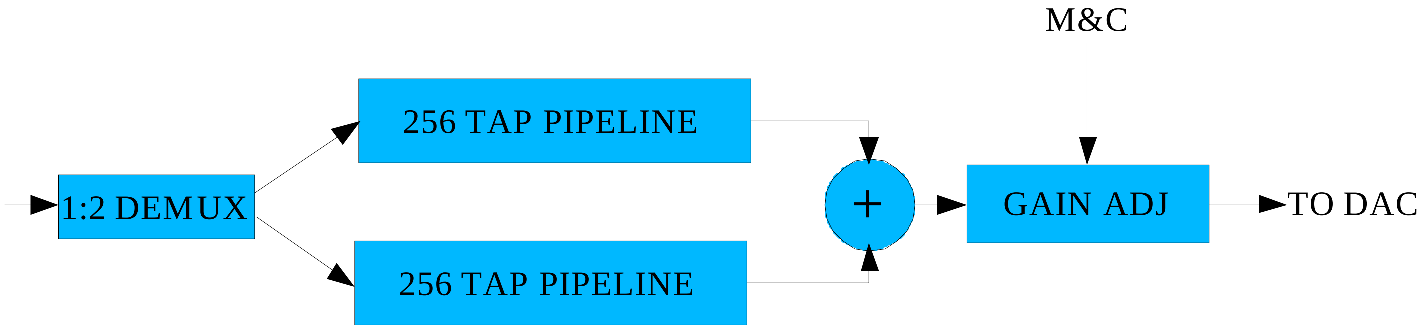


FILTER



FROM DEFORMATTER
16 TAP PIPELINE
16 TAP PIPELINE
16 TAP PIPELINE
16 TAP PIPELINE
+
FPGA 1
FROM DEFORMATTER
16 TAP PIPELINE
16 TAP PIPELINE
16 TAP PIPELINE
16 TAP PIPELINE
+
FPGA 3
M&C
+
GAIN ADJ
MORE
FPGA 2

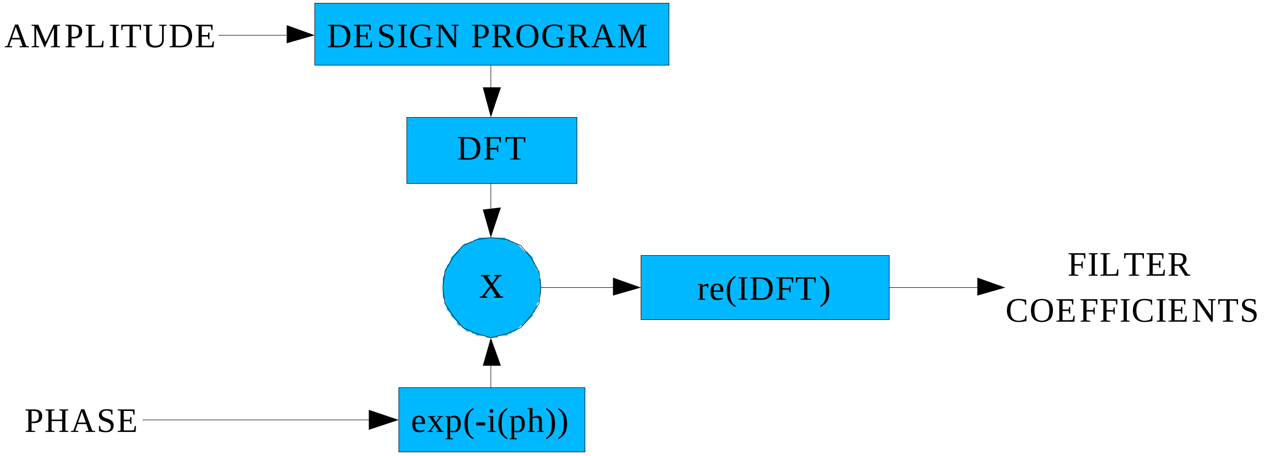
FILTER



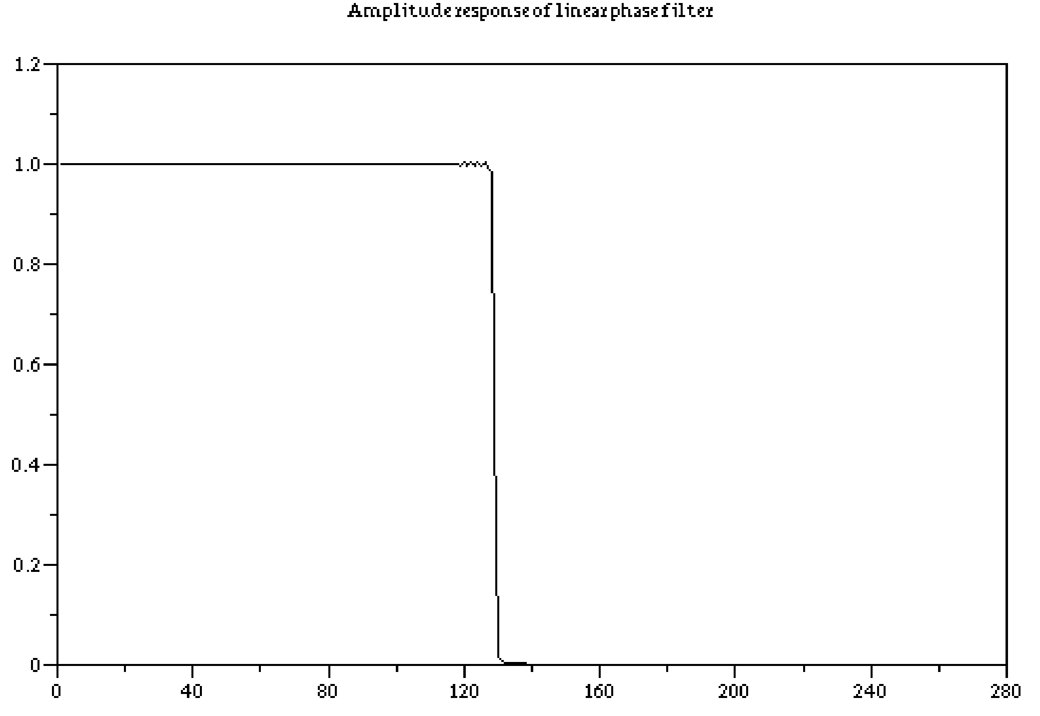
FIR FILTERS

- Are computational entities, they have no counterpart in the analog world.
- Filter design programs support design of linear phase FIR filters.
- Impulse response of direct form filters is exactly the coefficient set. We can apply the convolution theorem to the coefficent set.

NONLINEAR PHASE FIR PROCEDURE

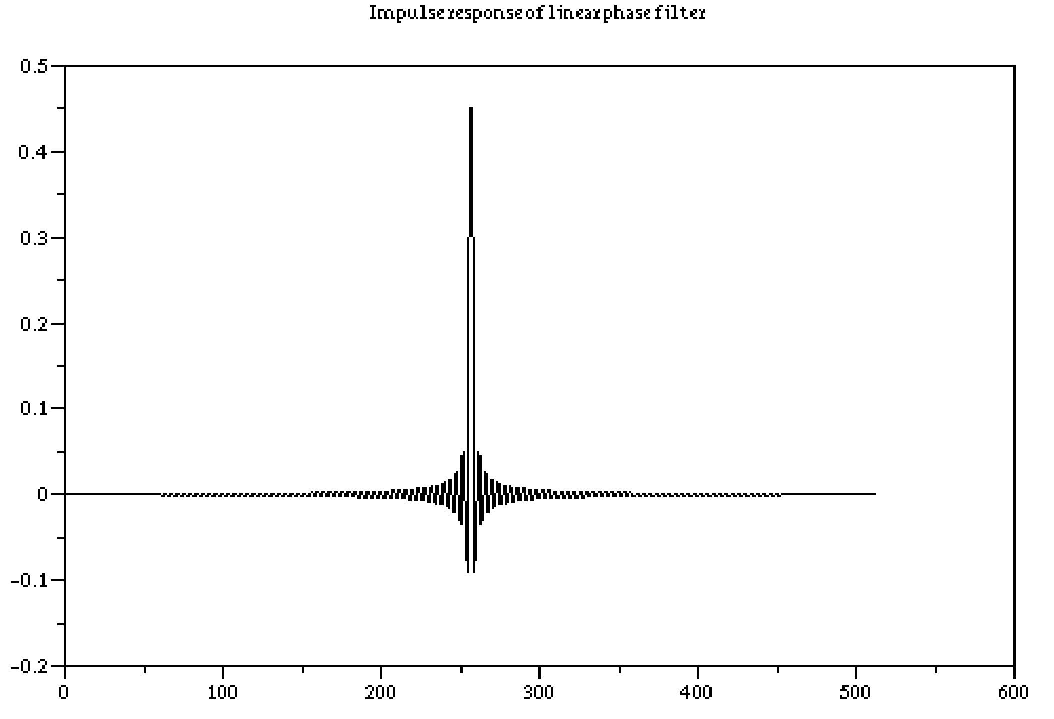


EXAMPLE

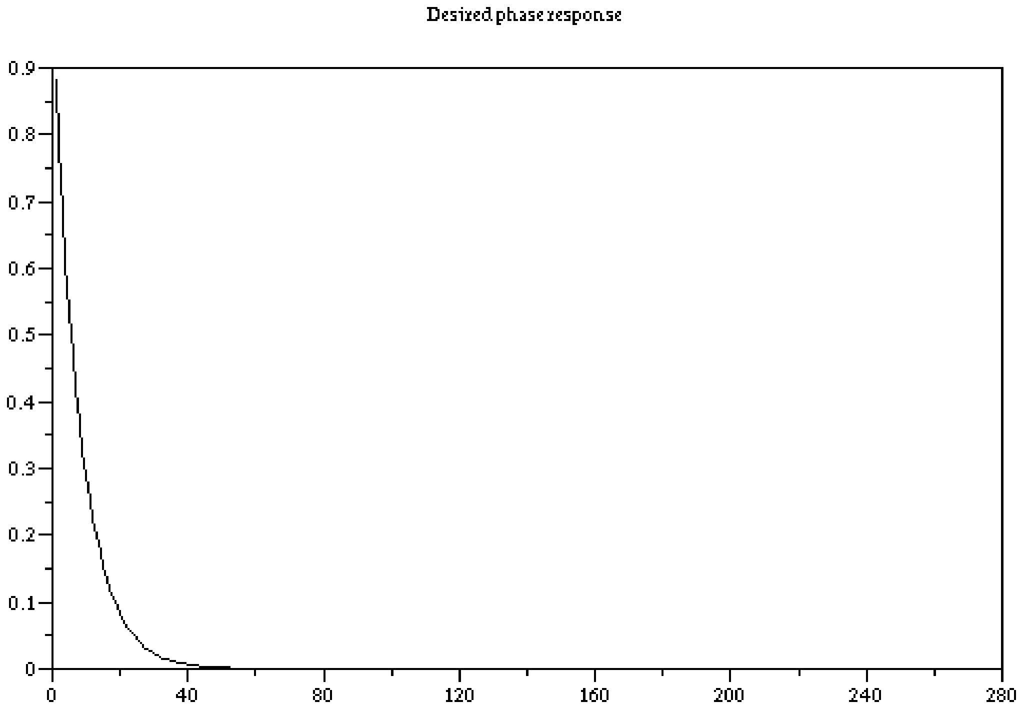


Amplitude response of linear phase filter
1.2
1.0
0.8
0.6
0.4
0.2
0
0
40
80
120
160
200
240
280

EXAMPLE

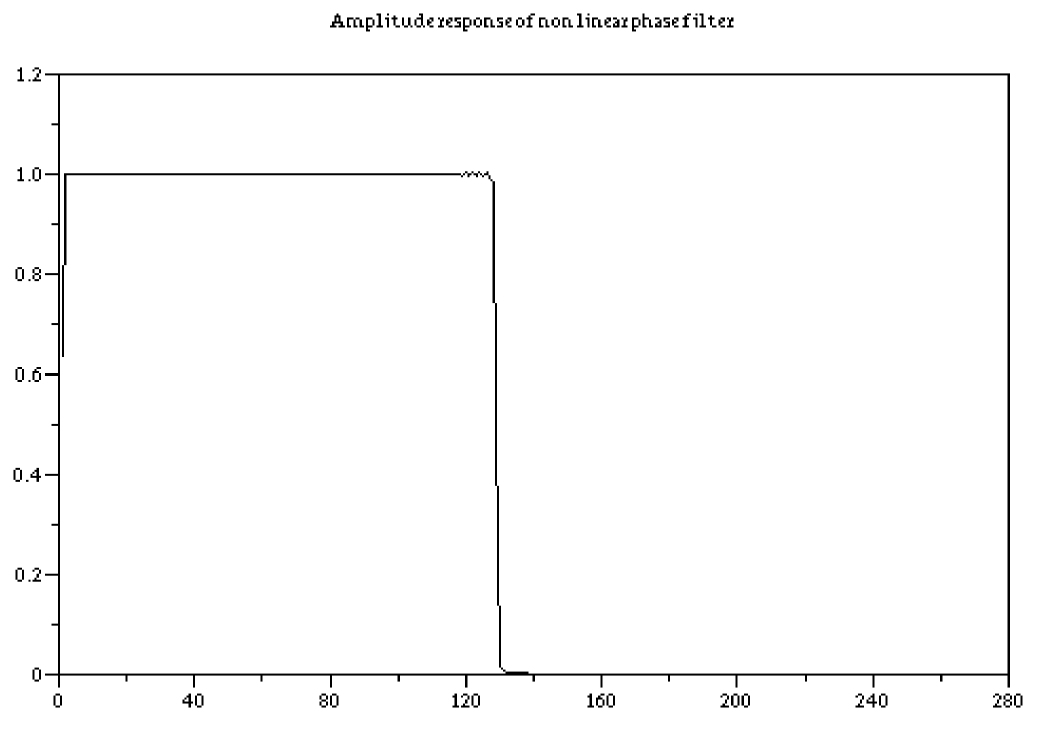

Impulse response of linear phase filter
0.5
0.4
0.3
0.2
0.1
0
−0.1
−0.2
0
100
200
300
400
500
600

EXAMPLE

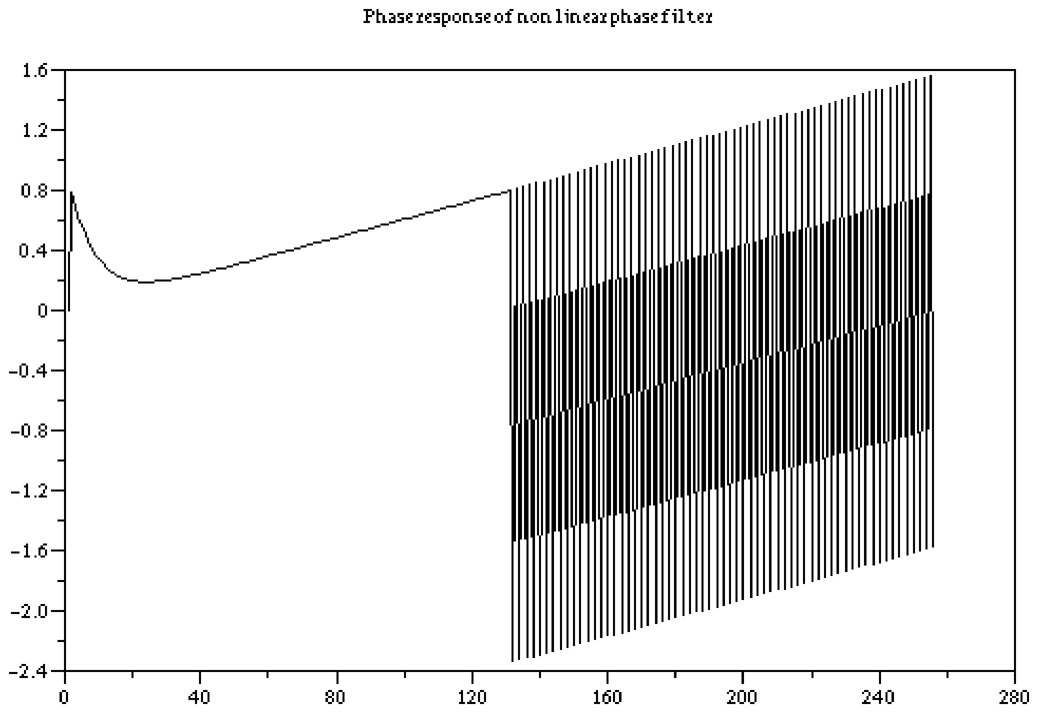


Desired phase response
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
40
80
120
160
200
240
280

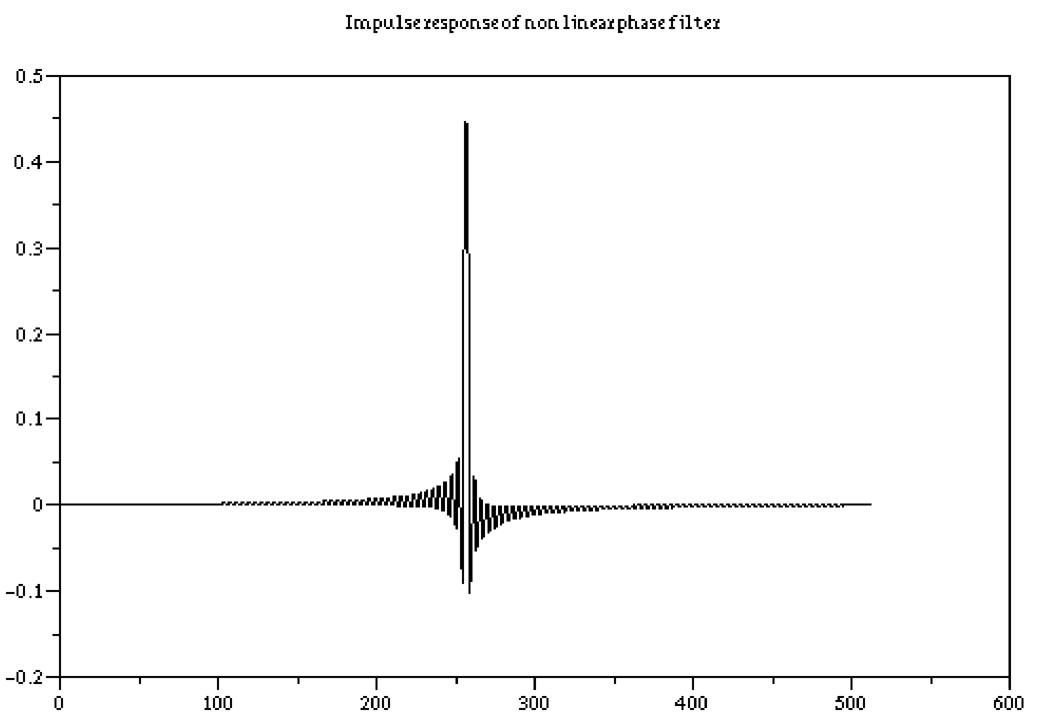
EXAMPLE


Amplitude response of non linear phase filter
1.2
1.0
0.8
0.6
0.4
0.2
0
0
40
80
120
160
200
240
280

EXAMPLE


Phase response of non linear phase filter
1.6
1.2
0.8
0.4
0
-0.4
-0.8
-1.2
-1.6
-2.0
-2.4
0
40
80
120
160
200
240
280

EXAMPLE



Impulseresponseof non linearphase filter
0.5
0.4
0.3
0.2
0.1
0
−0.1
−0.2
0
100
200
300
400
500
600

CONCLUSION

- We have operating prototypes of all elements.
- We have corrected designs ready for production.
- The transition converter works, we can match the VLA phase behavior.