Detailed Technical Points

Outline

- FIR filter.

- Recirculation.

- Correlator chip.

- LTA controller.

FIR Filter

- Desirable to implement in FPGA to minimize NRE+risk, and maximize flexibility (baseband input arrangement, 8-bit processing, 2-stage capability).

- Currently, it will not be affordable to implement 1024 taps, 4-bits in an FPGA (requires XC2V4000-5 >$1000 each).

- However, reducing the number of taps to ~500 should enable it to fit in an XC2V1500-5 @ ~$344 (Xilinx price projection to 2004).

- But, the budget is $200/chip…

- So, with 3-bit data, and cosine symmetric, should fit a 511-tap FIR in an XC2V1000-5 @ $224 ea. (Xilinx price projection to 2004).

FIR Filter

- ## With XC2V1000-5 chip for a cosine symmetric FIR:

  - Only have ~320 taps with 4 bits (direct realization, 4773 logic slices).

  - This is only 160 taps with 8 bits initial quantization. But, *with 4-bit requantization*, only 1/8 bandpass required, therefore gang two chips to yield 320 taps. Ganging chips is probably going to be required for narrower band selection, but reduces number of sub-bands available...

  - But, problem with 8-bit initial quantization and 7-bit requantization (because of output data highways). Only 160 taps to produce 1/16 bandpass…not acceptable performance!
    - Solution: 1 pol'n per Station Board? (but still only 320 taps).
    - Solution: smaller LUT? (less reject-band attenuation when we want it).
    - Solution: no 7-bit requantization…just chuck interference sub-band...
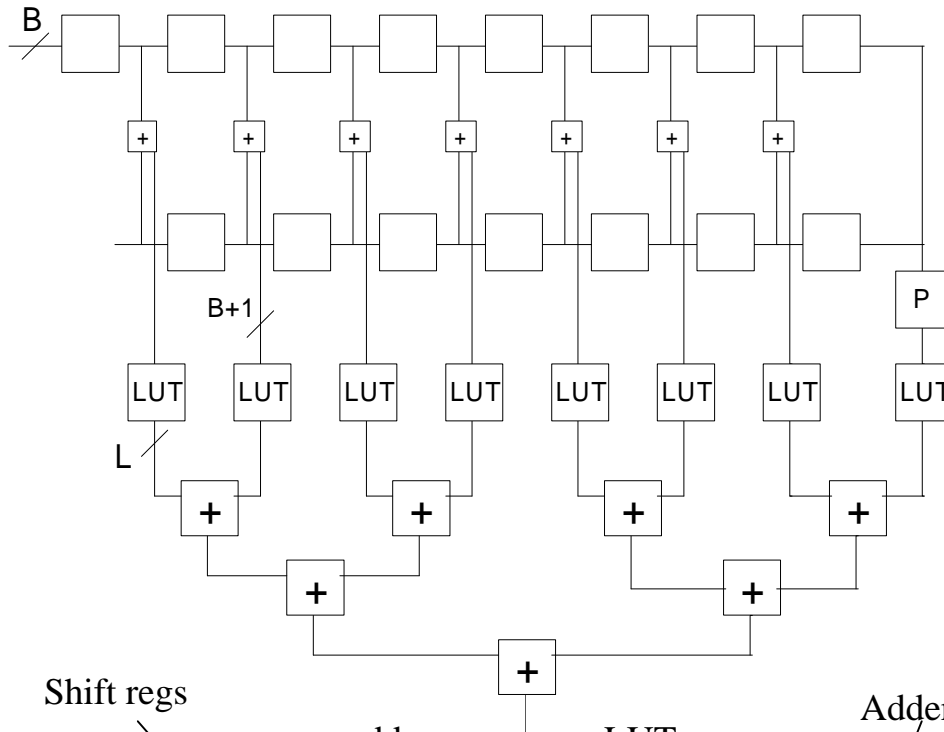
FIR Direct Realization: B=4-bits
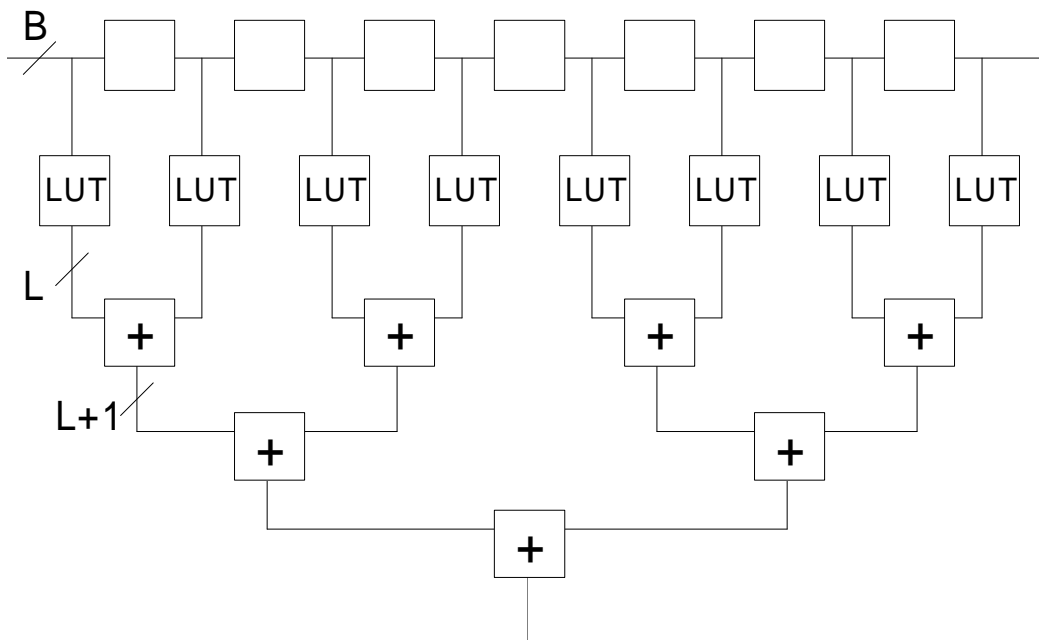
For B=4, L=12, N=512:

LS=7638 logic slices

XC2V1500=7680 LS's

(max 16-bit adder)

For B=4, **L=10**, N=512:

LS=6638 logic slices

XC2V1500=7680 LS's

(max 16-bit adder)

Shift regs   LUTs   Adder tree

$$LS = \frac{1}{2} \cdot \left[(N-1) \cdot B + N \cdot L + N \cdot \sum_{i=1}^{ceil(\log_2(N))} \frac{(L+i)}{2^i} \right]$$

NRC·CNRC

Cosine Symmetric B=3-bits

For B=3, L=12, N=511:

LS=4582 logic slices

XC2V1000=5120 LS's

(max 16-bit adder)

For B=3, **L=10**, N=511:

LS=4082 logic slices

For B=3, **L=10**, **N=1023**:

LS=8174 logic slices

XC2V2000-5=10752 LS's
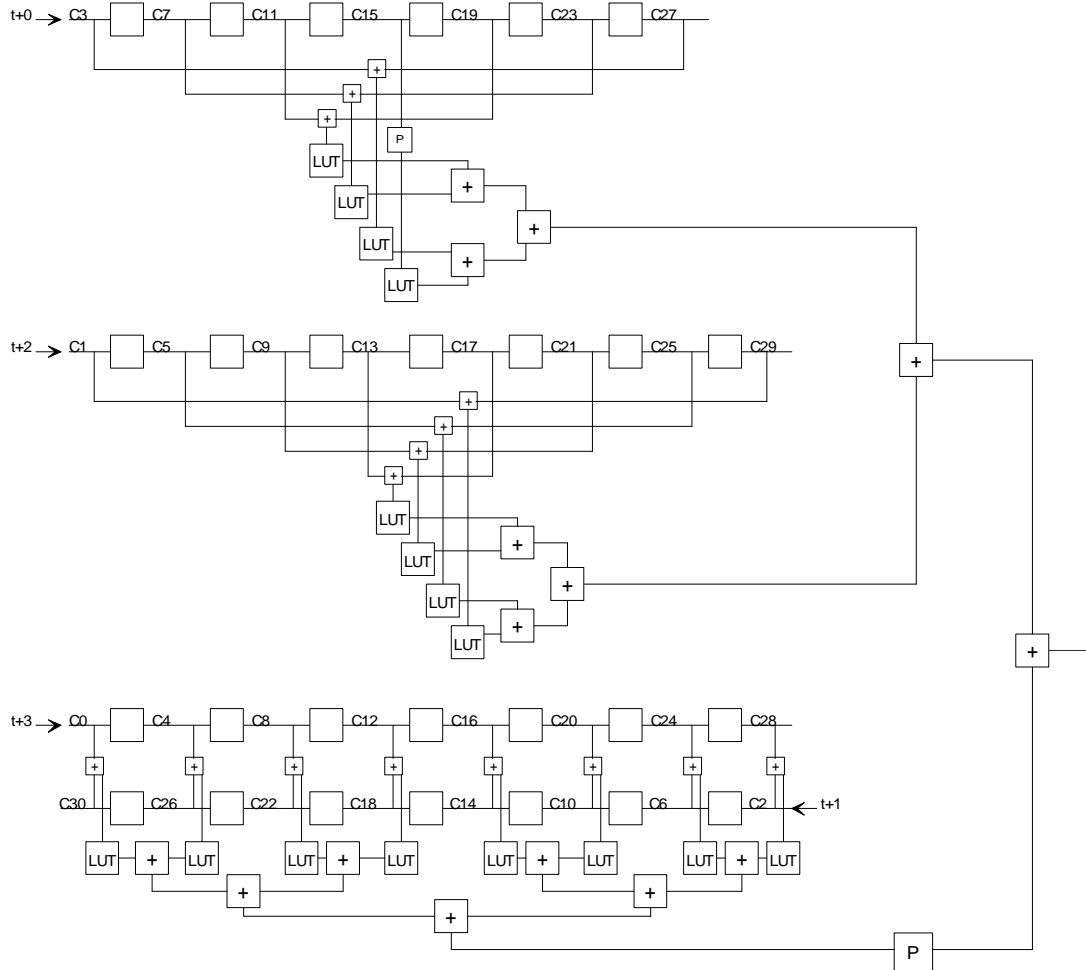
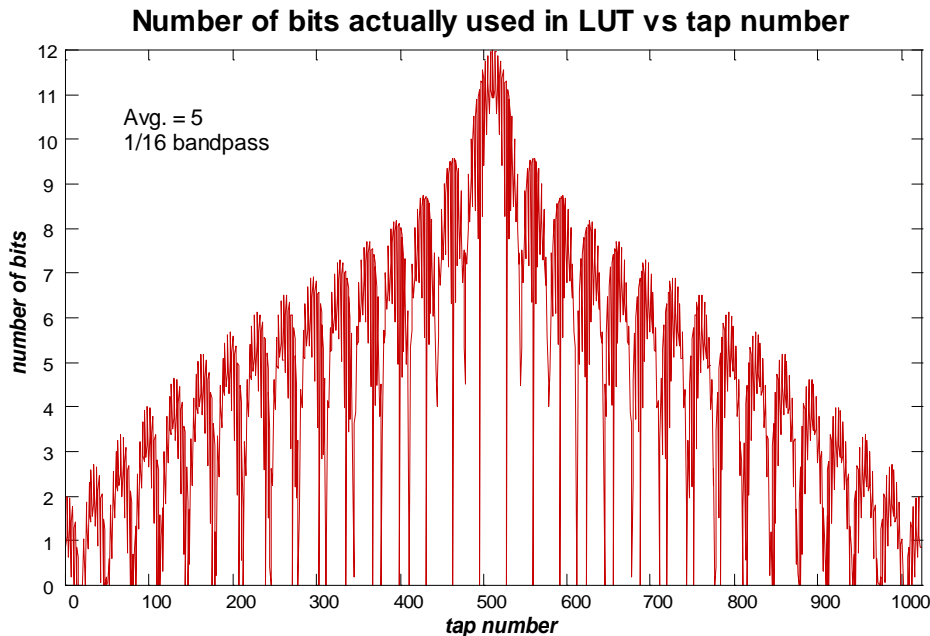and \$431!

Shift regs

adders

LUTs

Adder tree

$$LS = \frac{1}{2} \cdot \left[B \cdot N + \frac{N-1}{2} \cdot (B+1) + L \cdot \left(\frac{N+1}{2} \right) + \frac{N+1}{2} \cdot \left(\sum_{i=1}^{ceil\left(\log_2\left(\frac{N+1}{2} \right) \right)} \frac{(L+i)}{2^i} \right) + B \right]$$

31-tap, poly-phase=4, cosine symmetric FIR

Or…minimum LUT fit

- Fit LUT and adder tree to number of bits used for each tap.
- Requires one design for every set of tap coefficients.
  - *May* be possible/practical with HDL coding of FPGA.
  - **But, savings drop as filter narrows!**: 1/16 avg=5, 1/64 avg=7, 1/256 avg=10

Number of bits actually used in LUT vs tap number

Avg. = 5
1/16 bandpass

number of bits

tap number

For B=3, L=5, N=1023:

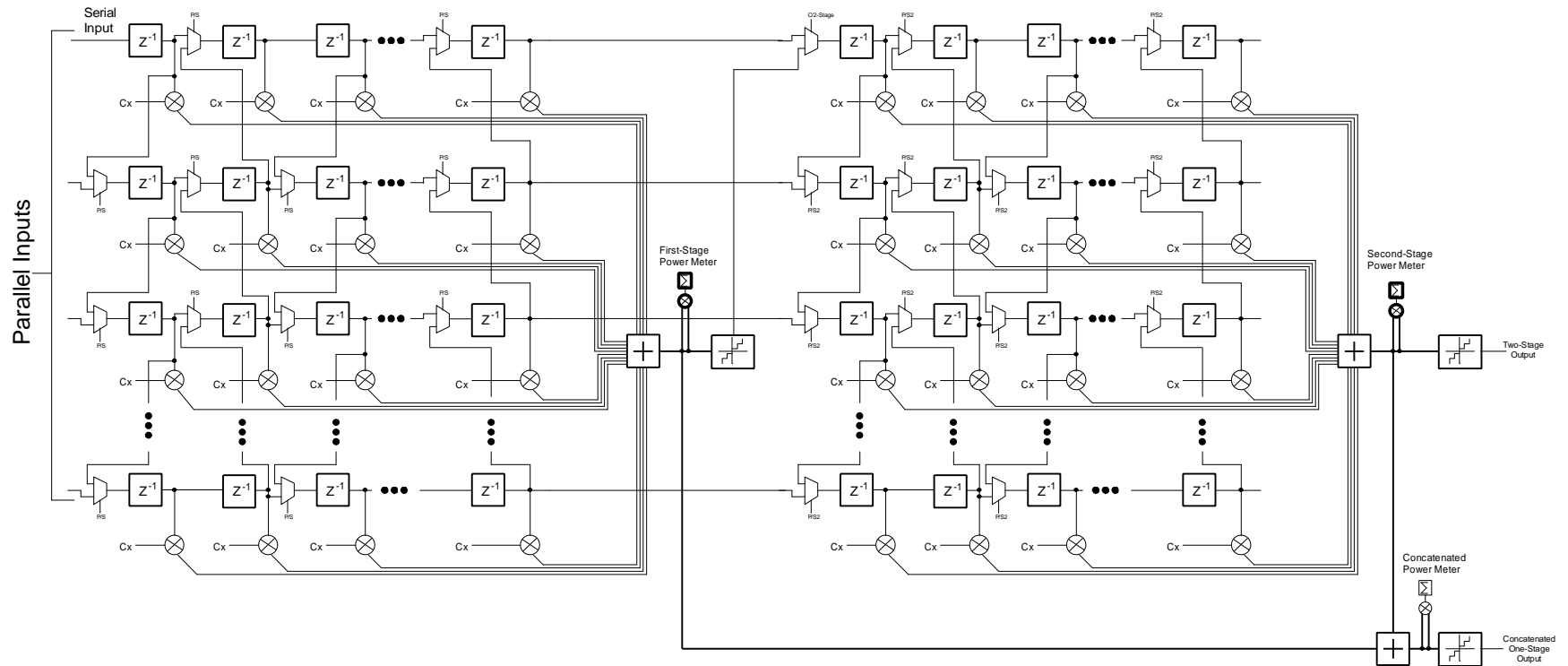LS=5622 logic slices

XC2V1000=5120 LS's

XC2V1500=7680

For B=3, L=5, N=767:

LS=4205 logic slices

XC2V1000=5120 LS's

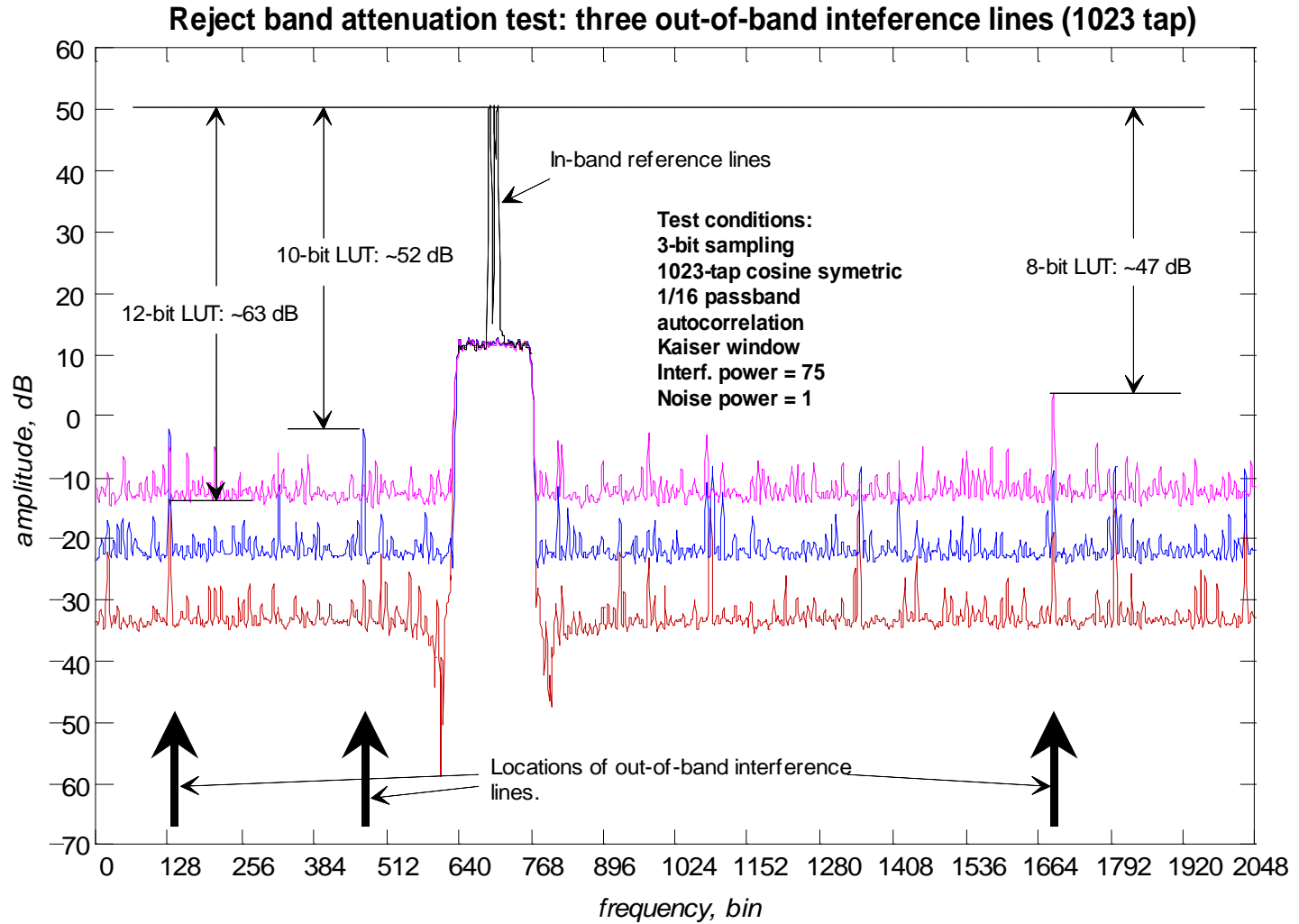![NRC·CNRC]

Or…Gate Array

1023 taps: ~16k logic slices $\equiv$ 4M system gates (Xilinx) $\equiv$ ~32k FF's ~= 200k gates?

(PLUS: dual-port memory for sub-band multi-beaming!)

Reject band attenuation test: three out-of-band inteference lines (1023 tap)

In-band reference lines

Test conditions:
3-bit sampling
1023-tap cosine symetric
1/16 passband
autocorrelation
Kaiser window
Interf. power = 75
Noise power = 1

12-bit LUT: ~63 dB

10-bit LUT: ~52 dB

8-bit LUT: ~47 dB

Locations of out-of-band interference lines.

amplitude, dB

frequency, bin

Reject band attenuation test: one out-of-band inteference line (1023 tap)
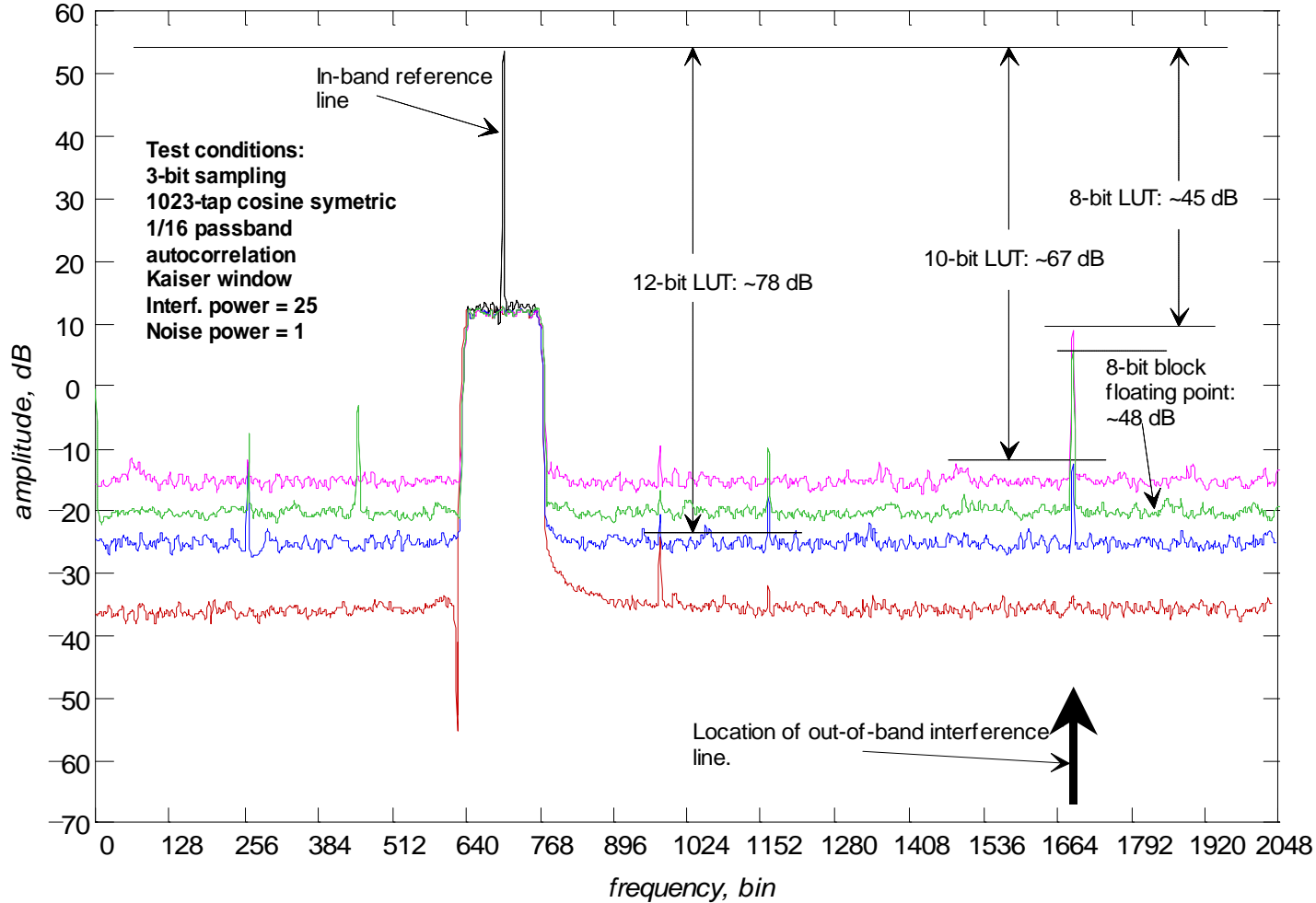
Using "block floating-point" buys ~5 dB better rejection.

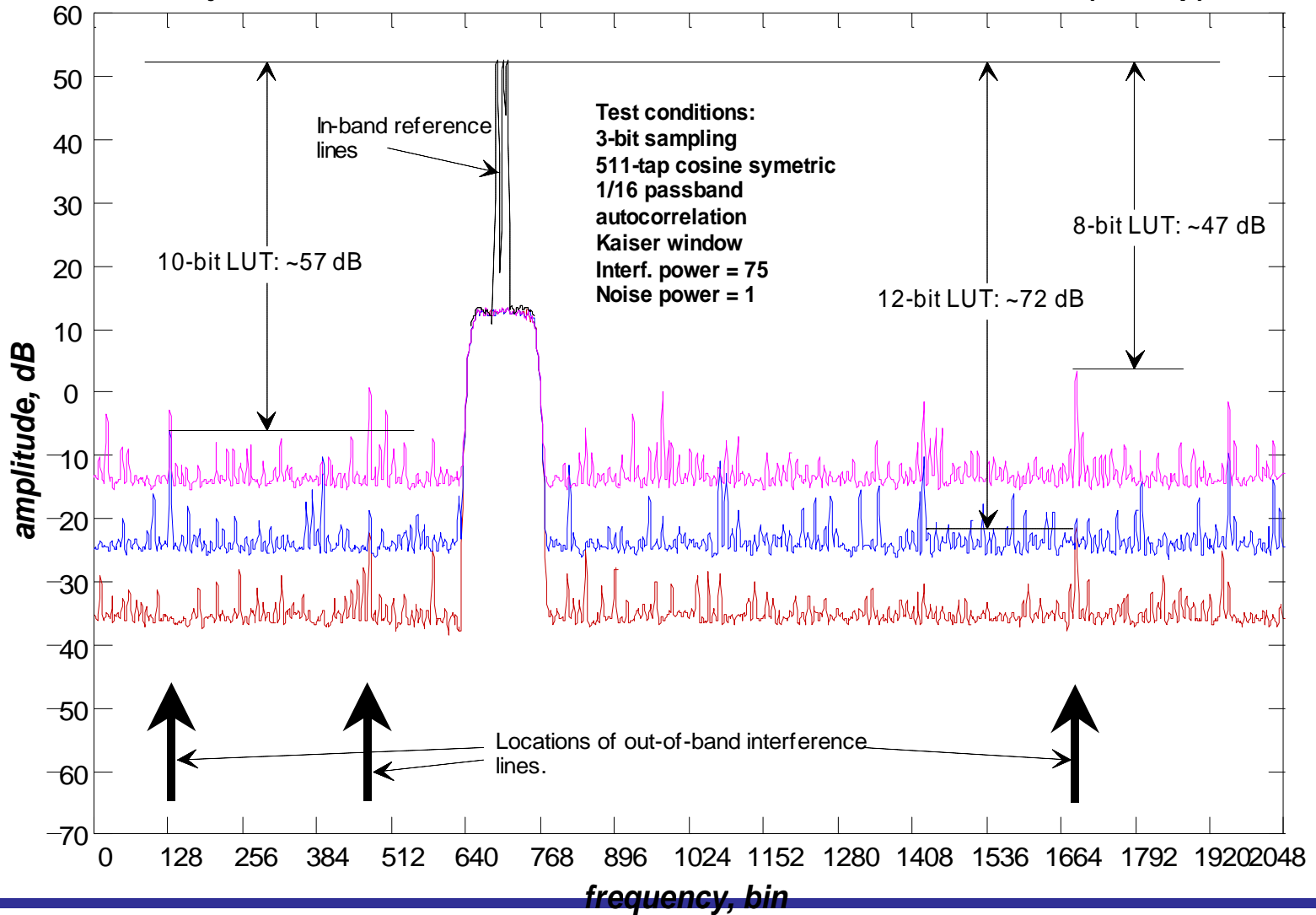**Reject band attenuation test: three out-of-band inteference lines (511 tap)**

In-band reference lines

Test conditions:
3-bit sampling
511-tap cosine symetric
1/16 passband
autocorrelation
Kaiser window
Interf. power = 75
Noise power = 1

10-bit LUT: ~57 dB

8-bit LUT: ~47 dB

12-bit LUT: ~72 dB

Locations of out-of-band interference lines.

amplitude, dB

frequency, bin
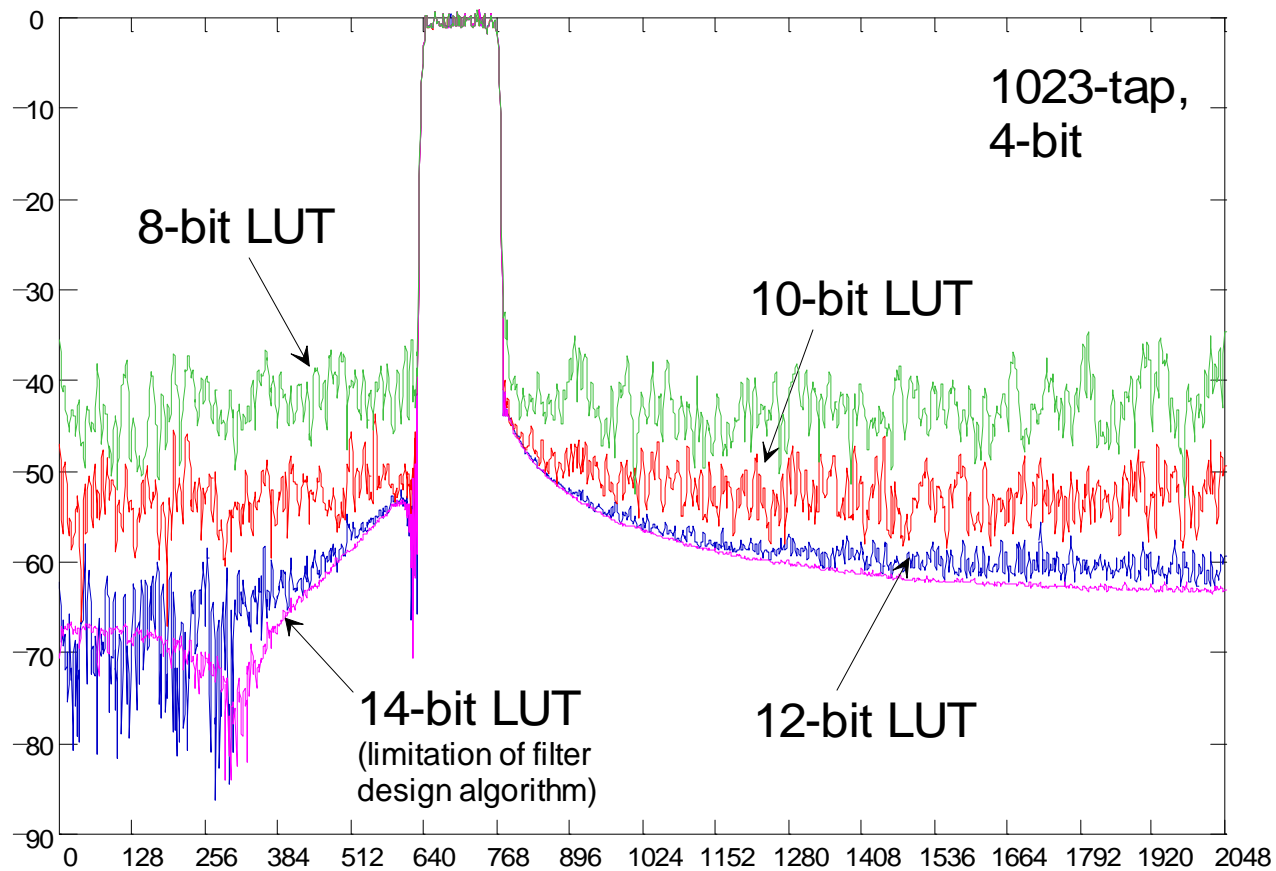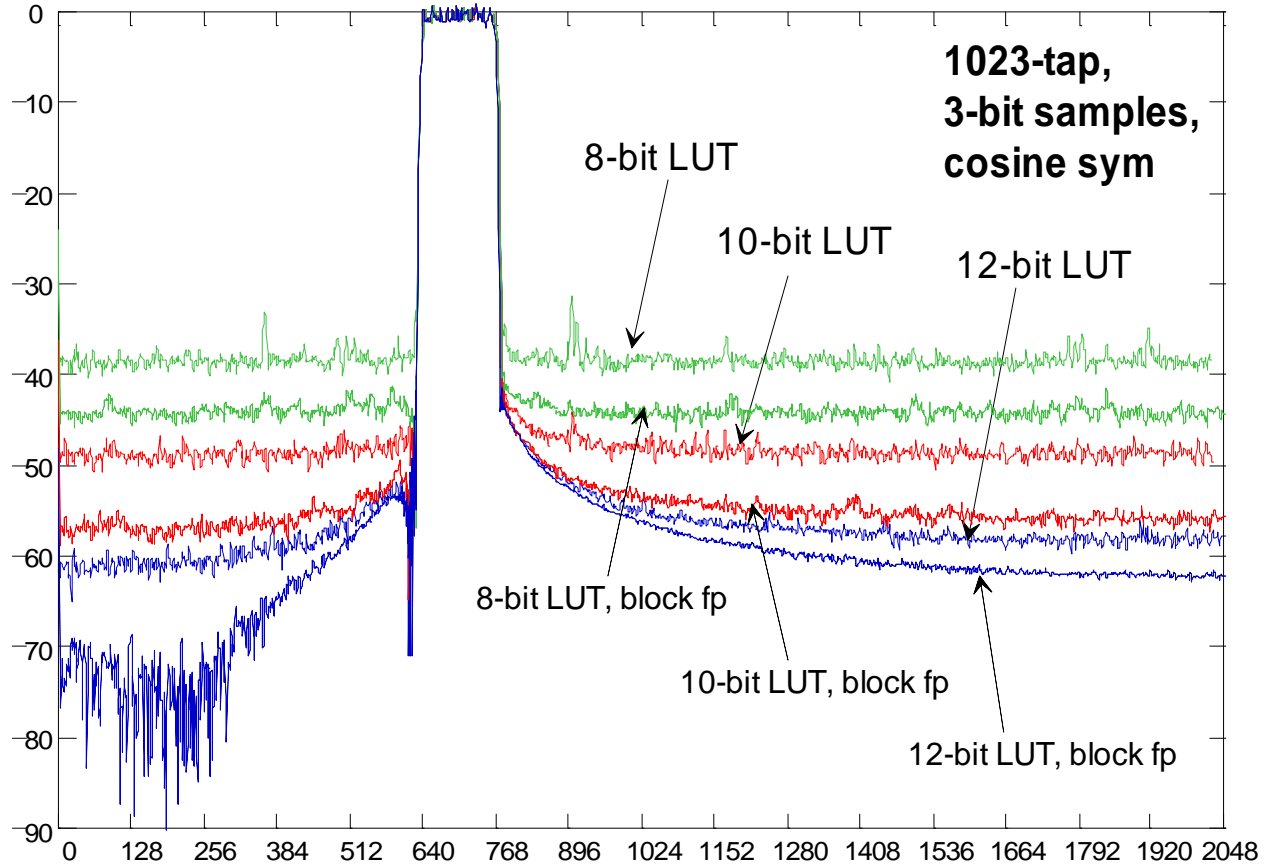
FIR Filter Sub-band Boundary Loss Curves

-1.25 dB cutoff : 1/16 flat bandpass

Dotted line: filter only
Solid line: filter+requant+f. rot loss

255 taps

511 taps

1023 taps

sensitivity loss, %

frequency from sub-band edge in MHz

1/16 bandpass filter responses

128 MHz

amplitude, dB

slot number
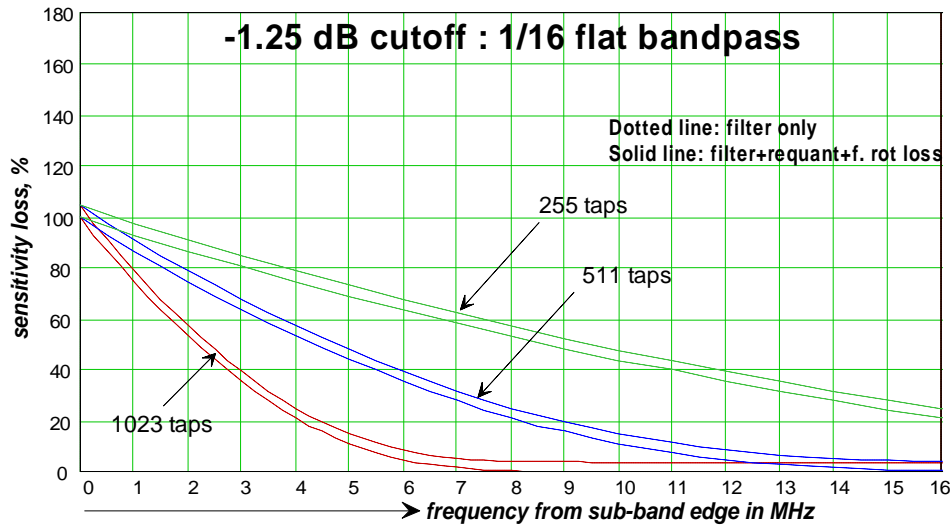
1023 taps, -1.25 dB cutoff has been used for almost all previous testing.

2047 taps would be very nice!

B. Carlson, 2001-Nov-02

EVLA Correlator Conceptual Design Review

16

-13.5 dB cutoff : 1/16 flat bandpass

Dotted line: filter only
Solid line: filter+requant+f. rot loss
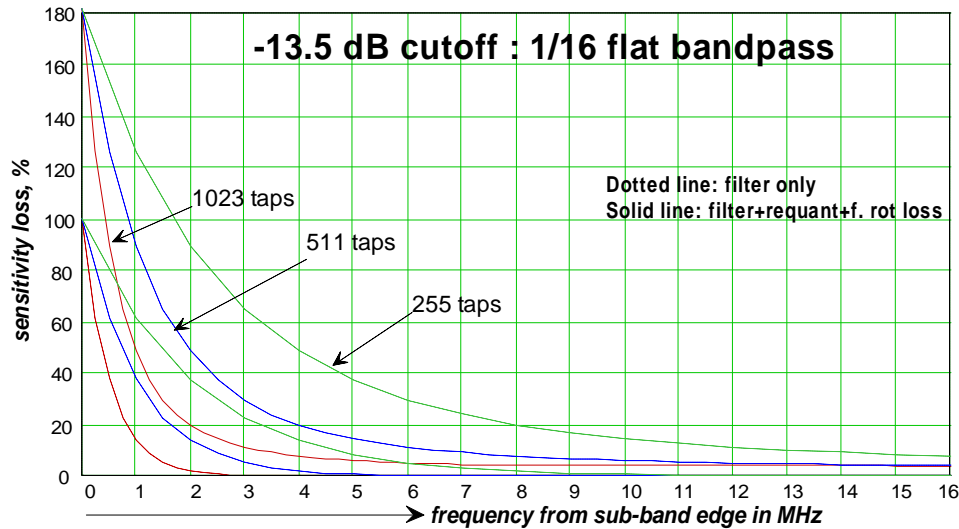
1023 taps

511 taps

255 taps

sensitivity loss, %

frequency from sub-band edge in MHz

**1/16 bandpass
filter responses**

128 MHz

amplitude, dB

slot number
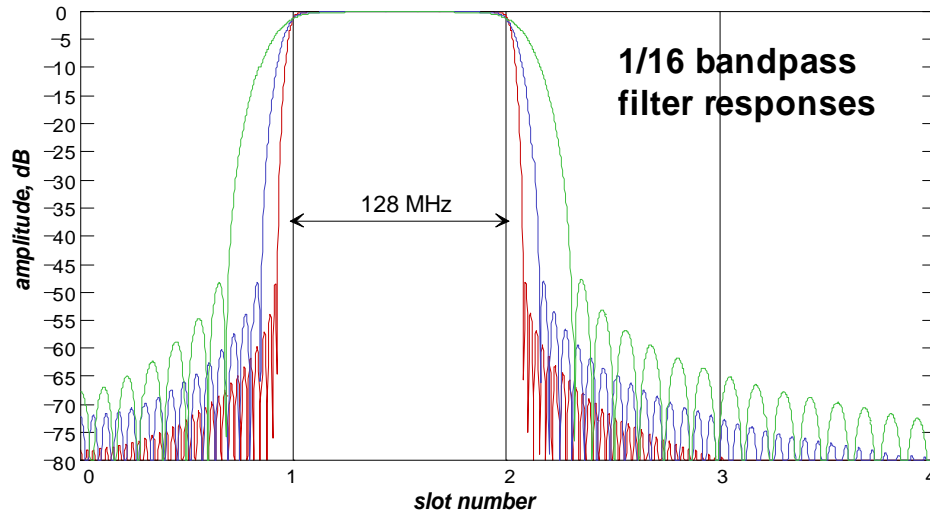
With 1023 taps, ~1 MHz *more* is degraded due to requantization (1.3%) and fringe rotator loss (2.2%). With 511 taps it is ~2.5 MHz more, with 255 taps it is ~4.5 MHz.

B. Carlson, 2001-Nov-02

EVLA Correlator Conceptual Design Review

-25 dB cutoff : 1/16 flat bandpass
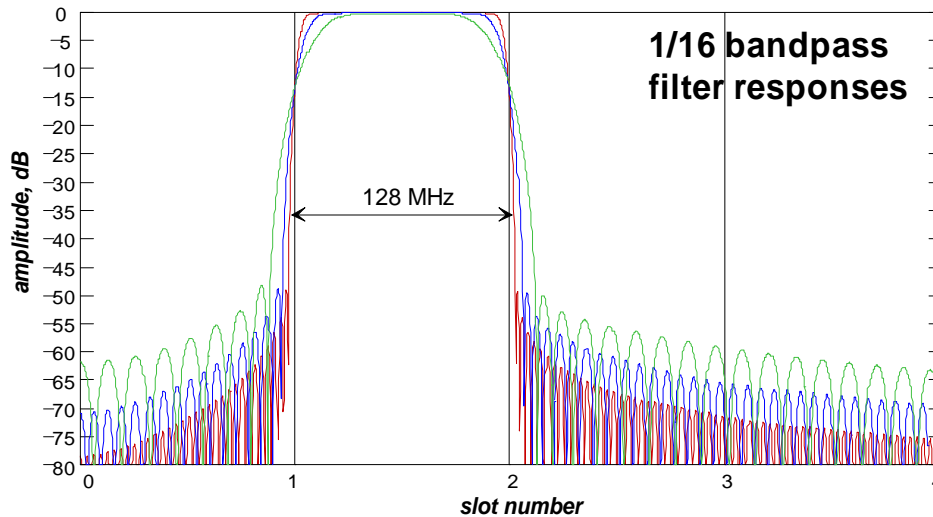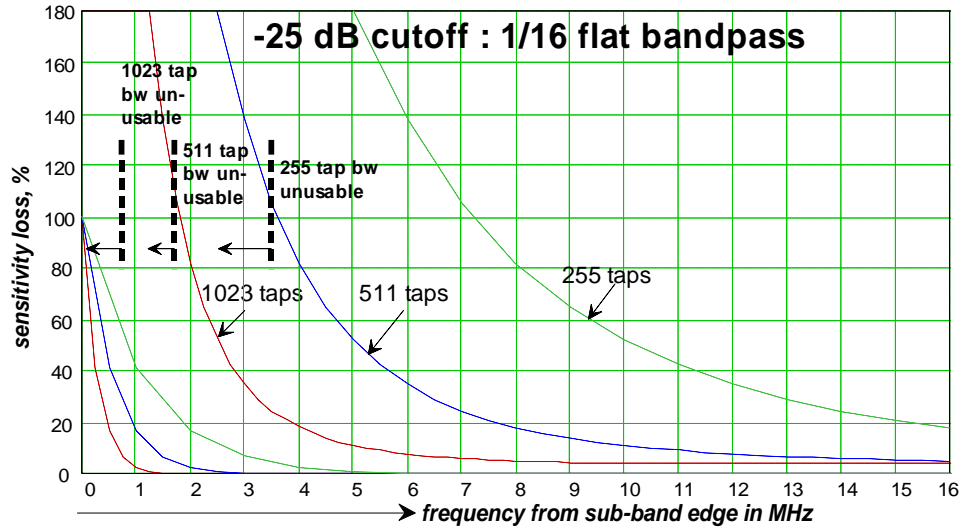
Clearly not acceptable performance.

~-12.5 dB cutoff, 511 taps (no requant or fringe rot. losses)

sensitivity loss, % (vertical axis)

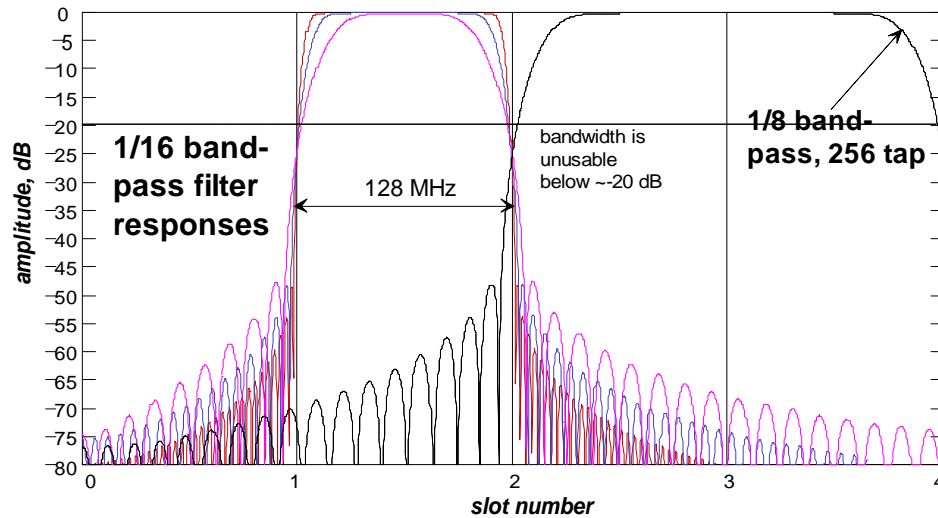*frequency from sub-band edge in MHz* (horizontal axis)

~1.7 dB

amplitude, dB (vertical axis)

128 MHz

1/16 bandpass filter response using "meteor" FIR filter design program, with bandpass ripple

slot number
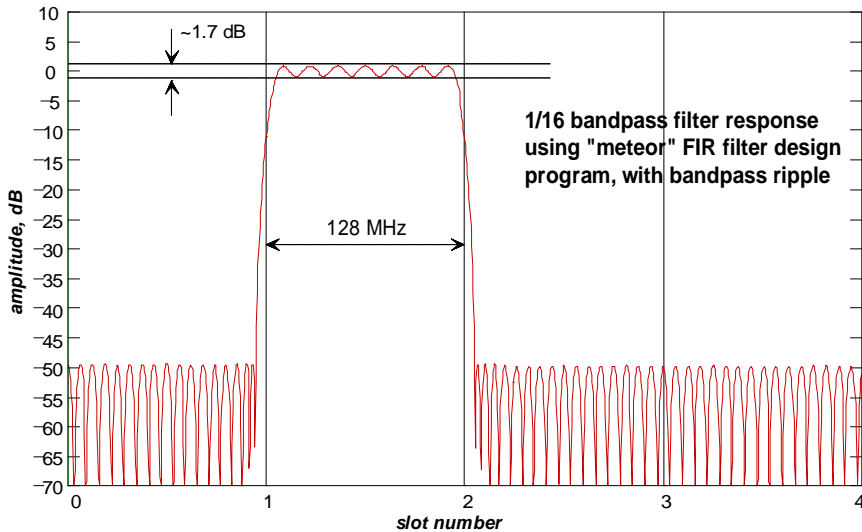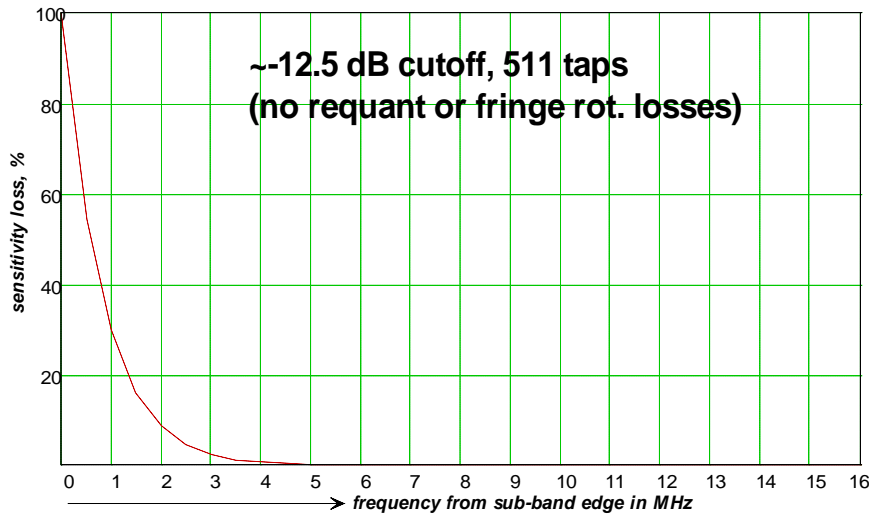
Using the "meteor" FIR filter design program, with ~1.7 dB passband ripple did not yield significantly better performance than the FFT filter design with a flat passband.

Autocorrelation: 10e6 samples, cos symmetric, 12-bit LUT
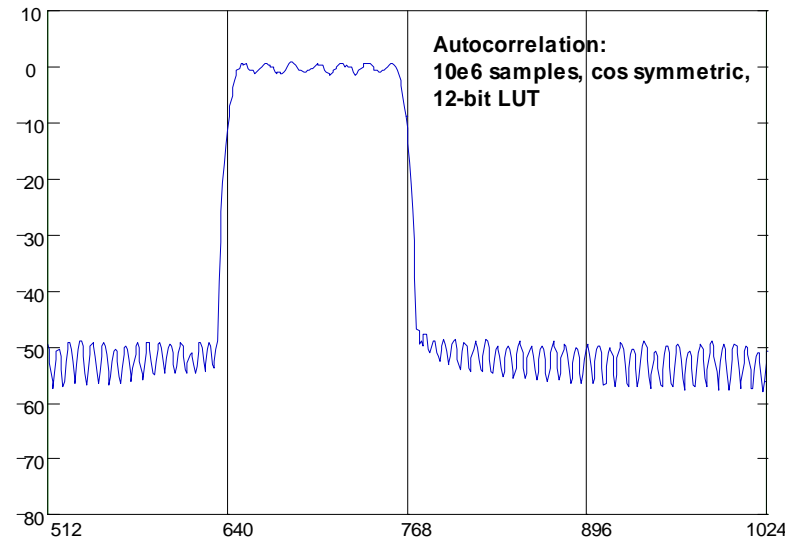
Some attenuation is sacrificed, only 50 dB achieved.

-6 dB cutoff: 1/16 bandpass with +/- 1 dB ripple

511 taps: 1/16 bandpass

1023 taps

511 taps

255 taps

dotted line: filter only
solid line: filter + requant + fr. rot. loss

sensitivity loss, %

frequency from sub-band edge in MHz
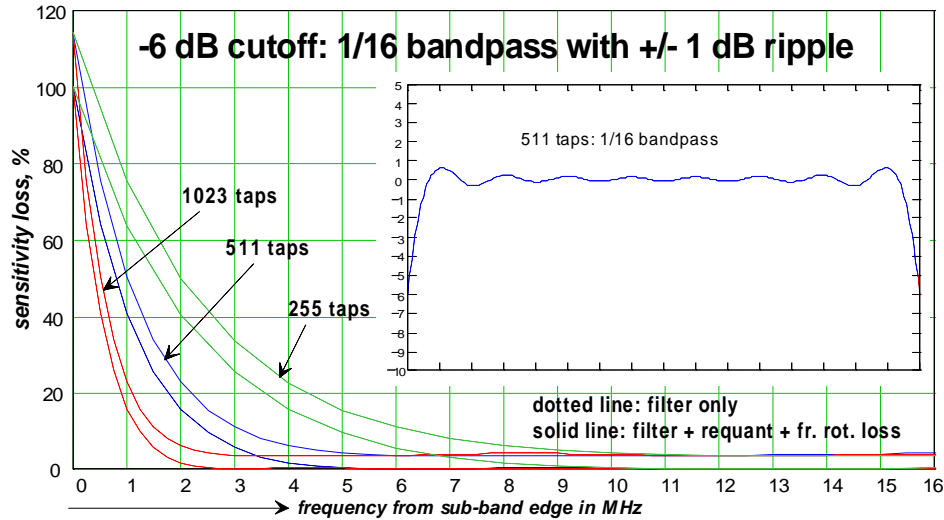
With 511 taps, this *may* be acceptable performance.

1/16 bandpass response using FFT filter design

Doesn't matter: folds over and washes out anyway.

128 MHz

amplitude, dB

slot number

Autocorrelation: 10e6 samples, 511 taps, cos symmetric, 12-bit LUT

After requantization
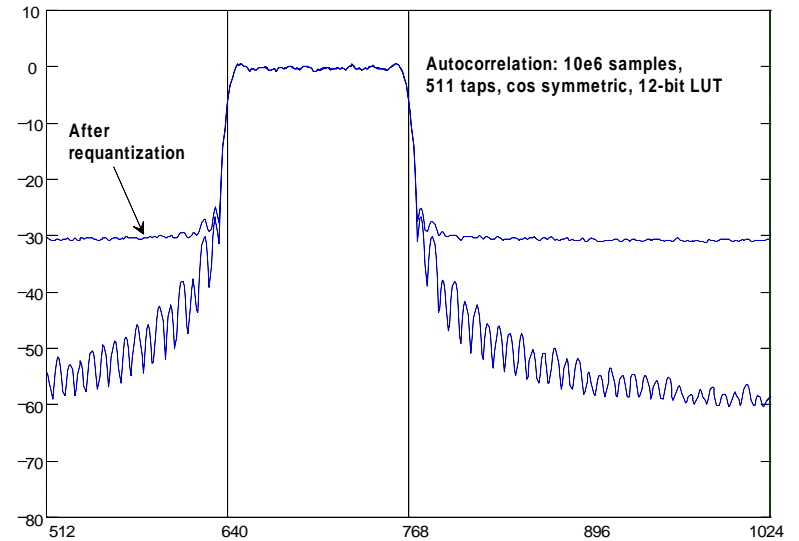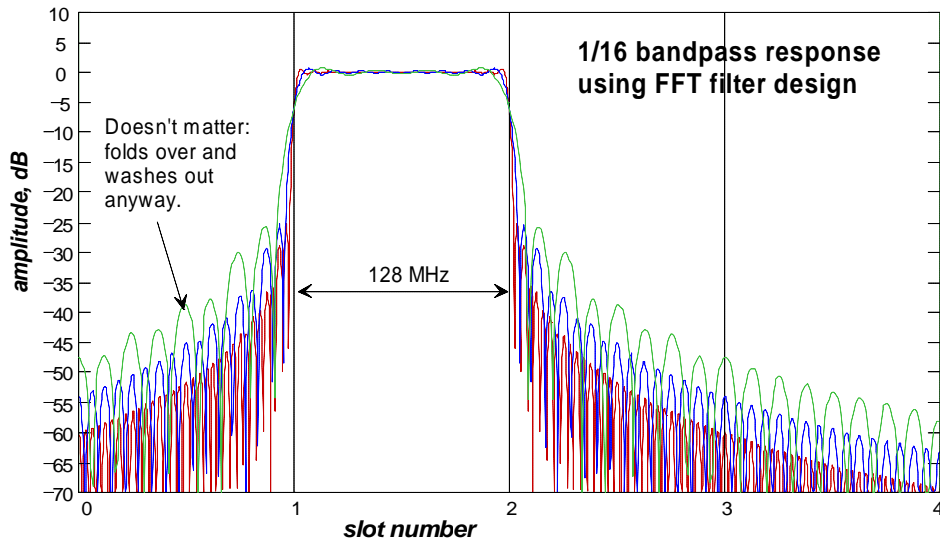
Recirculation

- Use (expensive, $98) DPSRAM (2 x 256k x 18 $\equiv$ 512k x 18).

- Good enough for 256k spectral points.

- Requires 1 msec correlator chip readout.

- Can only afford two data and phase paths:
  - Carry phase with data to simplify phase generation.
  - Allows 4 pol'n products on one baseband.
  - Simultaneous non-recirculation correlation.

- Controlled by DUMPTRIG and Recirculation Controller configuration.
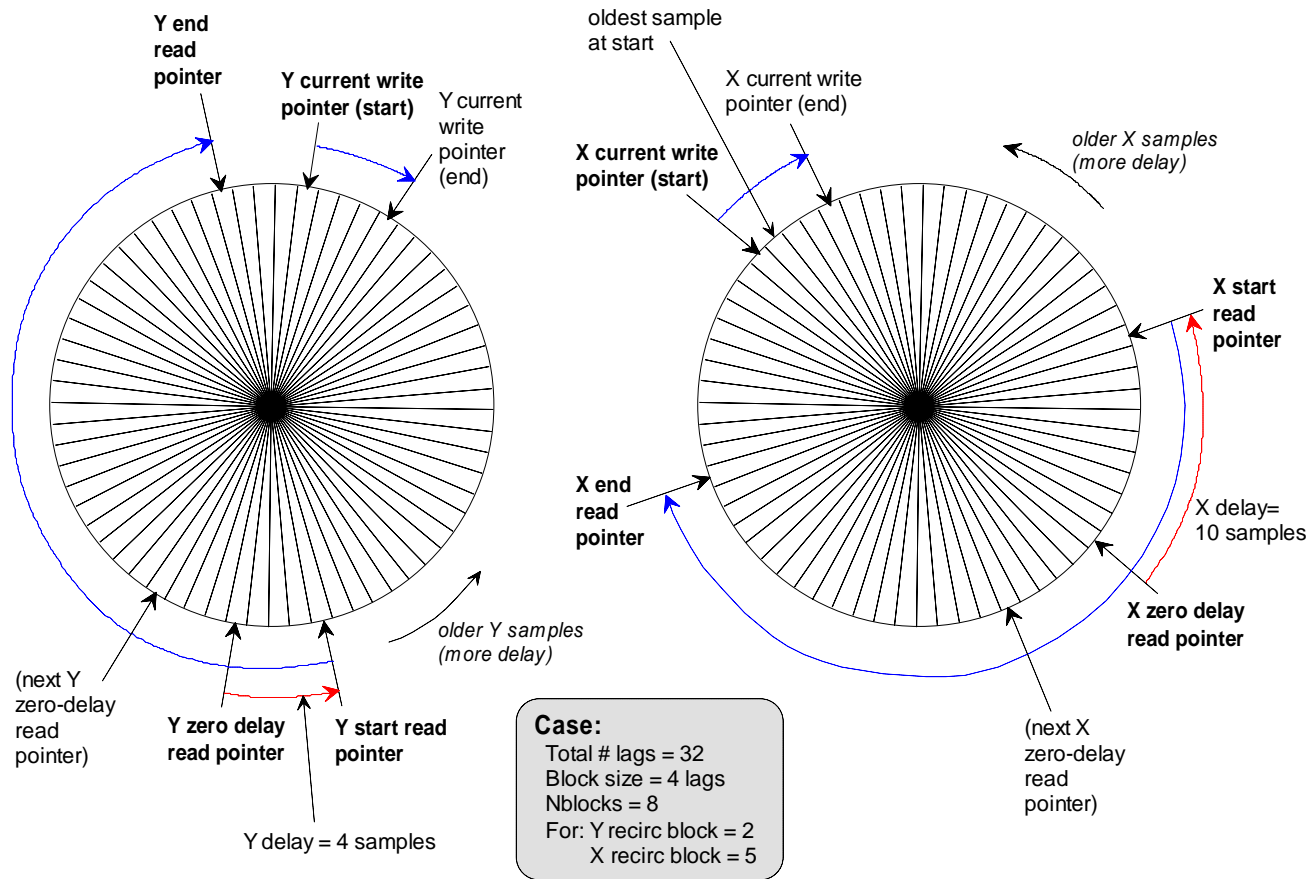
Y-Station Recirculation Buffer

X-Station Recirculation Buffer

Case:
Total # lags = 32
Block size = 4 lags
Nblocks = 8
For: Y recirc block = 2
X recirc block = 5

X-Station Recirculation Buffer - Timestamp Analysis
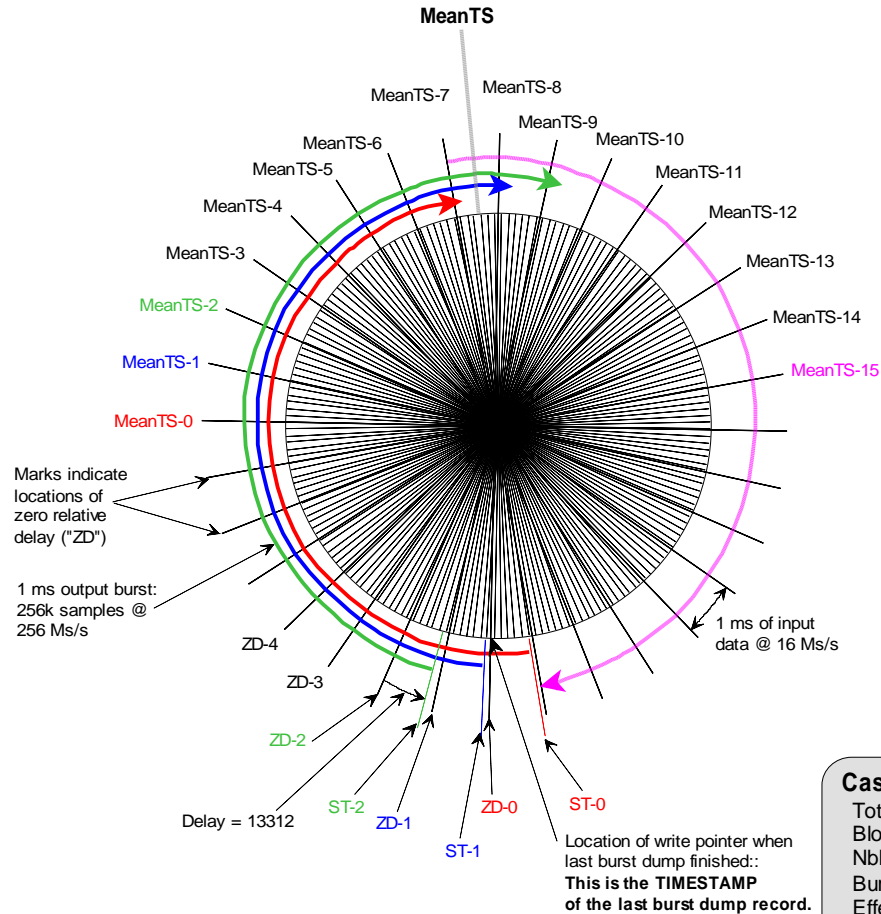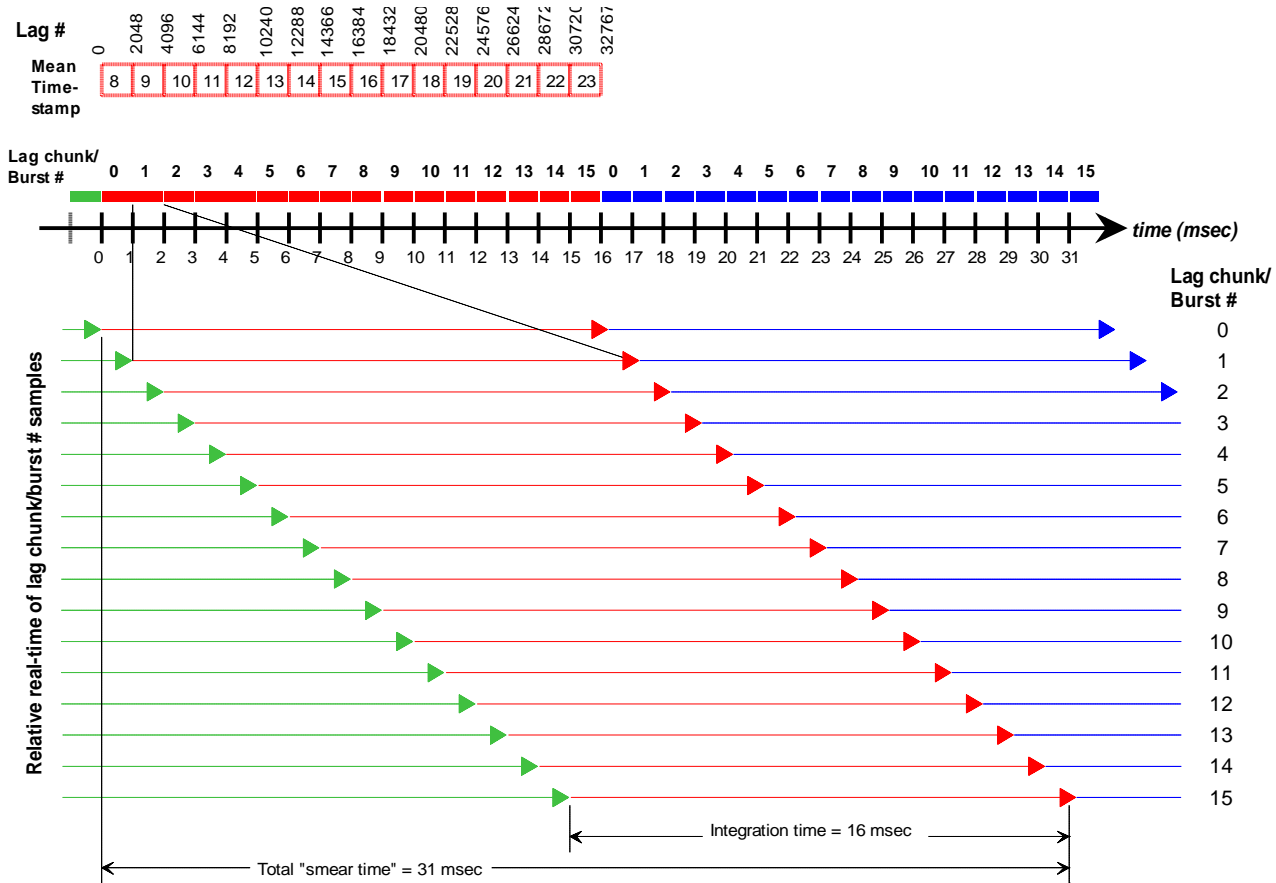
Case:
Total # lags synthesized = 32768
Block size = 2048 lags
Nblocks = 16
Burst readout time = 1 ms
Effective integration time = 16 ms
Sample rate: 16 Ms/s
Buffer size: 512k

Case: 16 x recirculation with original real-time sample rate of 16 Ms/s, 512 k buffer with 256k sample burst size.
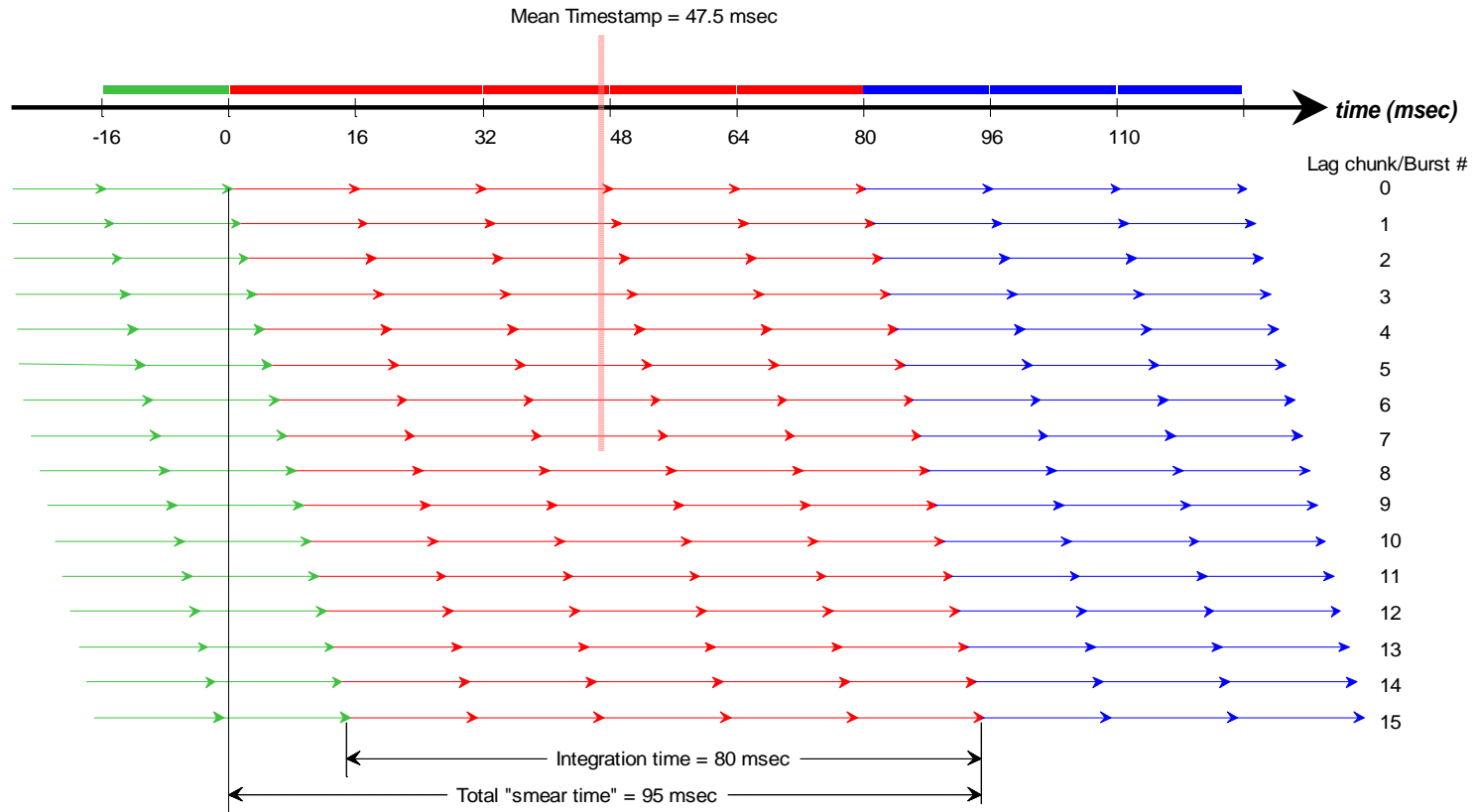
Case: 16 x recirculation with original real-time sample rate of 16 Ms/s, 512 k buffer with 256k sample burst size. 16 msec frame integration; total integration time 80 msec; "smear time" 95 msec.

DUMPTRIG: 16X recirculation, no pulsar phase binning
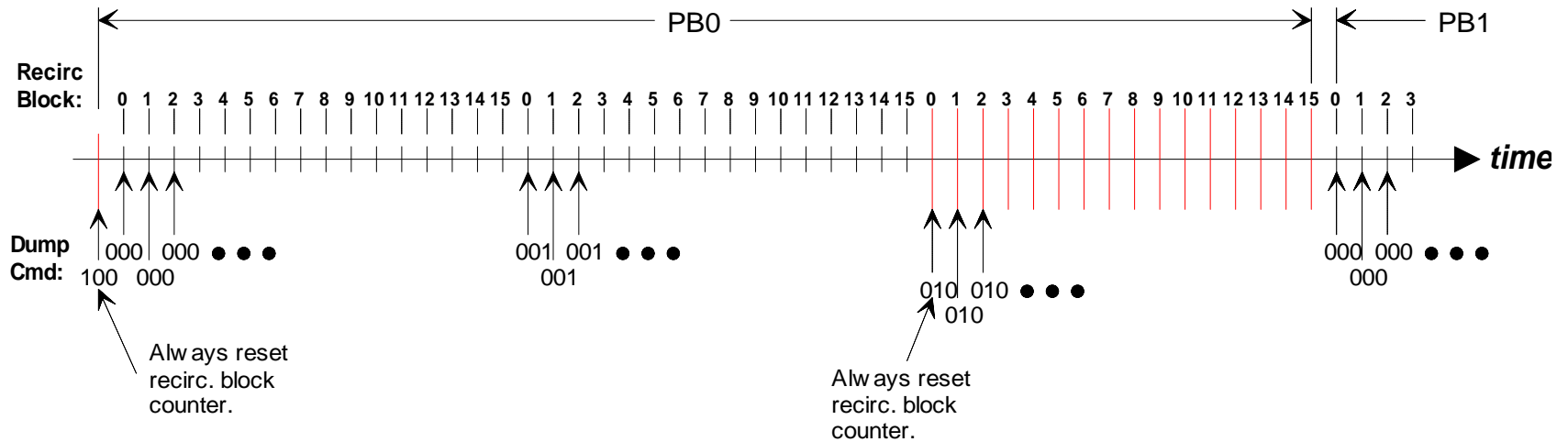
Each "recirculation block" must have its own bin to accumulate into. Thus, there are logical blocks/dumps and logical pulsar time/phase bins that map into physical bins in the LTA.
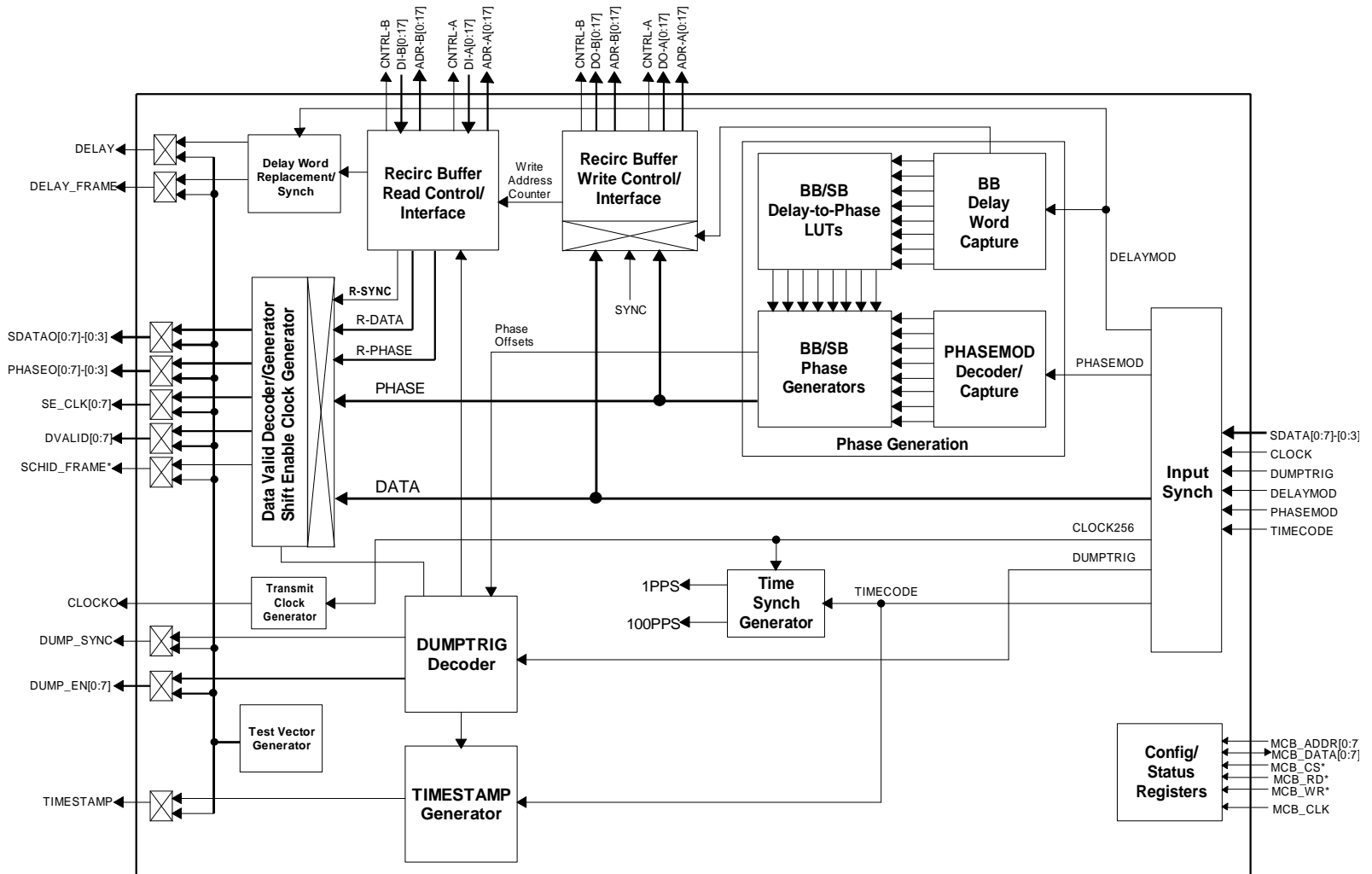
Recirculation Controller FPGA Simplified Block Diagram

Recirculation Controller to Correlator Chip Functional Timing
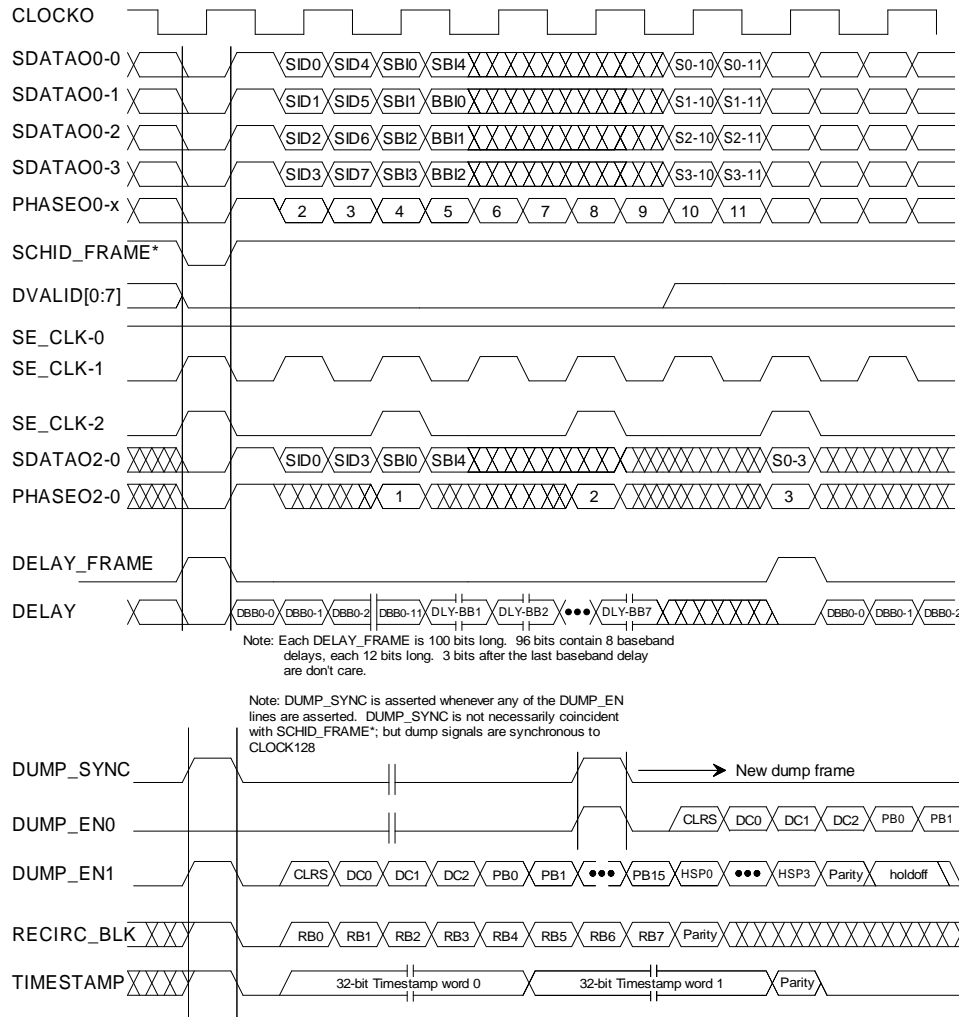
DUMP_EN control bits:

CLRS: If set, then the output of the lag chain shift registers is cleared.

DC2	DC1	DC0	ACTION
0	0	0	First dump of data into LTA. Just save data in LTA bin.
0	0	1	Add data to existing LTA data and save in LTA bin.
0	1	0	Last dump: add to LTA data; flag LTA bin as ready.
0	1	1	Speed dump: bypass LTA directly to output. The data bias is removed.
1	0	0	Dump data and discard it.

PB[0:15] Phase bin number for this particular dump.

HSP[0:3] Harmonic suppression phase. This 4-bit phase has been added to the PHASE data and must be removed by the LTA controller. This suppresses harmonics of strong narrowband interference and can be turned on or off by a control register in the recirculation controller. The correlator chip simply passes this phase data onto the LTA controller.

RECIRC_BLK and TIMESTAMP are for the data dump that just occurred.

TIMESTAMP word 0: bits 0 - 31: number of seconds since last epoch.
TIMESTAMP word 1: bits 0 - 28: number of clocks since last PPS
bits 29 - 31: major epoch.

Correlator Chip

- Plan 2048 complex-lag chip, 4-bit/16-level multipliers, 5-level fringe rotation.

- Specialized interfaces and control for high-performance.

- Knows very little about recirculation…passes information from the Recirculation Controllers onto the LTA controller via the output data frame.

- 16 x 128 complex-lag chip. Each 128 c-lag section is individually controlled and *always* has its own output data frame.

  - Homogeneous, simple, and fast operation.

EVLA Correlator Conceptual Design Review

LTA controller interface

DATA_CS*, DATA_RDY*, ACCDATA[0:31], DATA_OE*, DATA_CLKIN, DATA_CLKOUT, DATA_VALID*, FRAME_ABORT*

Correlator Chip

MCB interface

MCB_ADDR[0:6] — 7
MCB_DATA[0:7] — 8
MCB_CS*
MCB_RD*
MCB_WR*
MCB_CLK

X-station inputs

X-SDATAO[0:7]-[0:3] — 8x4
X-PHASEO[0:7]-[0:3] — 8x4
X-SE_CLK[0:7] — 8
X-DVALID[0:7] — 8
X-SCHID_FRAME*
X-DELAY
X-DELAY_FRAME
X-DUMP_SYNC
X-DUMP_EN[0:7] — 8
X-RECIRC_BLK
X-TIMESTAMP
CLOCK — 2

Y-station inputs

Y-TIMESTAMP, Y-RECIRC_BLK, Y-DUMP_EN[0:7], Y-DUMP_SYNC, Y-DELAY_FRAME, Y-DELAY, Y-SCHID_FRAME*, Y-DVALID[0:7], Y-SE_CLK[0:7], Y-PHASEO[0:7]-[0:3], Y-SDATAO[0:7]-[0:3]

Simplified Correlator Chip Quad (CCQ) Block Diagram

Center Lag = N/2

Complex lags

Correlator Chip Output Data Frame:

	28	24	20	16	12	8	4	0	
SYNCH	1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0								W0

STATUS BITS	Reserved	CCID	HSP-Y	HSP-X	Cmmd	W1

BBID-Y	BBID-X	SBID-Y	SBID-X	SID-Y	SID-X	W2

LTA (Phase) BIN	RECIRC_BLK-Y	RECIRC_BLK-X	W3

DVCOUNT-Center	W4
DVCOUNT-Edge	W5
DATA_BIAS	W6
TIMESTAMP-0	W7
TIMESTAMP-1	W8
Lag 0-In_phase accumulator	W9
Lag 0-Quadrature accumulator	W10
Lag 1-In_phase accumulator	W11
Lag 1-Quadrature accumulator	W12
• • •	W13-261
Lag 127-In_phase accumulator	W262
Lag 127-Quadrature accumulator	W263

SYNCH	0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0	W264

Parity Check	W265

LTA Controller

- One per corr. chip in FPGA (or, one per 4 corr. Chips)

- Corr. Chip data frame tells the LTA Controller what to do with it, and exactly where to put it.
  - But, LTA Controller is smart enough not to overwrite good data waiting for output.
  - Smart enough for burst operation.
  - "Speed dump" by-passes LTA RAM...straight to output.

- Use 128 MHz readout so cheap, slow-speed-grade FPGA can be used.

- Transmits ready data on local FPDP bus…that flows to output FPDP interface.
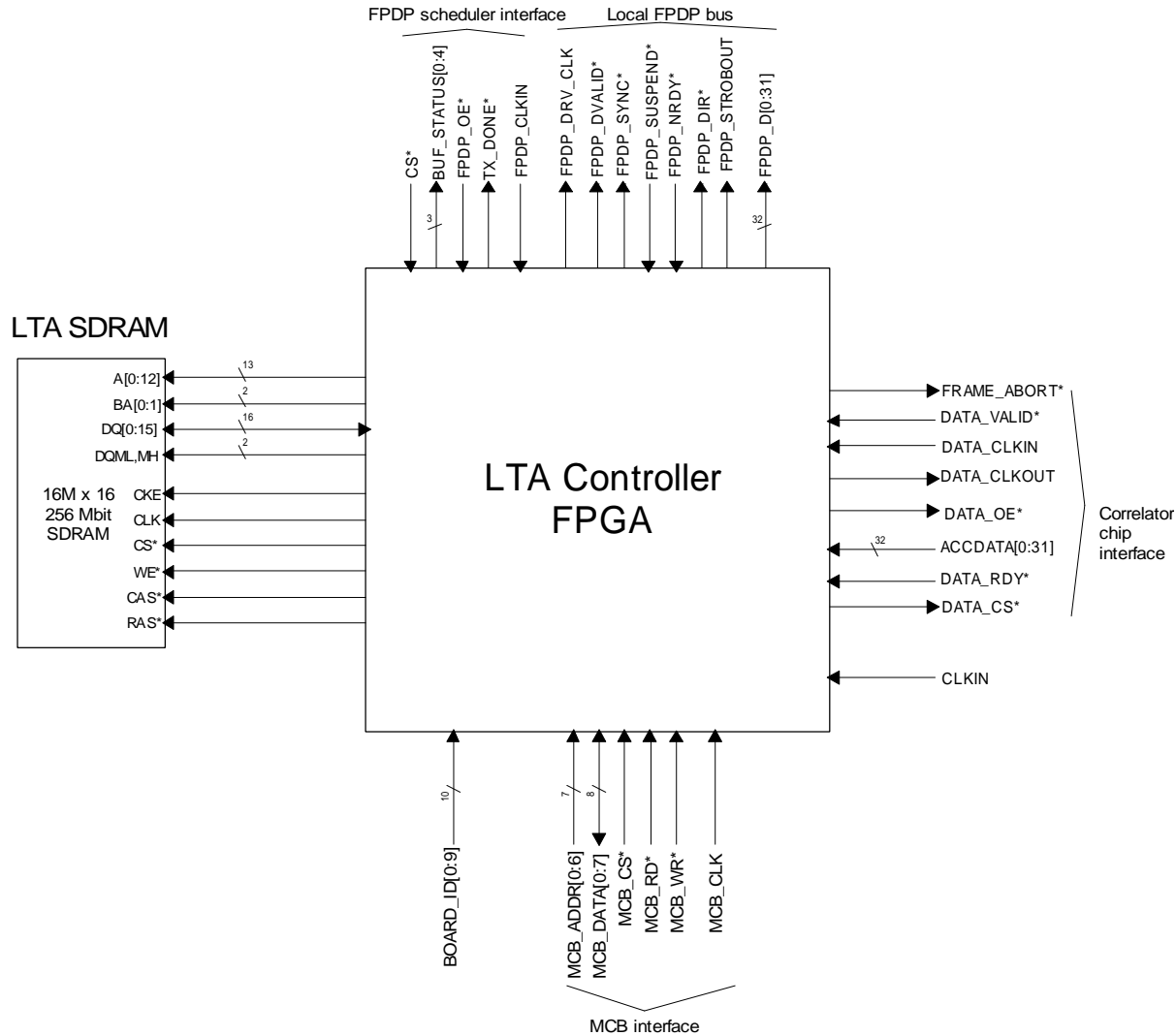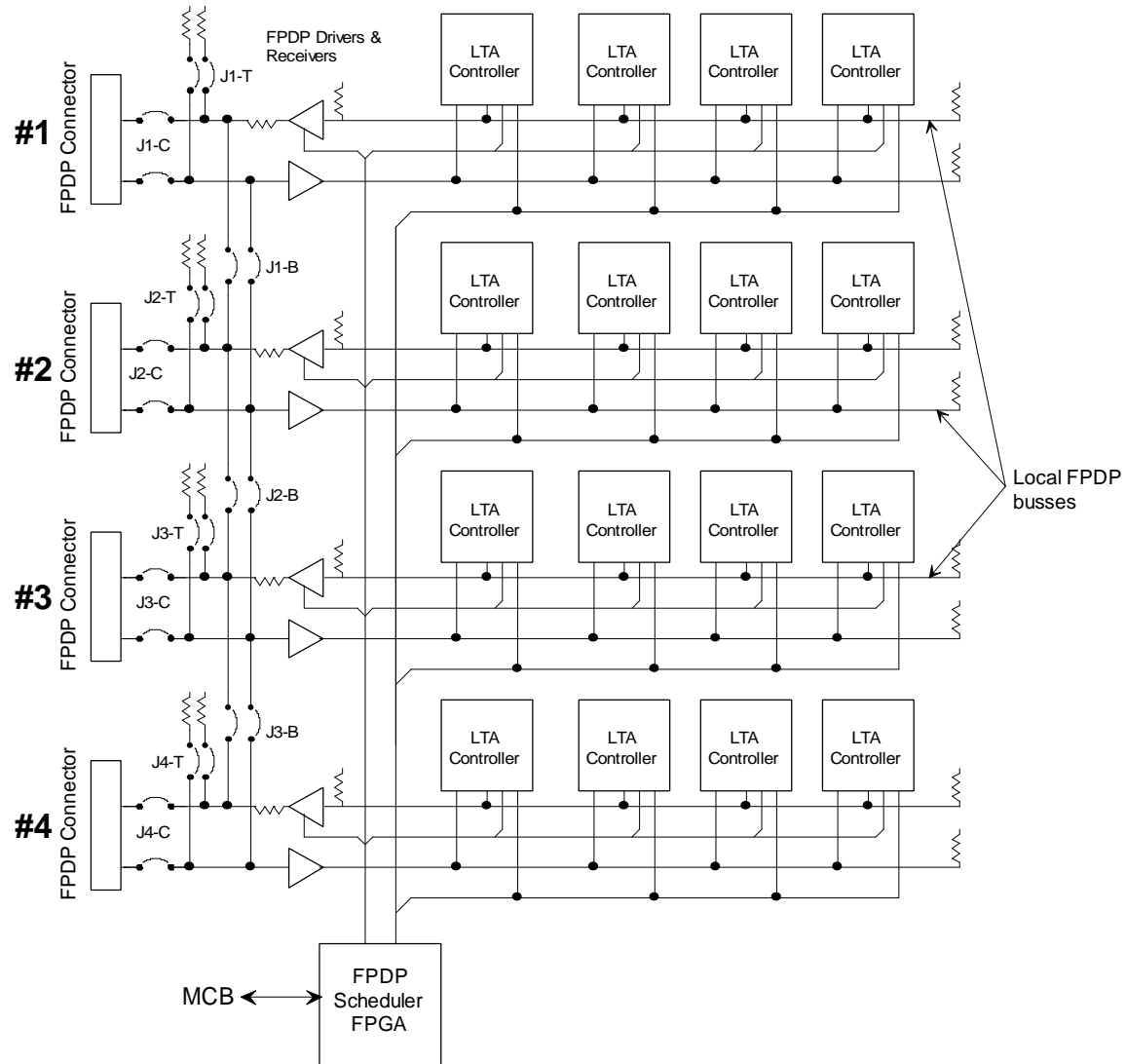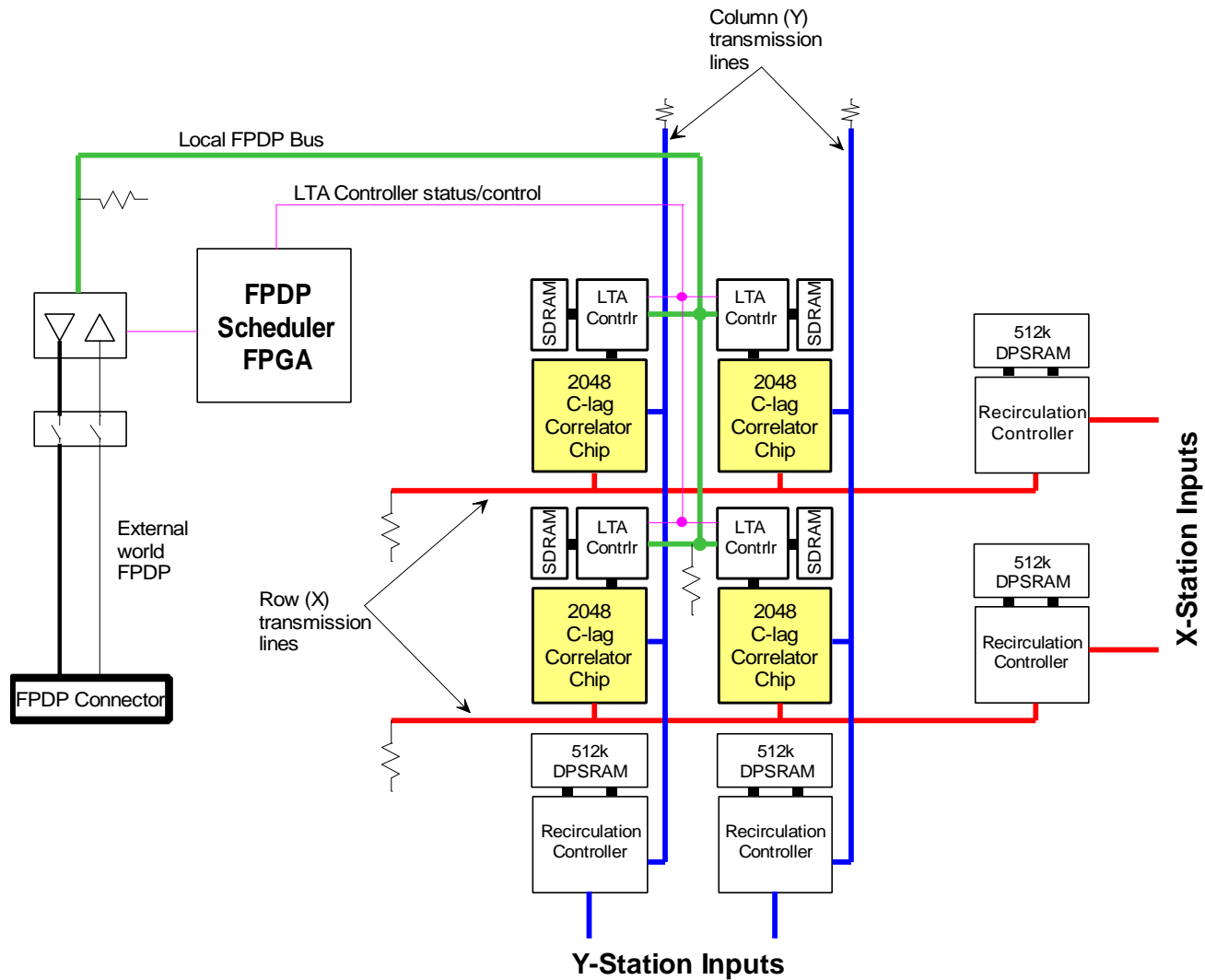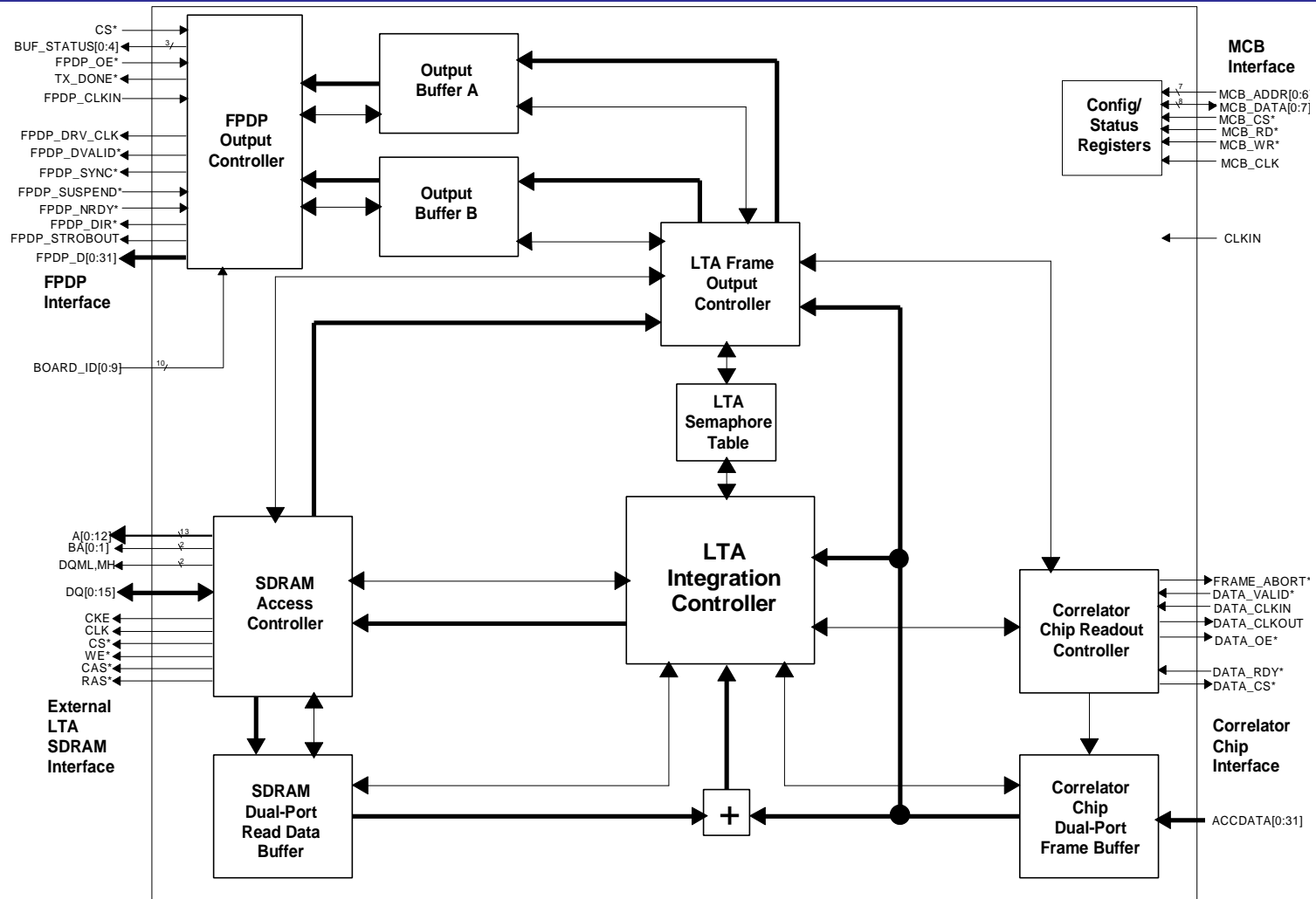
LTA Controller FPGA Functional Block Diagram

LTA Controller: FPDP Normal Output Data Frame

	28	24	20	16	12	8	4	0	
SYNCH	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1								W0

DATA_BIN#		Reserv	ChipID	CCID	FType	W1
BBID-Y	BBID-X	SBID-Y	SBID-X	SID-Y	SID-X	W2
STATUS BITS	FRAME_COUNT	RECIRC_BLK-Y	RECIRC_BLK-X			W3
DVCOUNT-Center						W4
DVCOUNT-Edge						W5
Reserved						W6
TIMESTAMP-0						W7
TIMESTAMP-1						W8
Lag 0-In_phase accumulator						W9
Lag 0-Quadrature accumulator						W10
Lag 1-In_phase accumulator						W11
Lag 1-Quadrature accumulator						W12
● ● ●						W13-261
Lag 127-In_phase accumulator						W262
Lag 127-Quadrature accumulator						W263
SYNCH 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1	Board ID					W264
CHECKSUM						W265

LTA Controller: FPDP "Speed Dump" Data Frame

Bit	28	24	20	16	12	8	4	0	Word

SYNCH: `0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1` — W0

STATUS BITS	Reserv.	ChipID	CCID	HSP-Y	HSP-X	FType	W1

BBID-Y	BBID-X	SBID-Y	SBID-X	SID-Y	SID-X	W2

Phase BIN#	RECIRC_BLK-Y	RECIRC_BLK-X	W3

DVCOUNT-Center	W4
DVCOUNT-Edge	W5
DATA_BIAS	W6
TIMESTAMP-0	W7
TIMESTAMP-1	W8
Lag 0-In_phase accumulator	W9
Lag 0-Quadrature accumulator	W10
Lag 1-In_phase accumulator	W11
Lag 1-Quadrature accumulator	W12
● ● ●	W13-261
Lag 127-In_phase accumulator	W262
Lag 127-Quadrature accumulator	W263

SYNCH: `0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1 1` Board ID — W264

CHECKSUM	W265

This Just In ...

FIR Filter Chip

- AMI semiconductor FPGA-to-gate array conversion (0.18 μm --full production capacity available Dec. 2001).
  - NRE: $200k (XCV2000E-8 [1024 taps, 4-bit])
  - per chip cost: $50 (10k piece pricing…5k piece pricing unavailable).
  - 13-16 weeks lead-time for straight conversion.

- Total FIR cost: ~$430k (save up to $500k).

- Some loss of flexibility because no longer programmable, but design is still very flexible.

Correlator Chip

- AMI semiconductor could convert FPGA design to 0.18 μm gate array and scale up the number of lags.
  - Cost: NRE $200k, $50 each in 10k quantities.
- Could build prototype correlator chip in FPGA and do a conversion from the FPGA design to gate array.
  - Can test and debug design fully with tools now being purchased.
  - Eliminates need for development using full custom toolsets.
  - Drop-in the full custom chip (footprint compatible).
- The big question is power…is gate array capable???
  - Must get serious answers before any decision is made.
- Potential savings: ~$300k (over the *budgeted* $1 million).

Correlator Chip

- THIS PAGE CONFIDENTIAL

High-Speed Cabling

- "Woven Electronics" cable with MDR-80 connector:
  - 3 m: roughly $100-$125 each in 3k quantity (GORE: $268 ea). **Save: ~$400k**.
  - 13 m: waiting for quotation (Guess ~$230). **Save: ~$160k**.
  - Will work on cable configuration to meet our requirements…probably flat cable...have access to expanded PTFE as well…not just normal Woven Electronics flat cable.
  - May require "relaxed" Baseline Rack cable routing.

Modified Baseline Rack Cabling
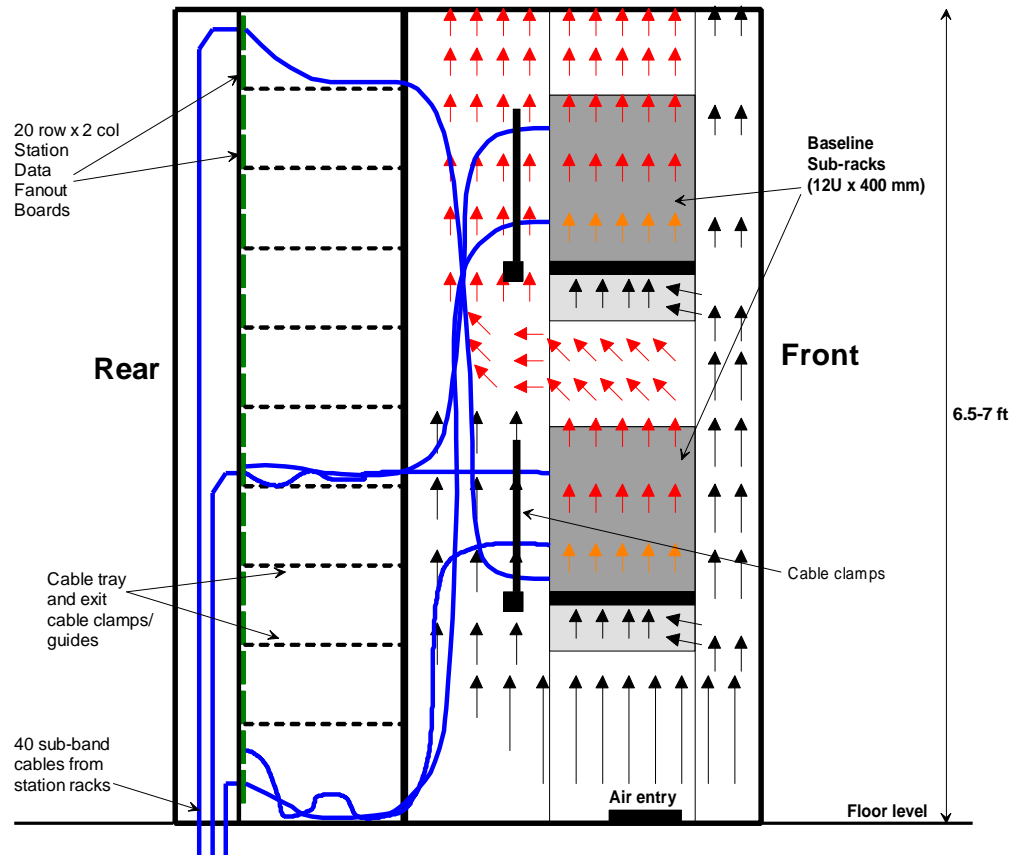
Recirculation Memory

- 256k x 36-bit IDT memory now available for ~$82.

- Could allow *full* performance recirculation on 2 pairs (no phase jitter, 4-bit data).

- Could allow *reduced* performance recirculation on all 8 basebands (8x3 + 8 + 2 = 34 bits), but with 3-bit data (and 4/fs phase jitter?).

- **BUT**: for I/O, requires a 600E-8 FPGA ($263 vs current $143 for 400E-8). **Total extra cost: ~$300k**.

Summary

- FIR savings (~$500k) + cable savings (~$500k) + correlator chip savings (~$300k) = $1.3 million.

- Total project cost $10.4 million, including $1.4 million contingency.

- Improved recirculation width costs *additional* ~$300k.