VLA EXPANSION PROJECT

Architecture Walk-through

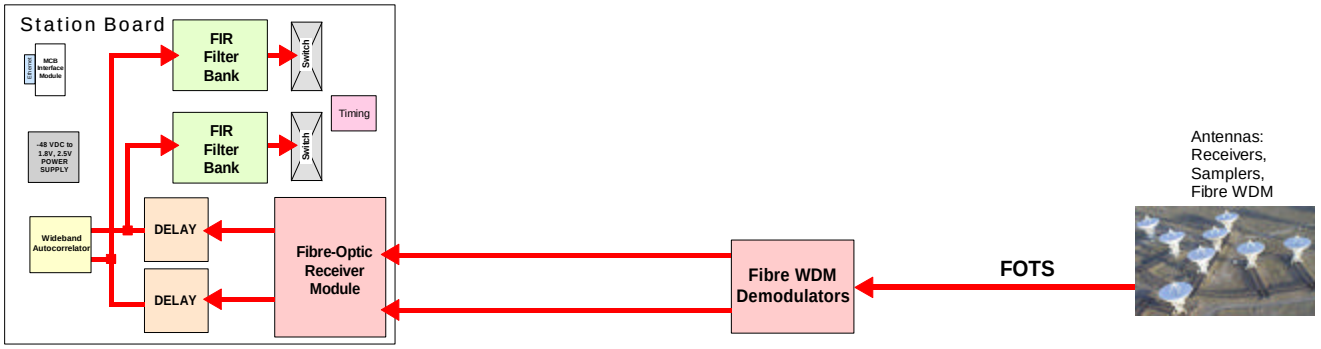
Outline

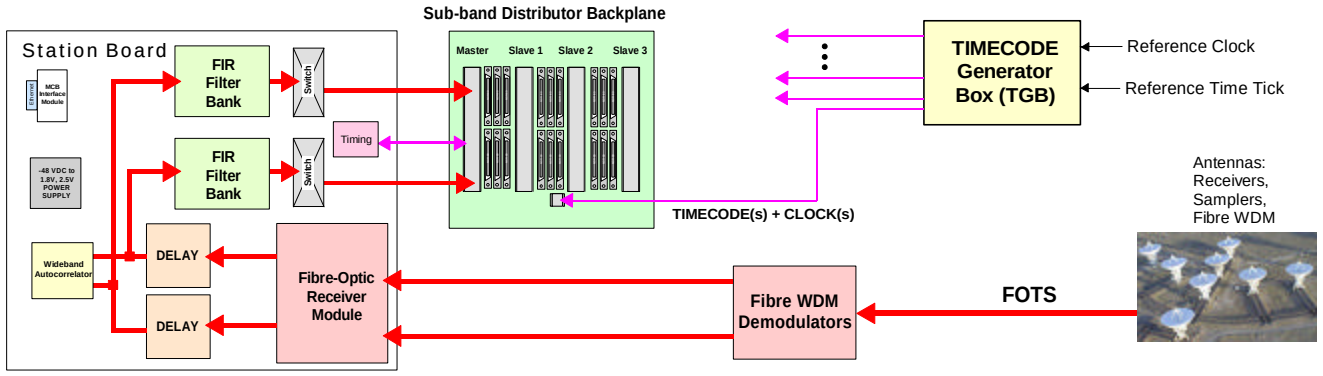
- Overview.
- Board descriptions.
- System design issues.

OVERVIEW

Antennas:
Receivers,
Samplers,
Fibre WDM

FOTS


Station Board
FIR Filter Bank
Switch
FIR Filter Bank
Switch
Timing
-48 VDC to 1.8V, 2.5V POWER SUPPLY
Wideband Autocorrelator
DELAY
DELAY
Fibre-Optic Receiver Module
Fibre WDM Demodulators
FOTS
Antennas: Receivers, Samplers, Fibre WDM


Sub-band Distributor Backplane
Station Board
FIR Filter Bank
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Switch
Switch
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Wideband Autocorrelator
DELAY
DELAY
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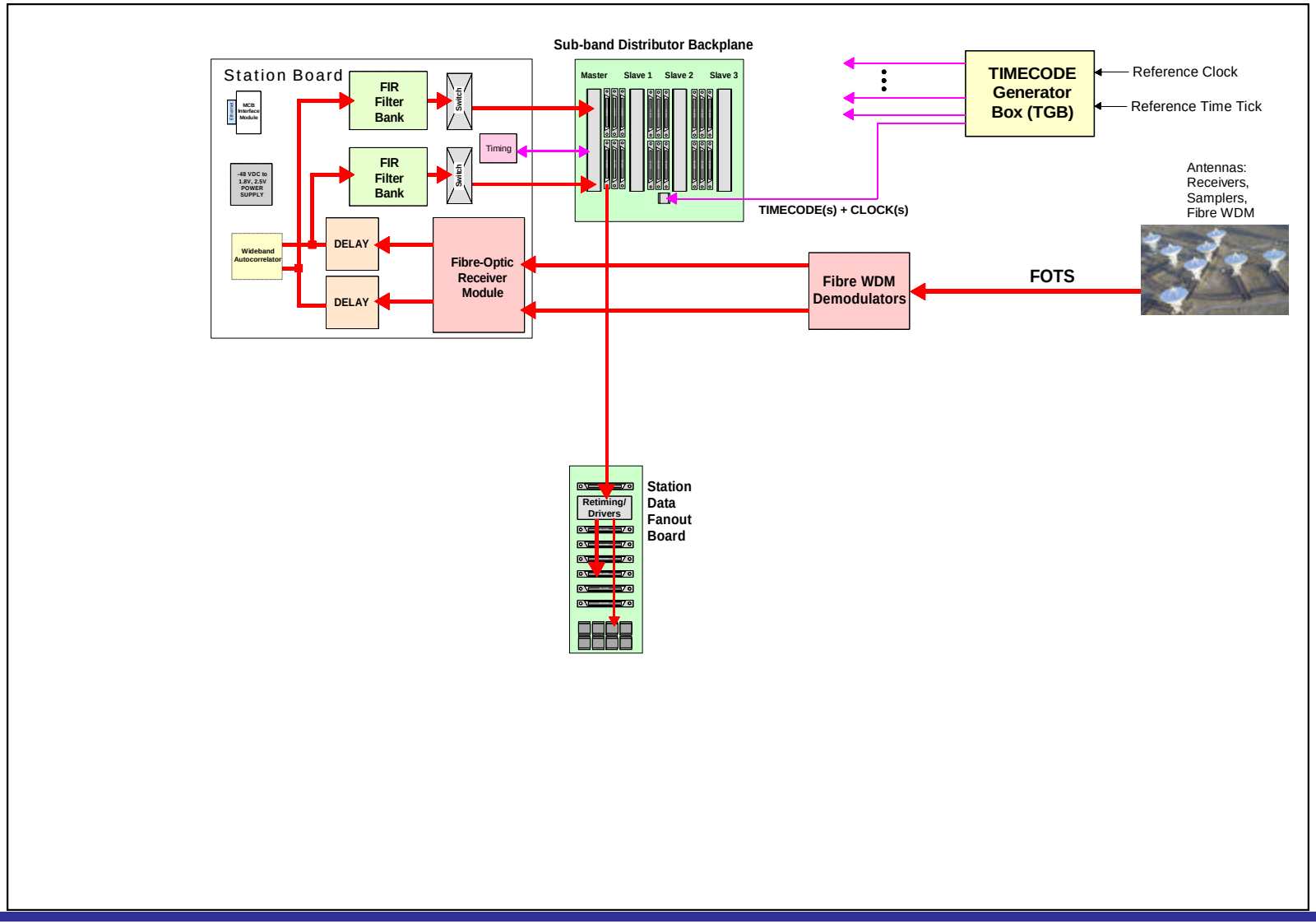
Master
Slave 1
Slave 2
Slave 3
TIMECODE(s) + CLOCK(s)
TIMECODE Generator Box (TGB)
Reference Clock
Reference Time Tick
Antennas: Receivers, Samplers, Fibre WDM
FOTS
Fibre WDM Demodulators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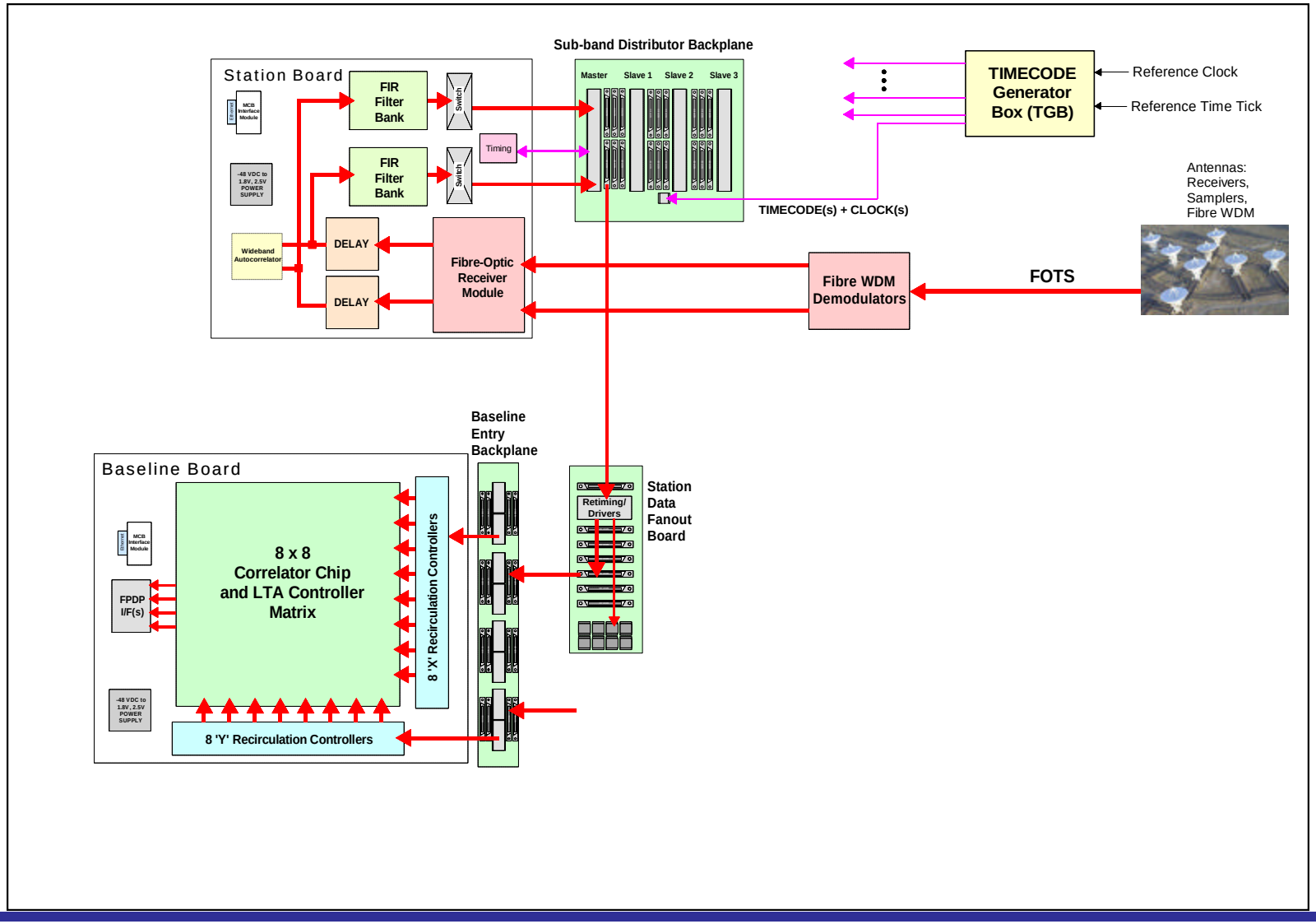
Fibre WDM Demodulators
Retiming/ Drivers
Station Data Fanout Board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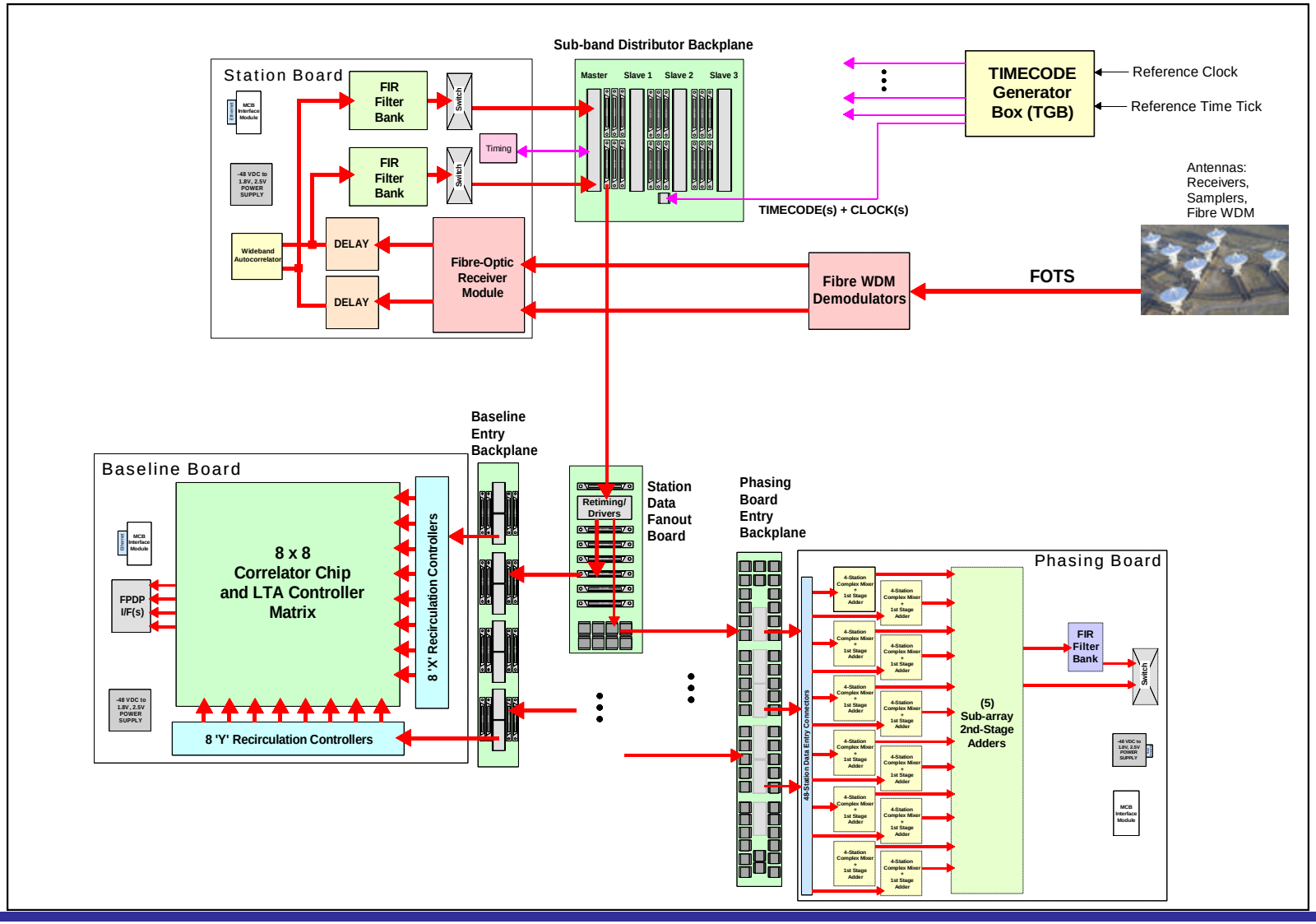
TIMECODE(s) + CLOCK(s)
Antennas: Receivers, Samplers, Fibre WDM
FOTS
Fibre WDM Demodulators
Baseline Entry Backplane
Baseline Board
8 x 8 Correlator Chip and LTA Controller Matrix
FPDP I/F(s)
8 'X' Recirculation Controllers
8 'Y' Recirculation Controllers
Retiming/ Drivers
Station Data Fanout Board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Station Board
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Switch
Switch
Timing
Master
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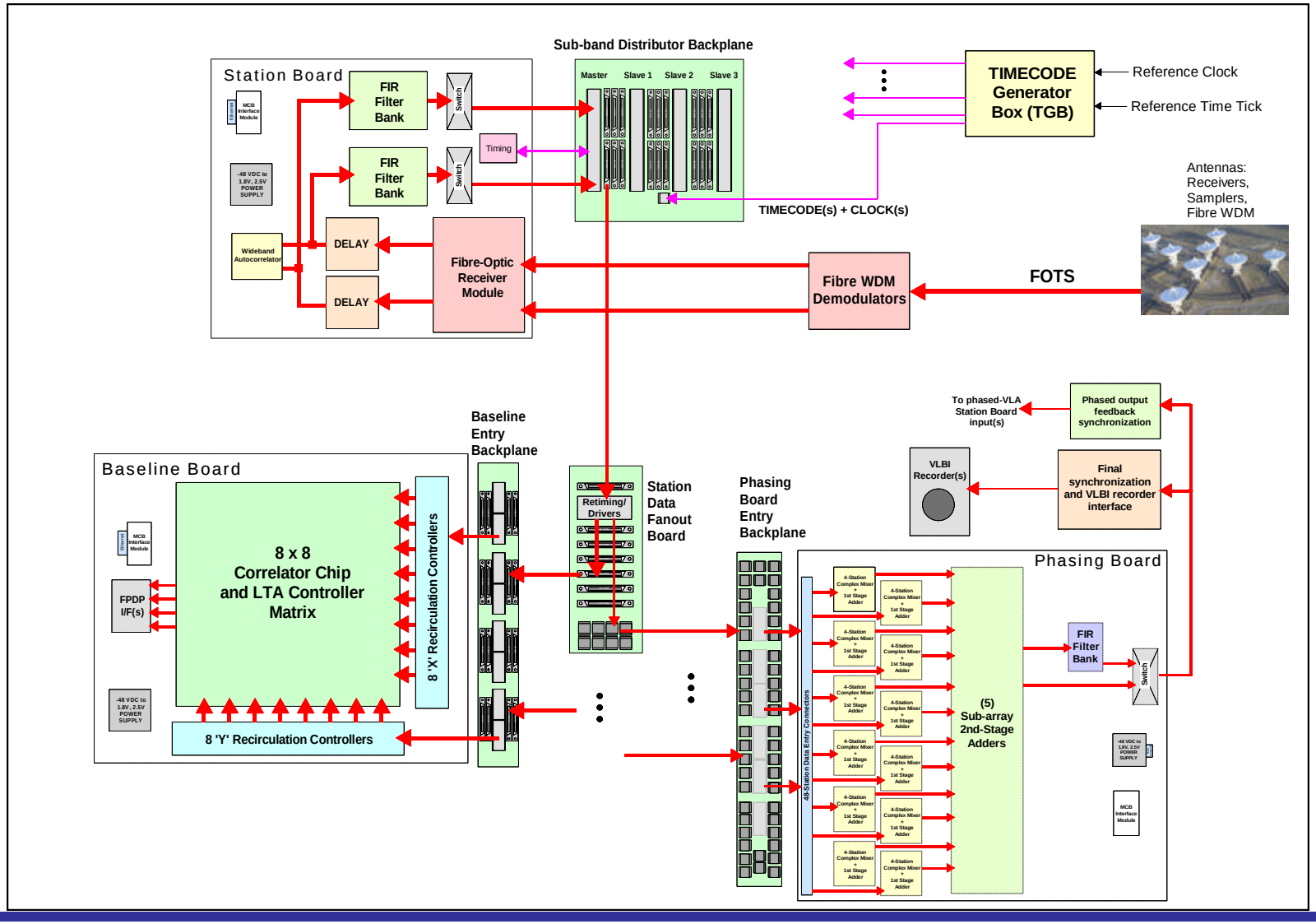
8 'Y' Recirculation Controllers
Retiming/ Drivers
Station Data Fanout Board
Phasing Board Entry Backplane
Phasing Board
(5) Sub-array 2nd-Stage Adders
FIR Filter Bank
Switch


Sub-band Distributor Backplane
Station Board
FIR Filter Bank
FIR Filter Bank
Switch
Switch
Timing
Master
Slave 1
Slave 2
Slave 3
TIMECODE Generator Box (TGB)
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TIMECODE(s) + CLOCK(s)
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Baseline Board
8 x 8 Correlator Chip and LTA Controller Matrix
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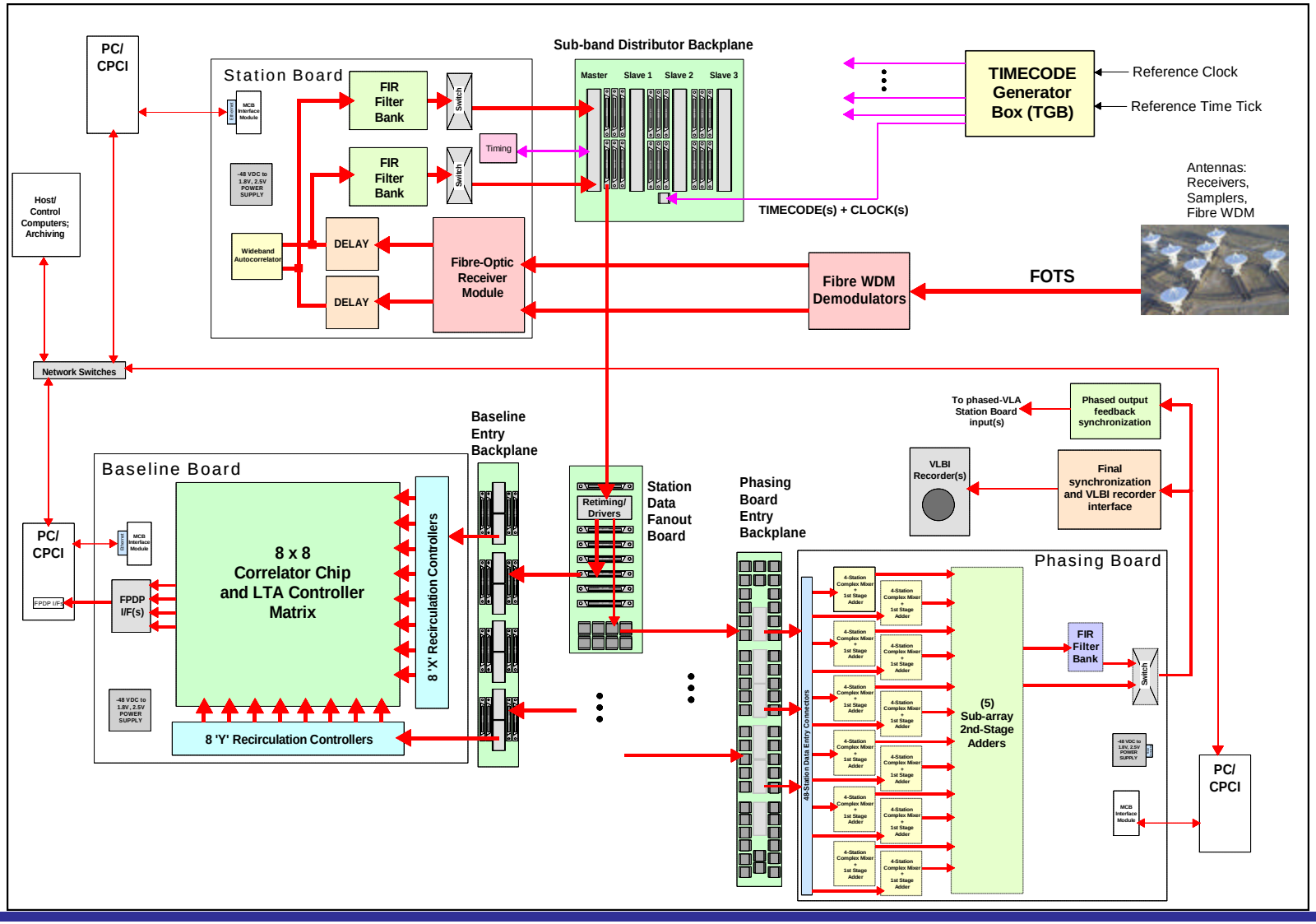
8 'X' Recirculation Controllers
8 'Y' Recirculation Controllers
Retiming/ Drivers
Station Data Fanout Board
Phasing Board Entry Backplane
To phased-VLA Station Board input(s)
Phased output feedback synchronization
VLBI Recorder(s)
Final synchronization and VLBI recorder interface
Phasing Board
4-Station Complex Mixer + 1st Stage Adder
(5) Sub-array 2nd-Stage Adders
FIR Filter Bank
Switch
MCB Interface Module


PC/ CPCI
Station Board
MCB Interface Module
FIR Filter Bank
FIR Filter Bank
Switch
Switch
Timing
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Reference Clock
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TIMECODE(s) + CLOCK(s)
Antennas: Receivers, Samplers, Fibre WDM
Fibre WDM Demodulators
FOTS
Host/ Control Computers; Archiving
Network Switches
Baseline Entry Backplane
Baseline Board
PC/ CPCI
MCB Interface Module
FPDP I/F(s)
8 x 8 Correlator Chip and LTA Controller Matrix
8 'X' Recirculation Controllers
8 'Y' Recirculation Controllers
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Retiming/ Drivers
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Phasing Board Entry Backplane
To phased-VLA Station Board input(s)
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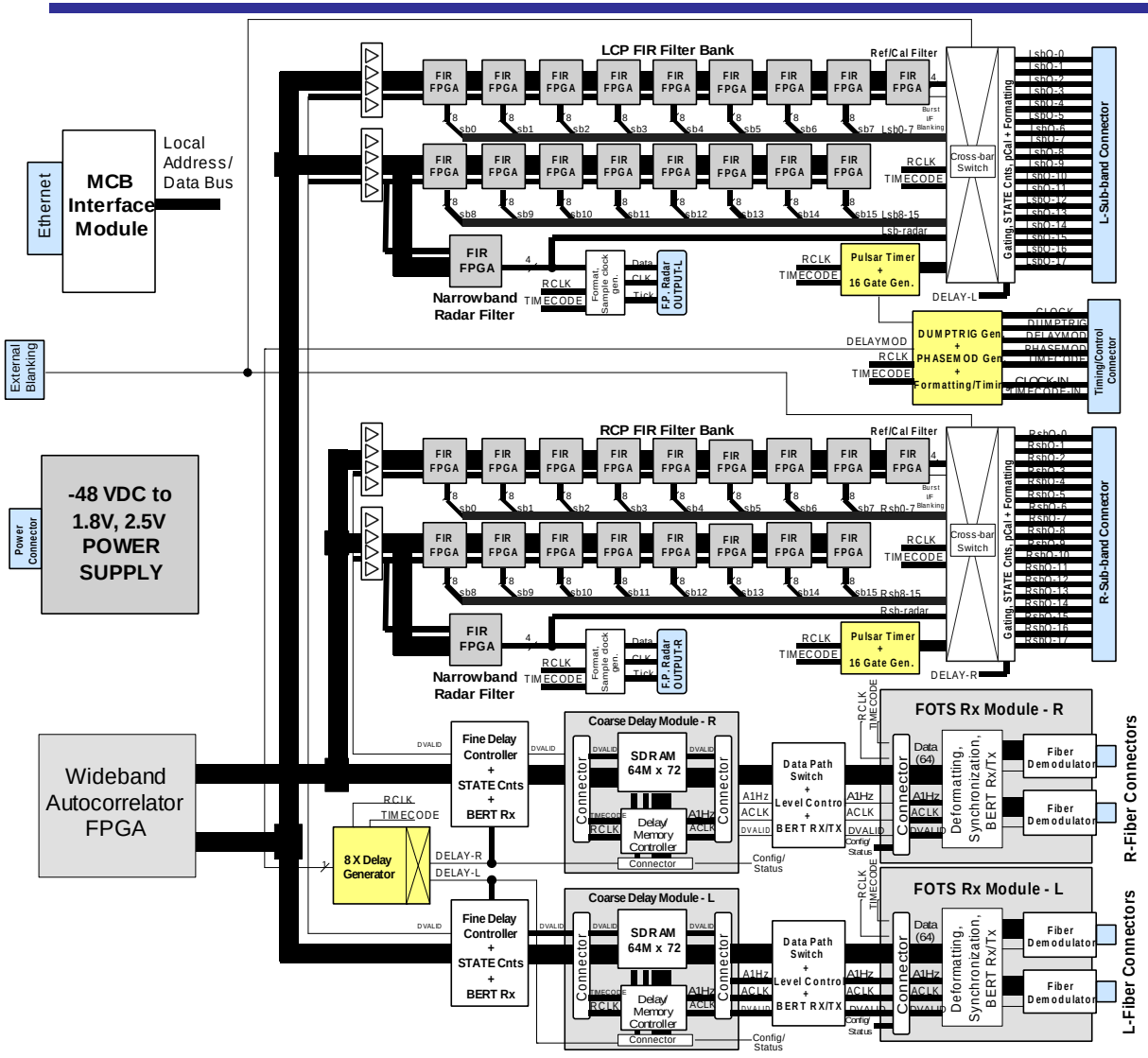
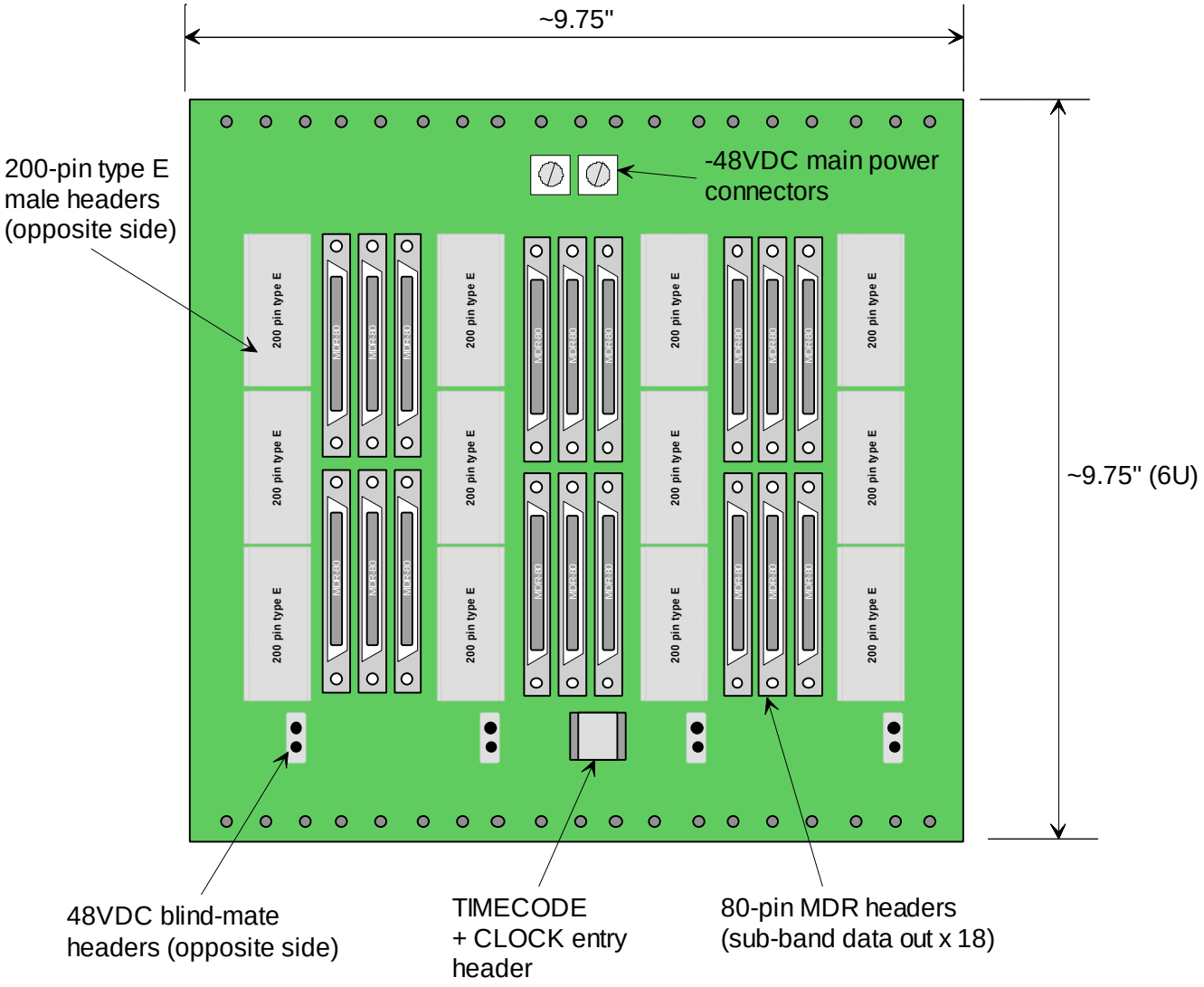
Final synchronization and VLBI recorder interface
Phasing Board
4-Station Complex Mixer + 1st Stage Adder
48-Station Data Entry Connectors
(5) Sub-array 2nd-Stage Adders
FIR Filter Bank
Switch
-48 VDC to 1.8V, 2.5V POWER SUPPLY
MCB Interface Module
PC/ CPCI

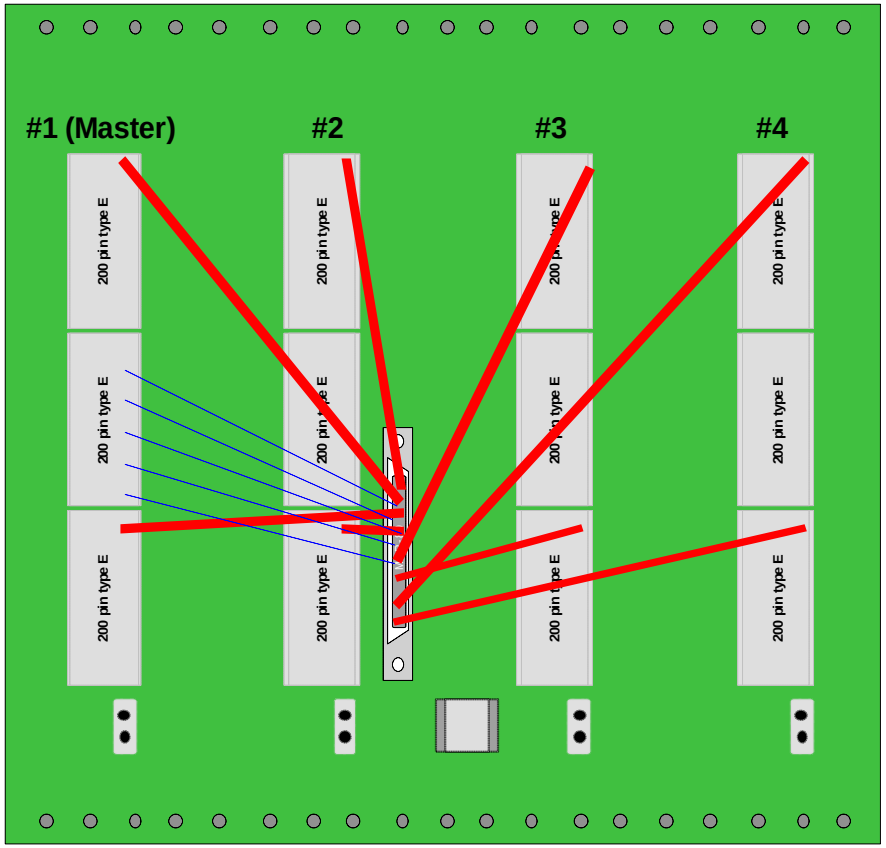
STATION BOARD



- Each Station Board handles one baseband pair (2 x 2 GHz = 4 GHz), 4 bits/sample.
- 8 bits/sample possible with 1/2 bandwidth.
- Two banks of 18 poly-phase FIR filters: each one independent in width and placement in the baseband.
- Input 64-bit, 256 Ms/s “data highway” *could* be reassigned to multiple basebands.
- Generates all timing, dump control, delay, and phase for downstream processing.
- Use SDRAM for >10k km baselines.
- Output switch for flexibility.

SUB-BAND DISTRIBUTOR BACKPLANE


~9.75"
200-pin type E
male headers
(opposite side)
-48VDC main power
connectors
~9.75" (6U)
48VDC blind-mate
headers (opposite side)
TIMECODE
+ CLOCK entry
header
80-pin MDR headers
(sub-band data out x 18)



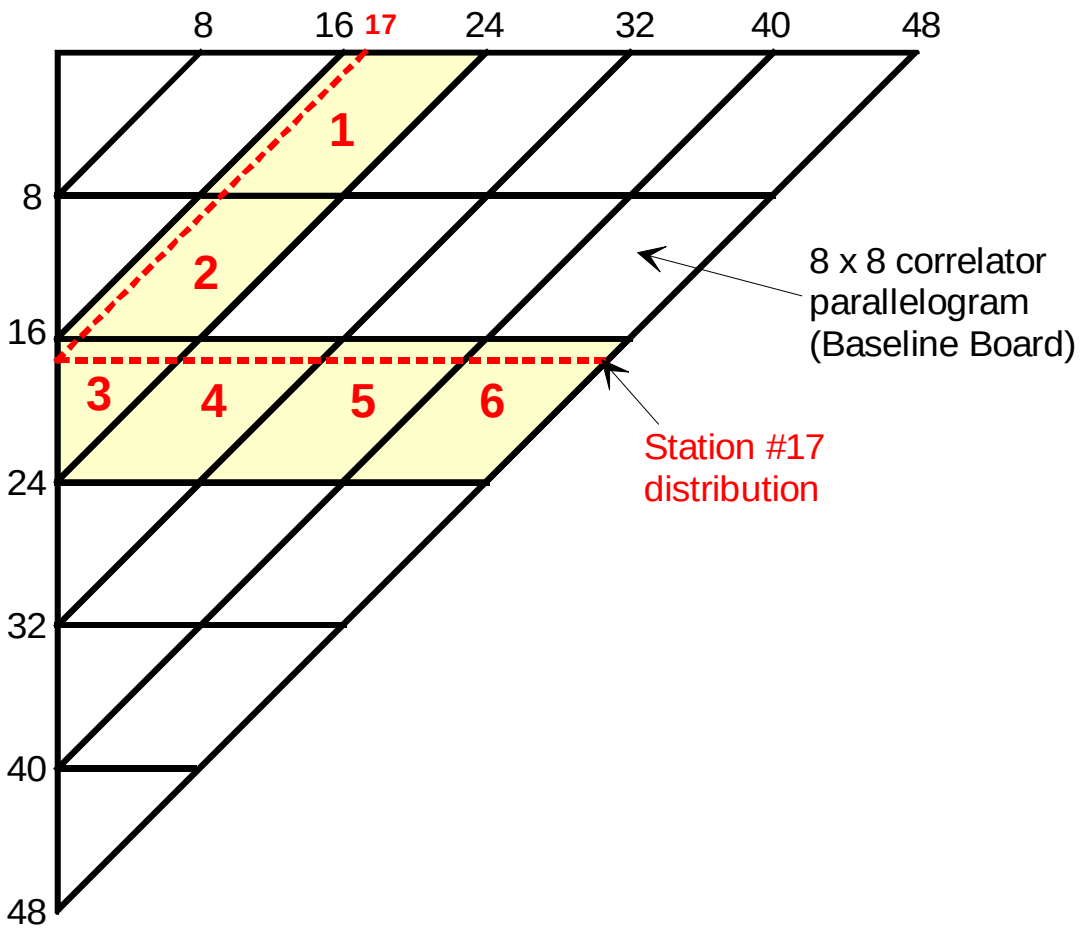
Each MDR-80 connector contains one sub-band from all 8 basebands (8 x 4-bits).

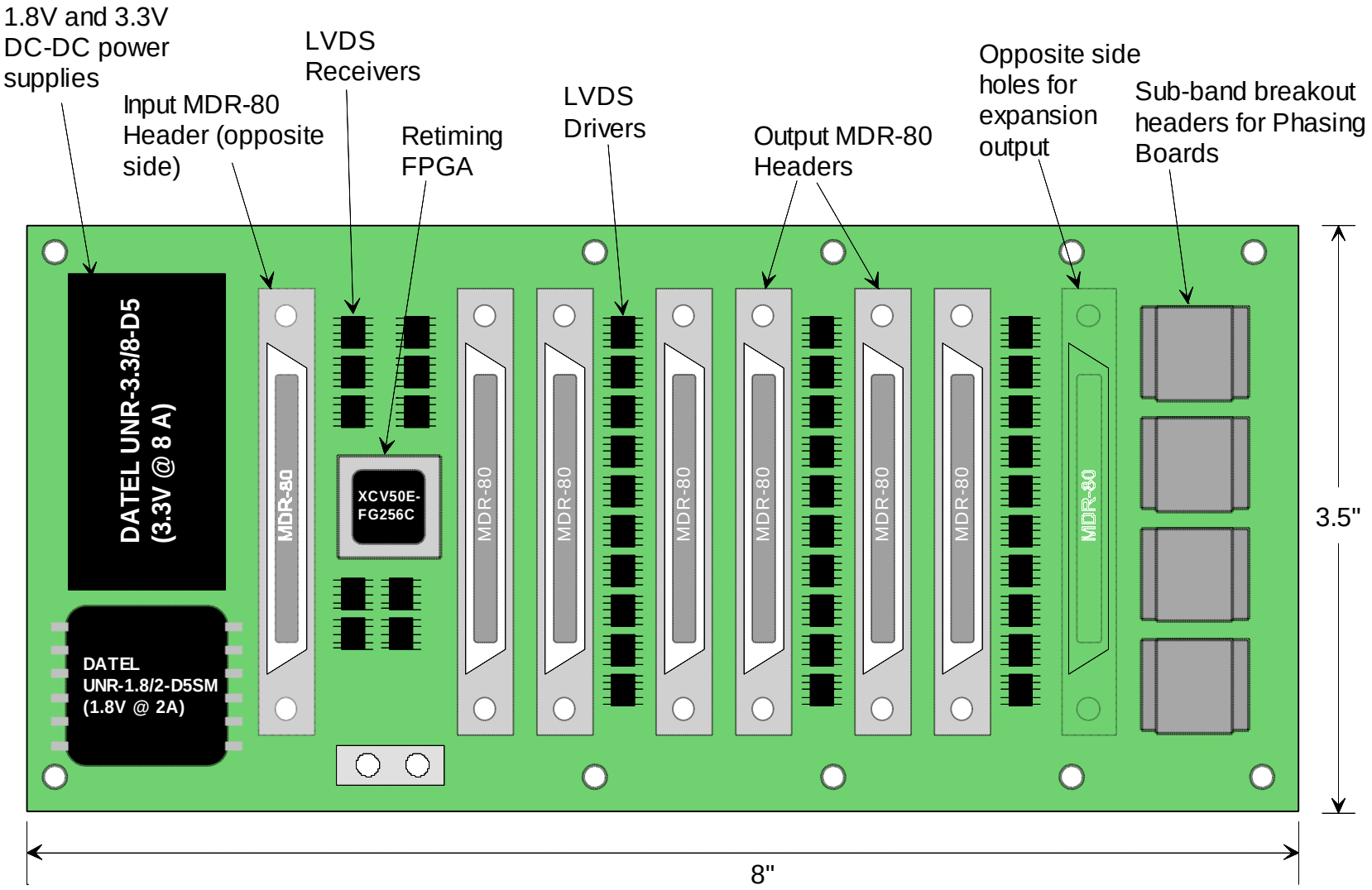
(+ TIMECODE + DUMPTRIG, + PHASEMOD, + DELAYMOD + CLOCK)

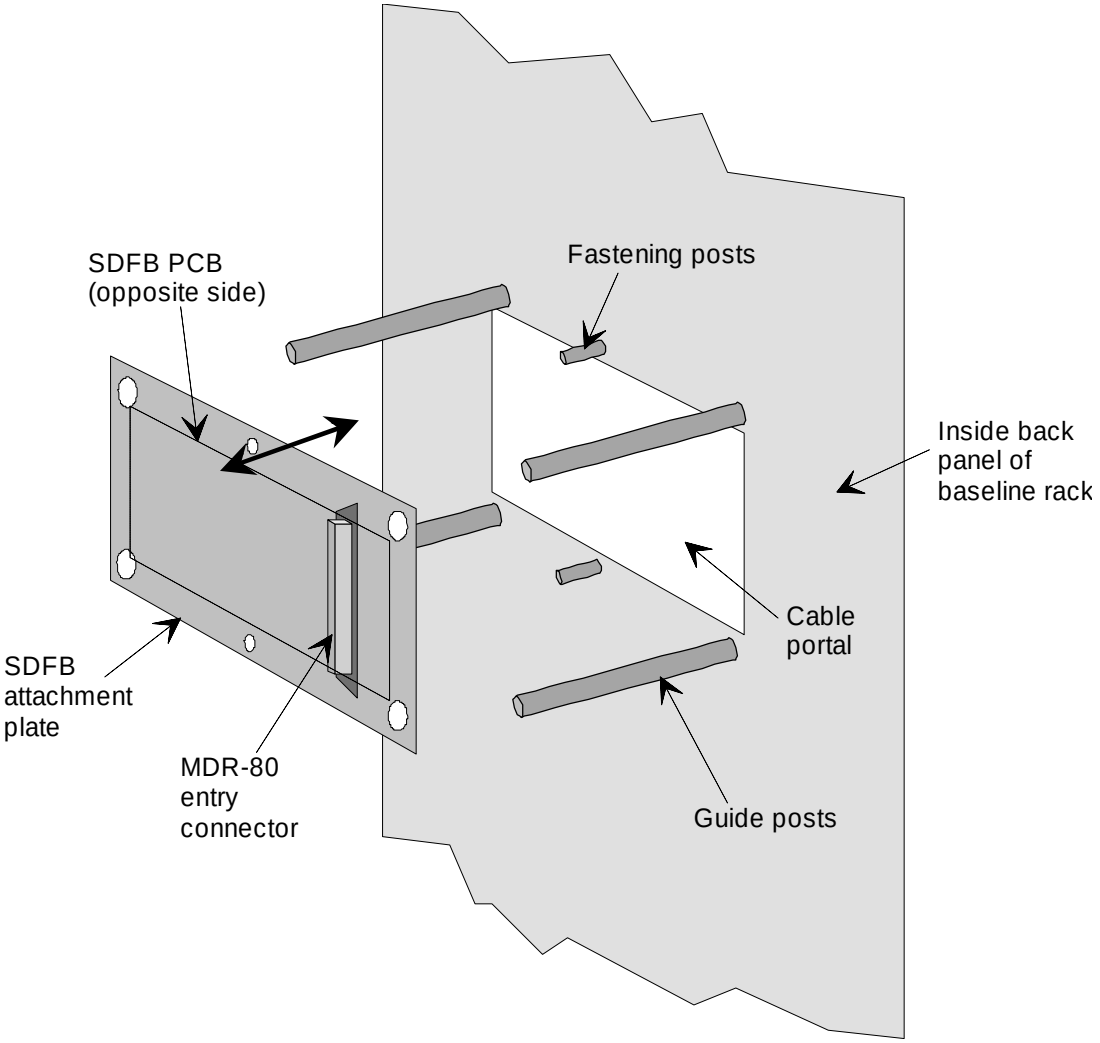
STATION DATA FANOUT BOARD

Station Data Fanout Board

- Fans data out to Baseline Boards within a Baseline Rack.
- For 32 stations, a fanout of 4 is required, 40 stations requires a fanout of 5, 48 stations a fanout of 6.
- Also fans data out to Phasing Boards, and expansion boards.

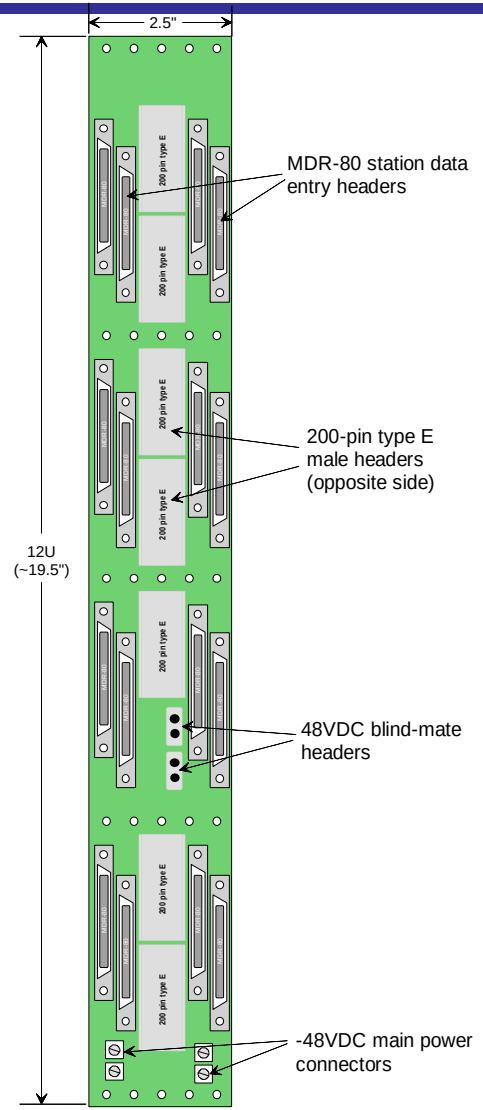



1.8V and 3.3V DC-DC power supplies
Input MDR-80 Header (opposite side)
LVDS Receivers
Retiming FPGA
LVDS Drivers
Output MDR-80 Headers
Opposite side holes for expansion output
Sub-band breakout headers for Phasing Boards
DATEL UNR-3.3/8-D5 (3.3V @ 8 A)
DATEL UNR-1.8/2-D5SM (1.8V @ 2A)
XCV50E-FG256C
MDR-80
3.5"
8"



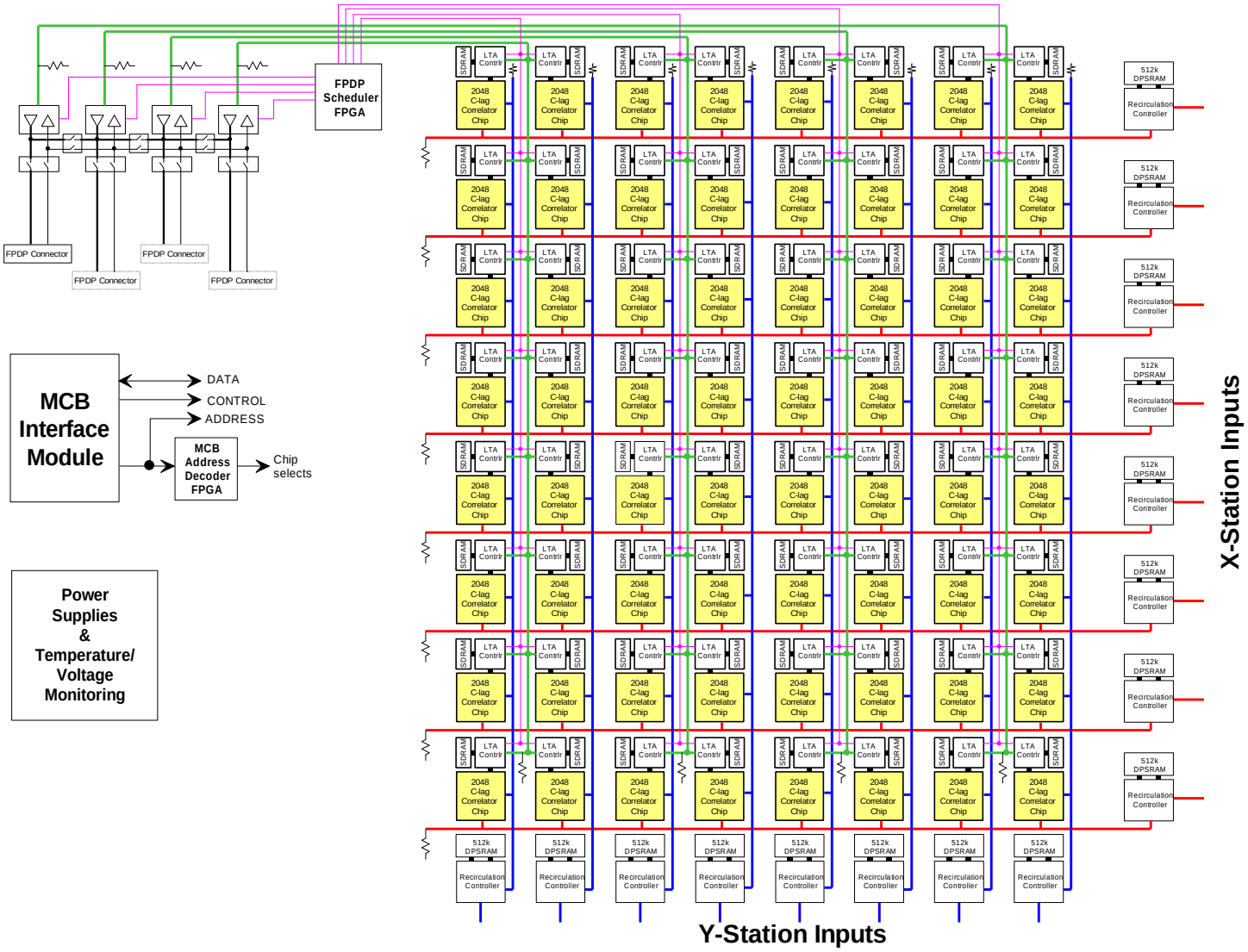
- Straw-man concept for hot-swapping the SDFB.
- Mount SDFB to plate, that can be unfastened from the back panel of the Baseline Rack.
- Guide posts allow extraction of SDFB plate without short circuit worry.
- Remove cables, install new plate assembly...
- Alternative is to use a set of blind-mate MDR-80 sockets on PCB that mounts permanently to back panel. Higher cost...

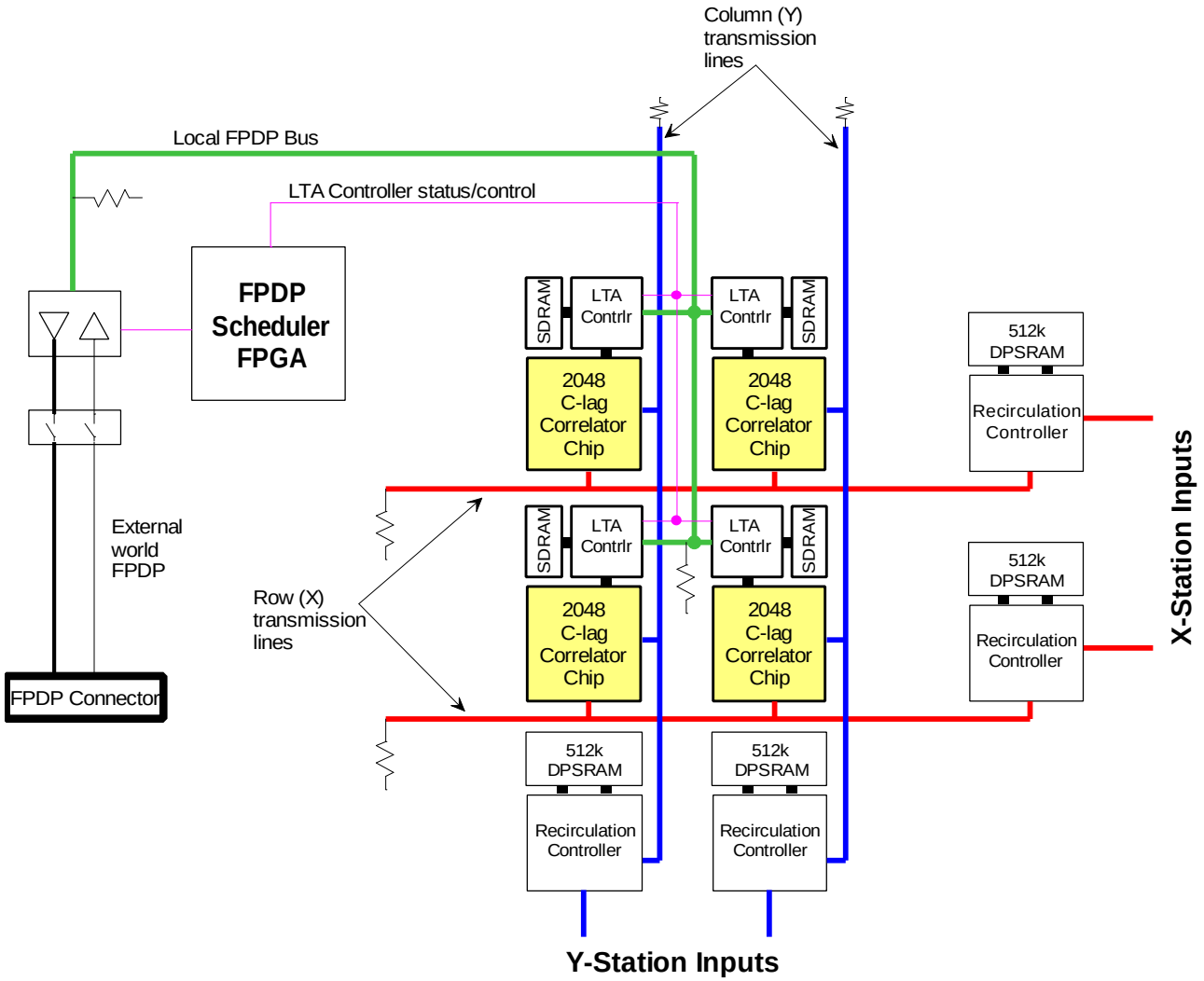
BASELINE ENTRY BACKPLANE



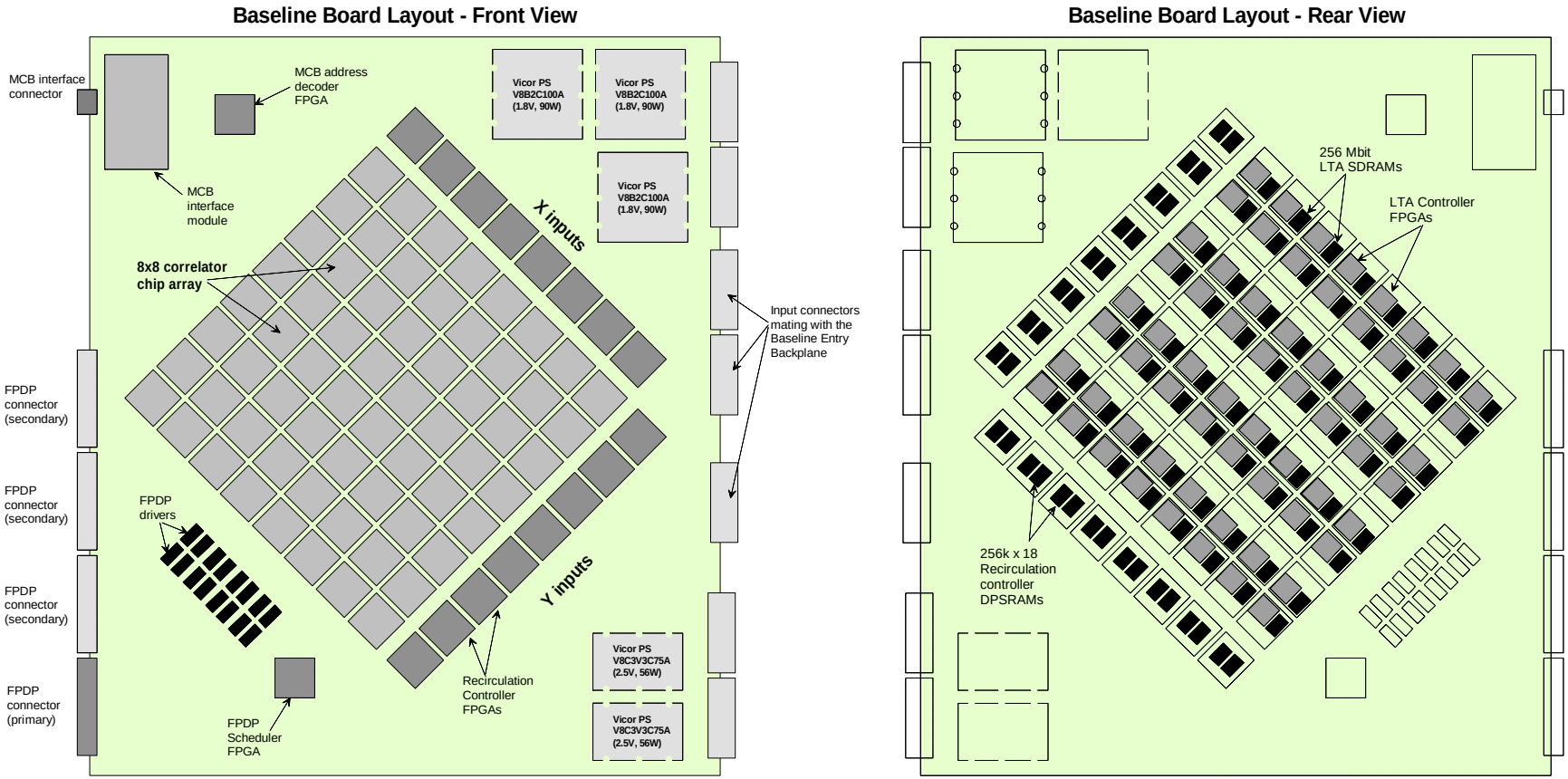
- Feeds sub-band (MDR-80) data through to the Baseline Board.
- Blind-mate with Baseline Board.
- Single board design permits flexibility in mixing Baseline Boards and Phasing Boards in the same sub-rack.
- Many pins using 200-pin (hm 2.0, 8 row) connectors, yields high insertion force (~100 lbs).
- hm 2.0 connectors should be ok for 256 Mbits/sec.

BASELINE BOARD

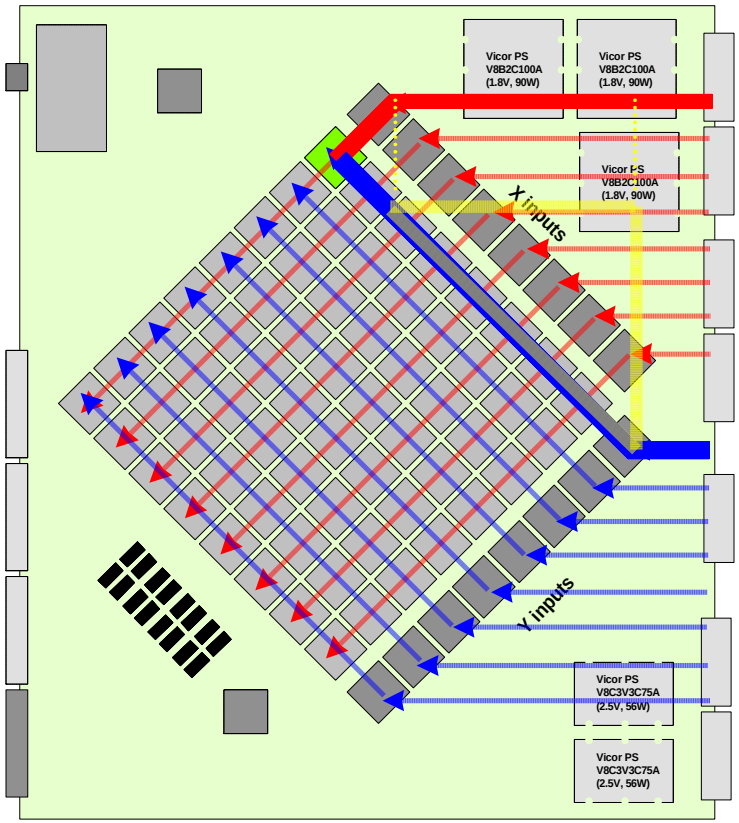

FPDP Scheduler FPGA
FPDP Connector
FPDP Connector
FPDP Connector
FPDP Connector
MCB Interface Module
DATA
CONTROL
ADDRESS
MCB Address Decoder FPGA
Chip selects
Power Supplies & Temperature/ Voltage Monitoring
SDRAM
LTA Contrlr
2048 C-lag Correlator Chip
512k DPSRAM
Recirculation Controller
X-Station Inputs
Y-Station Inputs



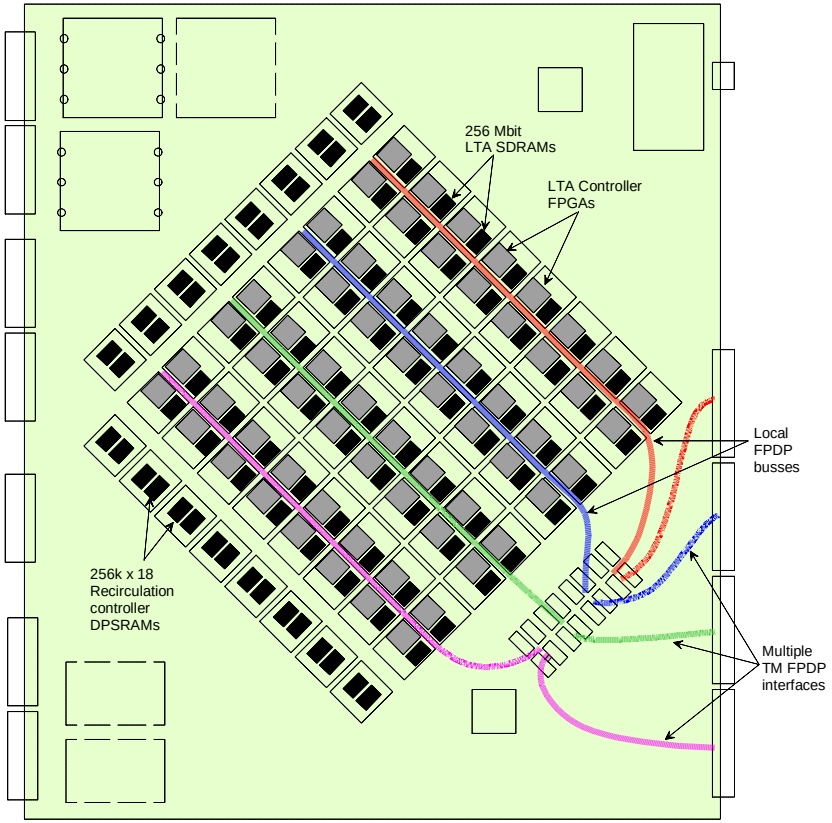
- FPDP is a simple protocol to handle with an FPGA, with no CPU interaction.
- Alternate solutions (Firewire) possible…as long as controlled by FPGA.


Baseline Board Layout - Front View
MCB interface connector
MCB address decoder FPGA
Vicor PS V8B2C100A (1.8V, 90W)
Vicor PS V8B2C100A (1.8V, 90W)
Vicor PS V8B2C100A (1.8V, 90W)
MCB interface module
X inputs
8x8 correlator chip array
Input connectors mating with the Baseline Entry Backplane
FPDP connector (secondary)
FPDP connector (secondary)
FPDP drivers
FPDP connector (secondary)
Y inputs
FPDP connector (primary)
Vicor PS V8C3V3C75A (2.5V, 56W)
Vicor PS V8C3V3C75A (2.5V, 56W)
Recirculation Controller FPGAs
FPDP Scheduler FPGA
Baseline Board Layout - Rear View
256 Mbit LTA SDRAMs
LTA Controller FPGAs
256k x 18 Recirculation controller DPSRAMs

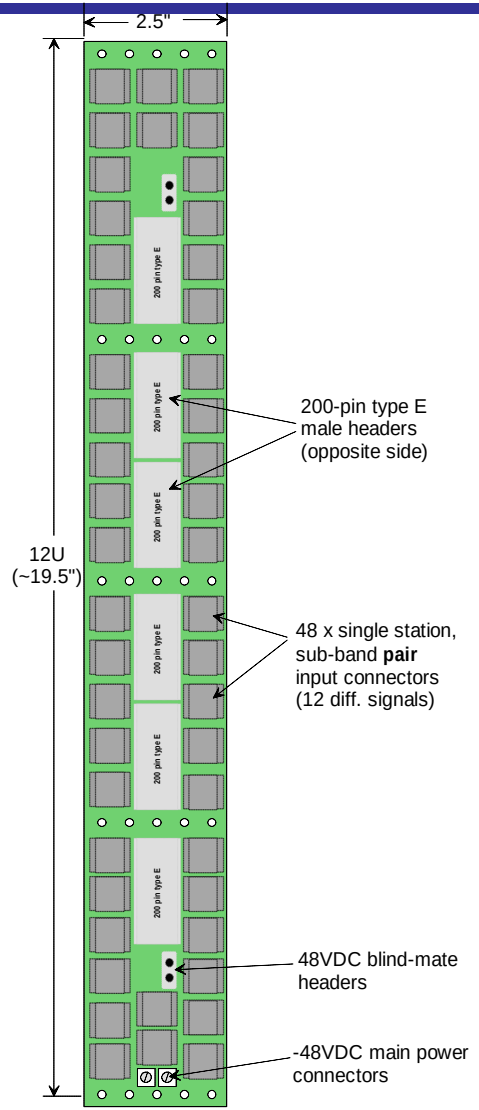
Baseline Board Layout - Front View - High Speed Data Routing



Baseline Board Layout - Rear View - FPDP Bus Routing - Multiple Output

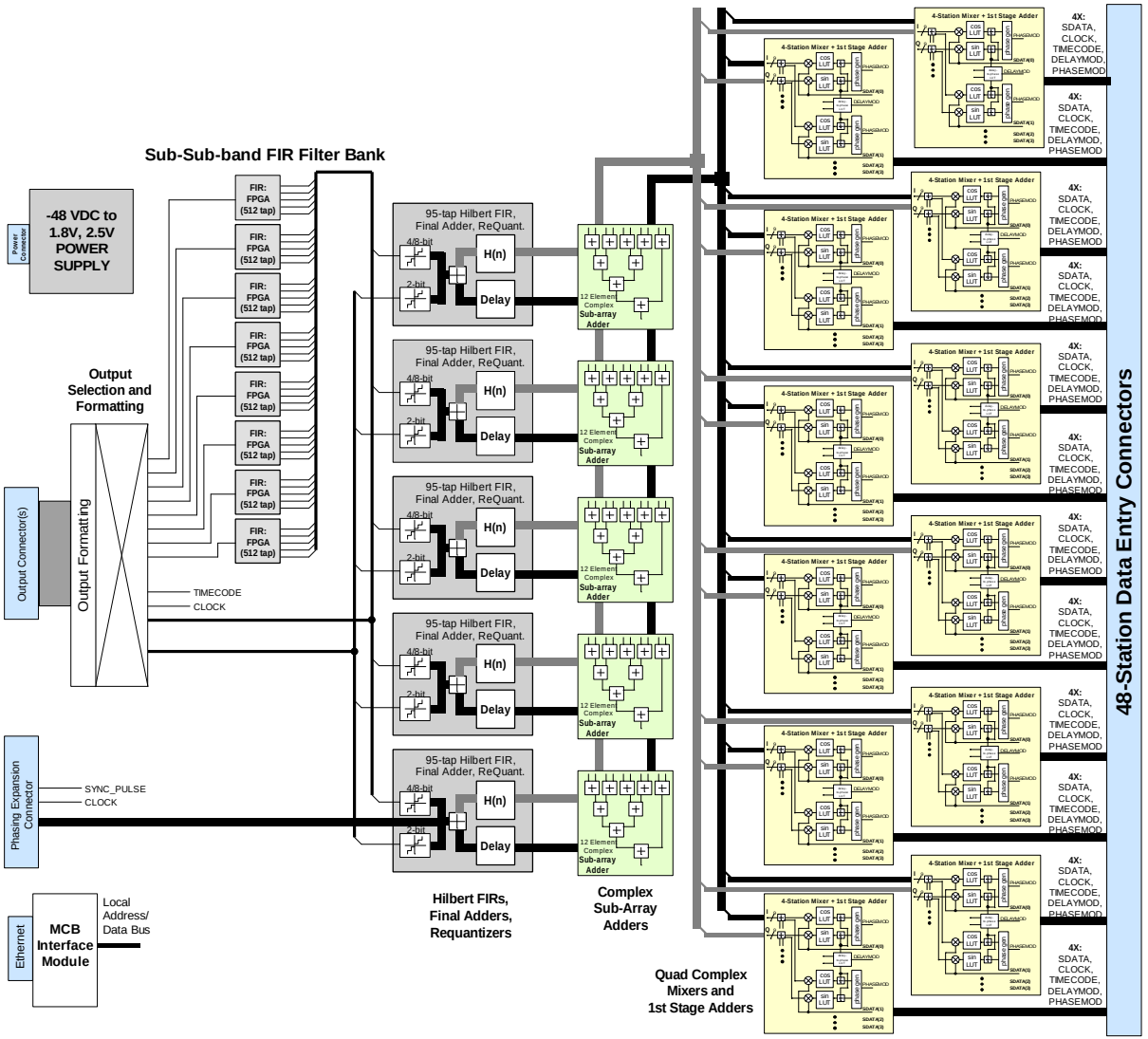


PHASING BOARD ENTRY BACKPLANE



- Feeds up to 48 stations, 1 sub-band *pair* into a Phasing Board.
- Each connector contains two, 4-bit data paths, timing, delay, and phase.
- Use GORE “quietzone” cables / connectors (12 pairs).

PHASING BOARD



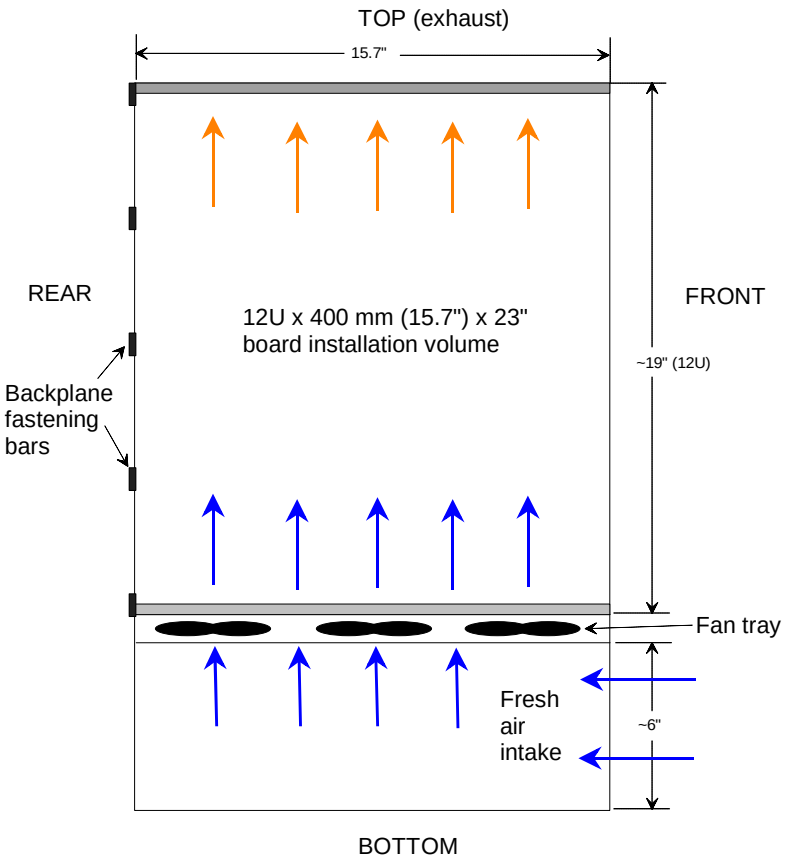
- Phases 1 sub-band pair, from up to 48 stations.
- "Phasing granularity" of 4 stations to prevent excessive connection problems.
- 5 sub-arrays.
- Sub-sub-band filtering for more efficient narrowband data recording.
- All digital.
- 8-bit output for expansion >48 stations

TIMECODE GENERATOR BOX

- Generates “TIMECODE” for use by correlator.
- 4 TIMECODES generated. Each Station Board “quad” can select any of the 4. This permits mixed real-time and tape-based VLBI operation.
- 48 outputs to go to up to 48 Sub-band Distributor Backplanes.
- Requires input clock and reference time tick.

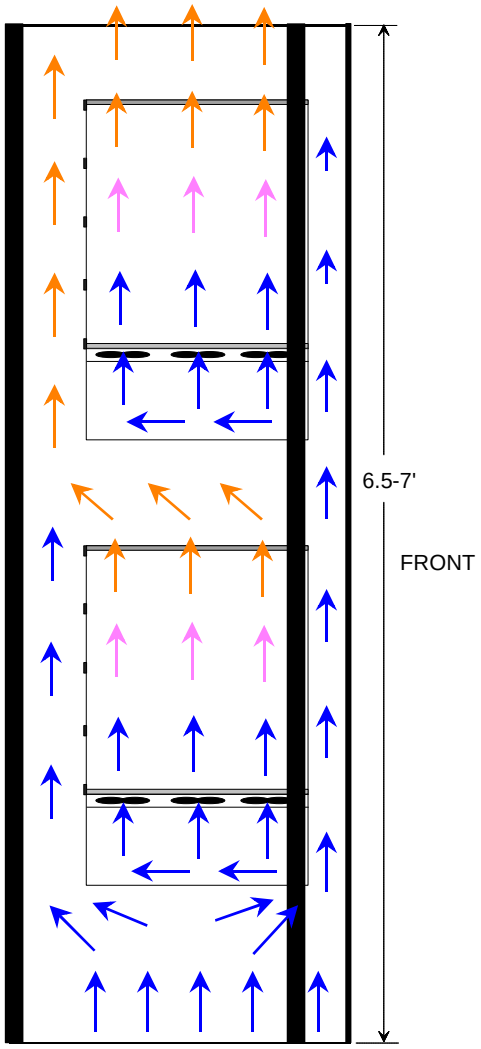
SYSTEM DESIGN ISSUES

Sub-rack Design



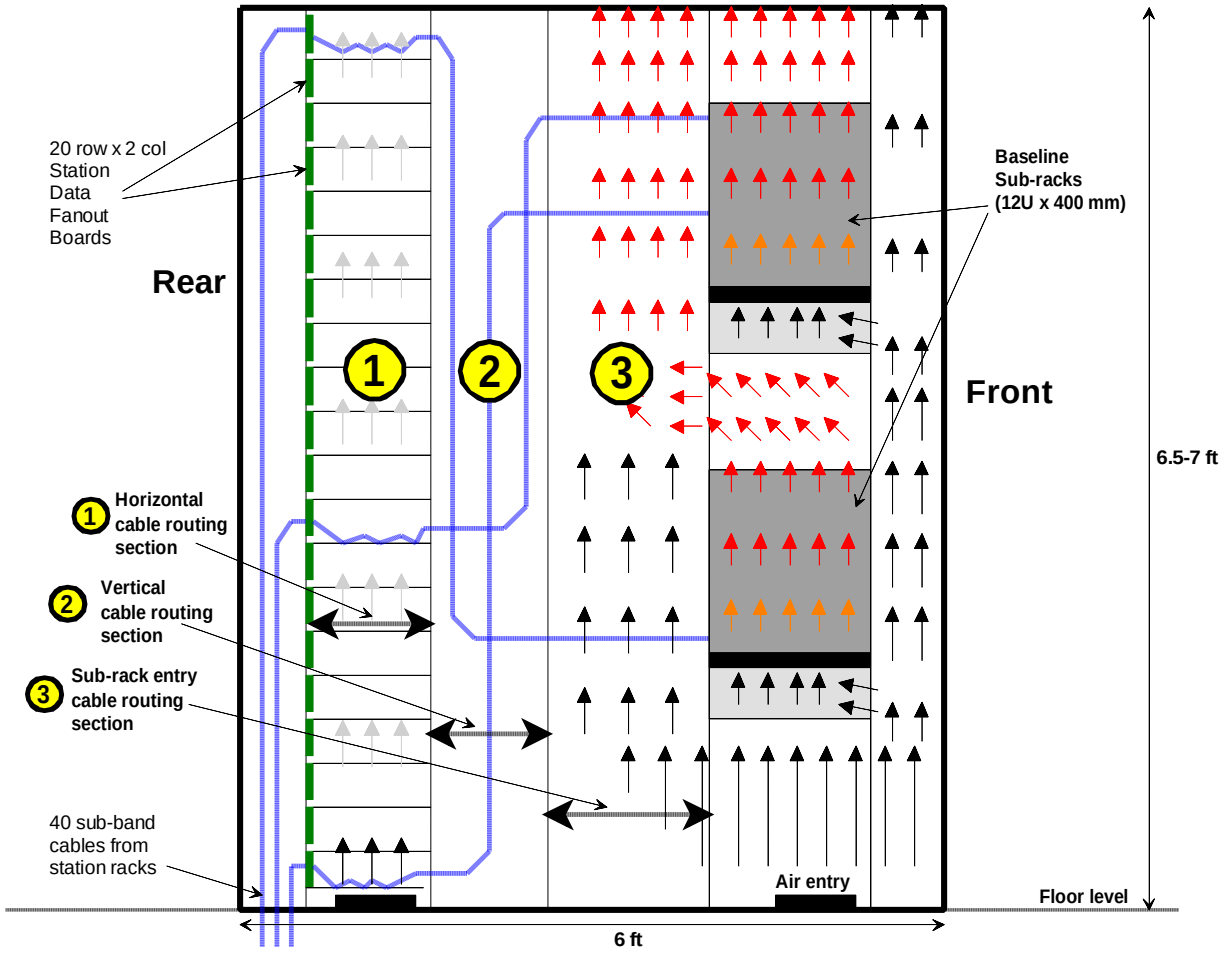
- 24” wide to allow 8 boards, with 2.5” width per board (3 full VME slots per board).
- Fresh (cool) air supply for each sub-rack (crate) of boards.
- Requires hot-swappable fan (tray).
- Requires more vertical rack space...

Station Rack Design



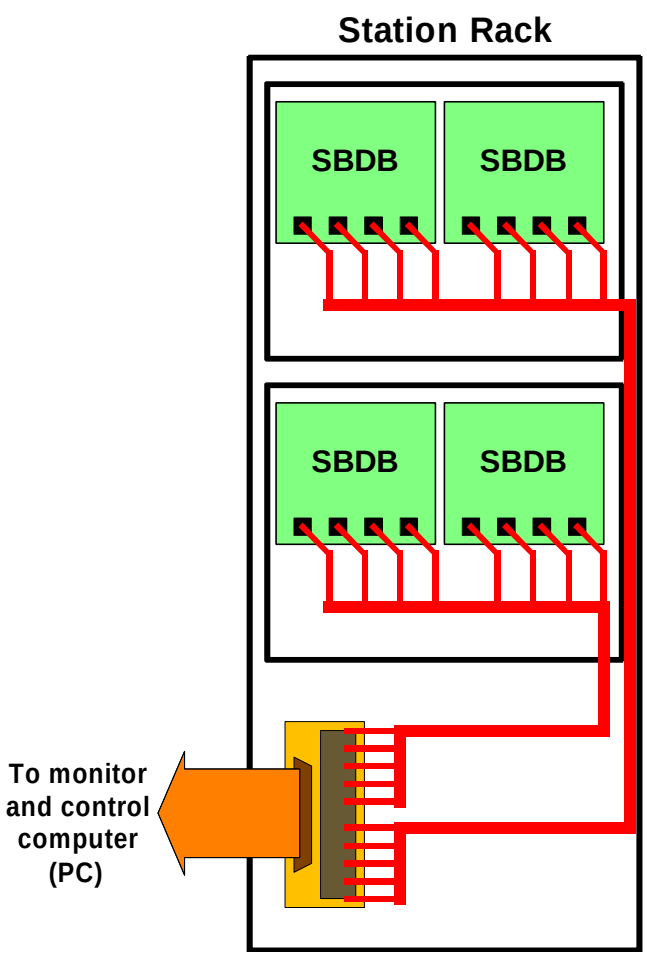
- Cool air entry from bottom.
- Each sub-rack has own cool air.
- Probably only fit two sub-racks per rack (7').
- Estimated power dissipation: 200W/board ~= 2kW/sub-rack ~= 4kW/rack.

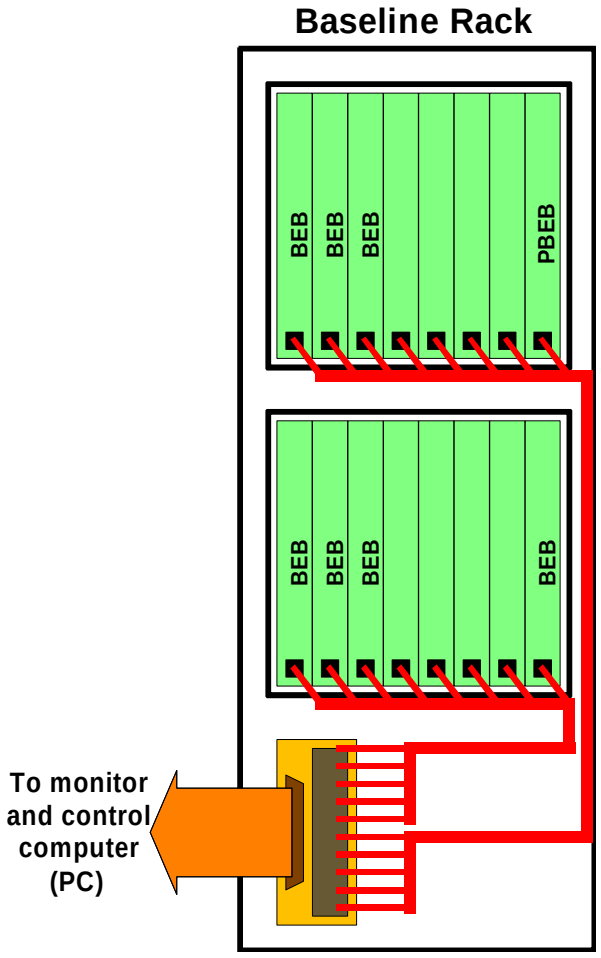
Baseline Rack Design



- Must hold up to 256, ~3 m 80-wire GORE cables.
- Extra 3’ depth, with rear and side-panel access.
- “Grid routing” to organize cabling.
- Will build full mock-up to test feasibility.

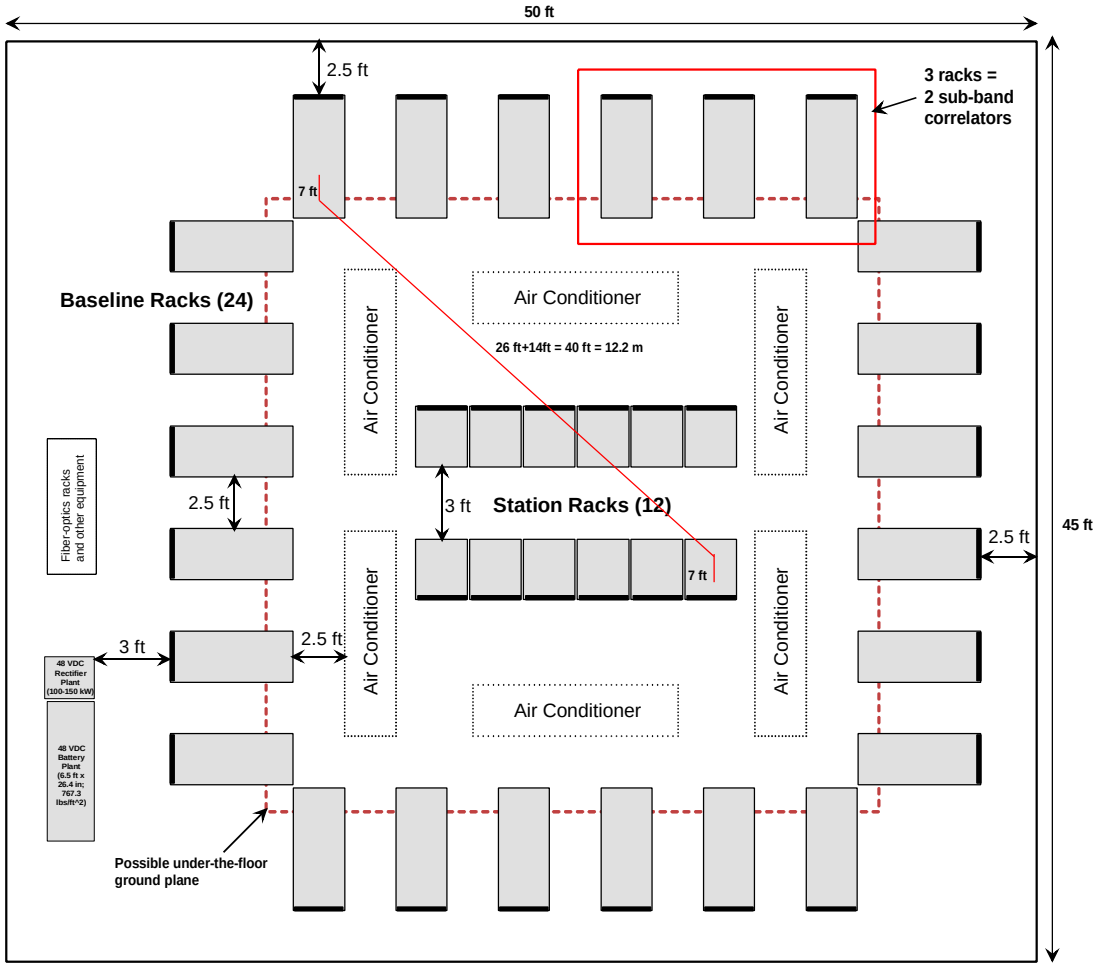
Remote Power M&C



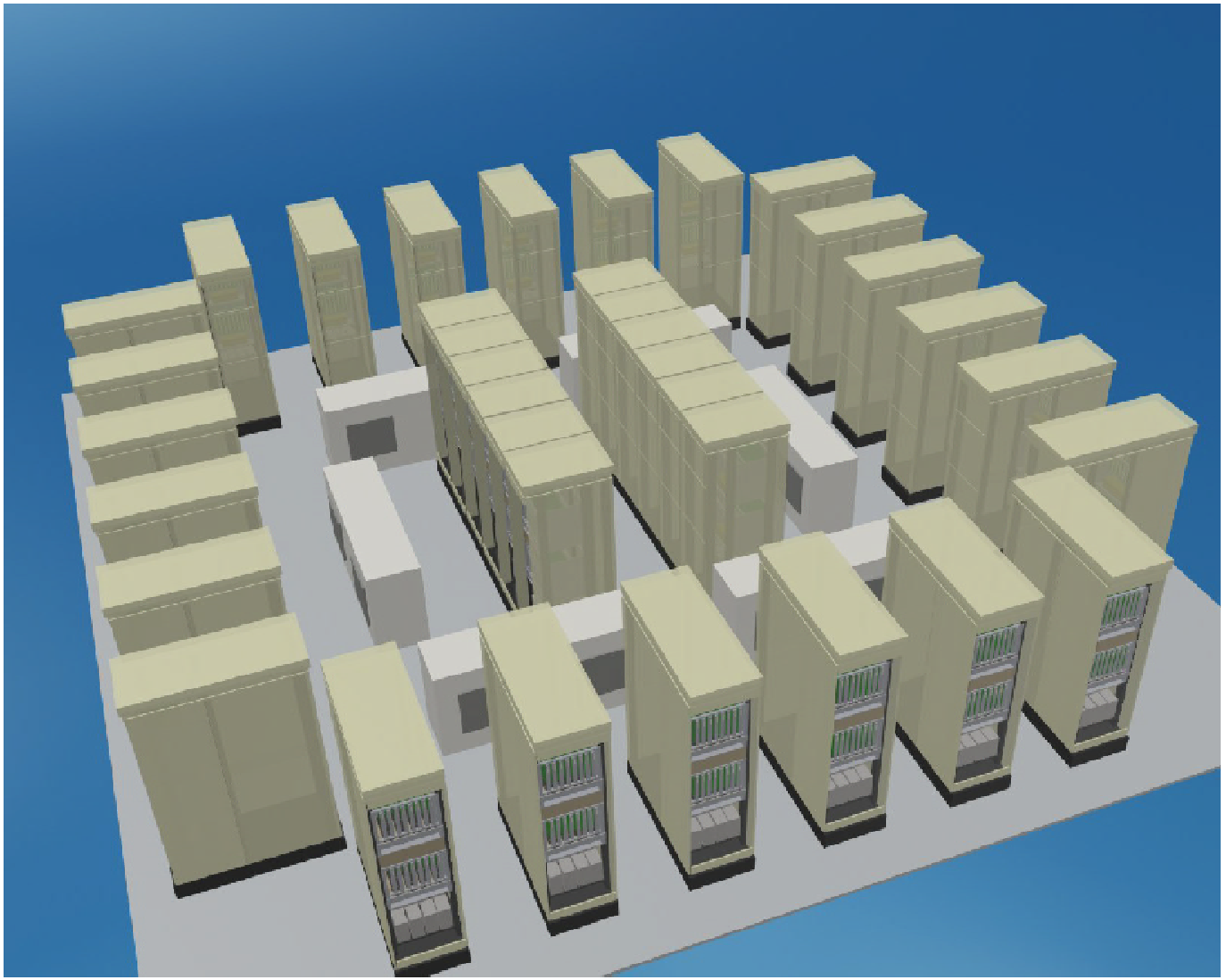


- DC-DC converters have power monitor and control line.
- Route via terminal block and DB25-pin connector to external control computer.
- Individual power-cycle and monitor capability for each board in the system.

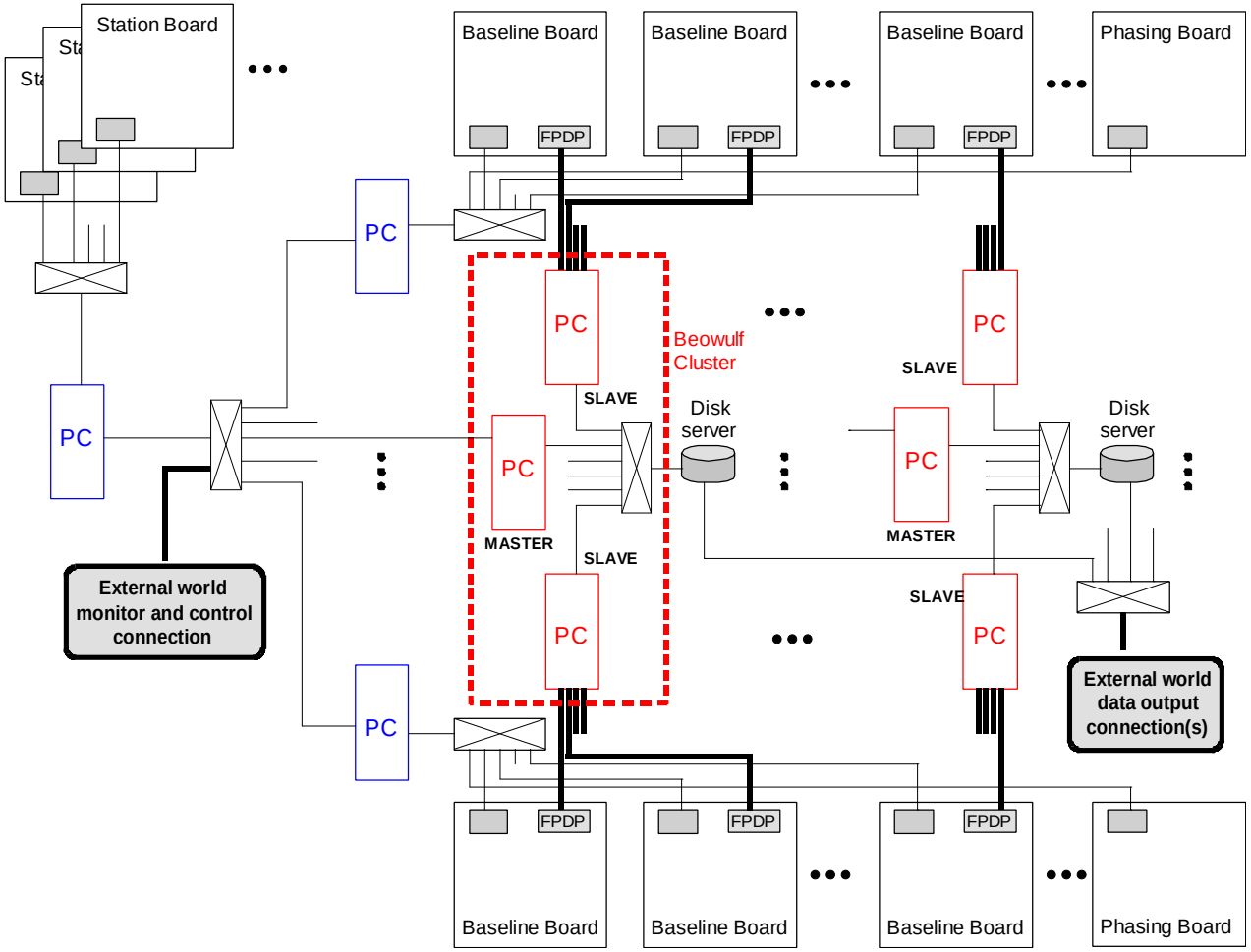
Correlator (48-station) Floor Plan



- 45 x 50 ft.
- Center Station Racks because of cabling.
- 360^{o} access to baseline racks (intra-rack cabling).
- 48 VDC mains supply Single-point failure, hot-swappable boards and modules.
- 48 VDC plant. Telephony central-office grade. N+*n* redundant, hot-swappable modules.



(One idea of the) Computing Environment



- Use NRAO "MIB". VxWorks? Home-brew OS? 100 Mbps Ethernet.
- Use Linux PCs for non-real-time "sophisticated" M&C computing (e.g. model generation)
- Use Linux PC Beowulf clusters for back-end data processing.
- Other solutions being proposed...

Summary

- 32 delivered stations expandable to 48+ stations.
- A few modules need to be developed.
- Baseline Board and correlator chip conceptual design is quite advanced.
- Station Board design straightforward, but not as advanced as the Baseline Board.
- System design (racks etc.) fairly conservative. High cabling density in Baseline Rack requires mock testing.
- Full remote control capability, can hot-swap all modules with semiconductors.
- Ideas for computing environment, but not decided...