EVLA Project Book, Chapter 7

FIBER OPTICS SYTEM

Version 5

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Revision History

2001-Aug 22: Initial release
2001-Nov 14: Revision one
2002-May 20: Revision Two: Changes after the fiber was procured.
2002-Aug 28: Revision –3. More information on fiber and round trip.
2004-Oct 31: Revision –4. Update information on fiber, Laser Safety, LO, and DTS.
2006-Mar 31: Revision –5. Update chapter, moved LO sections to chapter 6, included samplers.

Summary

7.1 Introduction

The EVLA makes extensive use of fiber optic technologies for the IF Data Transmission, the Local Oscillator and Reference distribution, and all Monitor/Control functions. This allows for the use of commercially developed technologies and components, leveraging on the tremendous investment made in these technologies by the computer and telecommunications industries. Each of these systems will be discussed separately.

7.2 The Fiber System

A set of twelve fibers runs to each pad location throughout the EVLA. The cables are run in a star configuration with all fibers originating at the termination room and ending at each antenna pad. The fibers from the Main Distribution Frame (MDF) in the termination room are grouped together into trunks and are terminated for each pad. The MDF is a commercial product that will be filled to 50% capacity at the end of the project.

The EVLA uses standard single-mode fiber. The fiber has a typical attenuation of 0.3 dB/km at 1310nm and 0.2dB/km at 1550nm. It has a Maximum chromatic dispersion of 17.4 ps/nm km at 1550nm. The Mode Field Diameter is 9.5 to 11.5 μm at 1550 nm. The fiber meets or exceeds ITU-T recommendation G.652, TIA-EIA-492CAAA, IEC Publication 60793-2, "Detail Specification for Class IVa Dispersion-Unshifted Single-Mode Optical Fibers," and ITU recommendation G.652, “Characteristics of Single-Mode Optical Fiber Cable.” and Bellcore GR-20-COR requirements.

The fibers are placed inside loose buffer tubes. The buffer tubes are in a double armored direct burial cable. The double armored cables have three sheaths of MDPE. The minimum nominal jacket thickness of the inner sheaths is 1.0 mm. The inner jacket is applied directly over the tensile strength members and water swellable tape. The armor is

a corrugated steel tape polymer coated on both sides for corrosion resistance, and is applied around the outside of the water blocking tape. The outer jacket is applied over the second layer of corrugated steel tape armor. The outer jacket's minimum thickness is 1.4 mm, Figure 7.2.1. The MDPE contains carbon black to provide ultraviolet light protection.

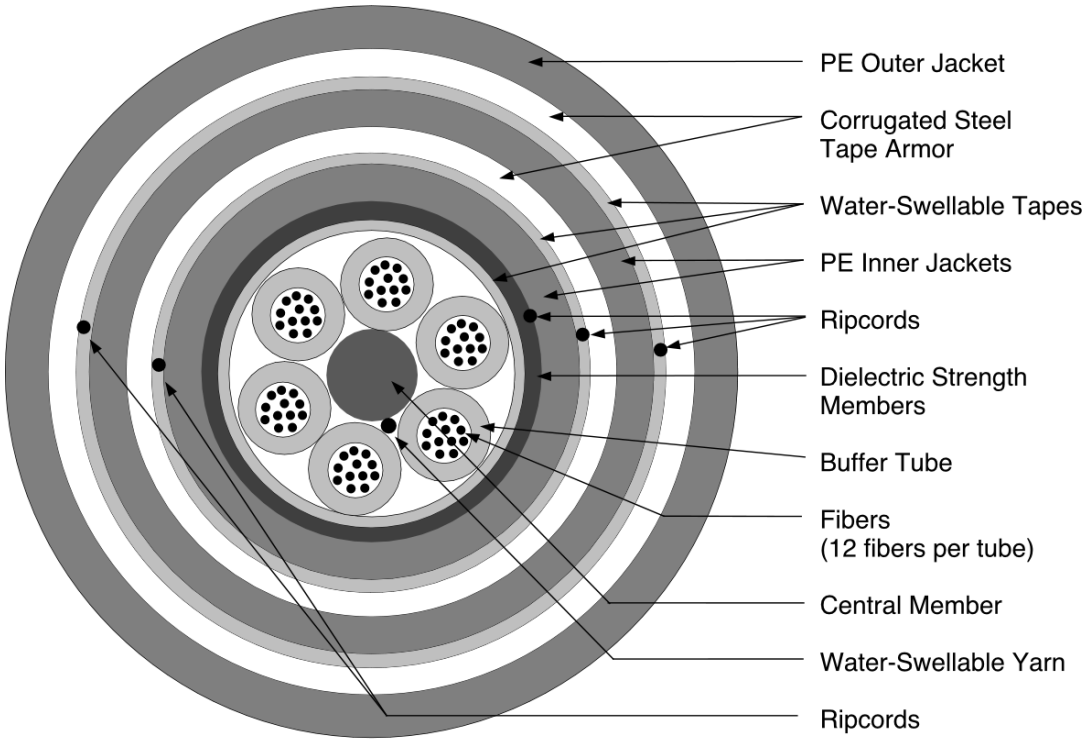

Figure 7.2.1 Double Armor Cable Construction

The fiber system is configured as shown in figure 7.2.2. These fiber counts include spares. A set of twelve single mode fibers is run to each existing pad and space is left for the future expansion.

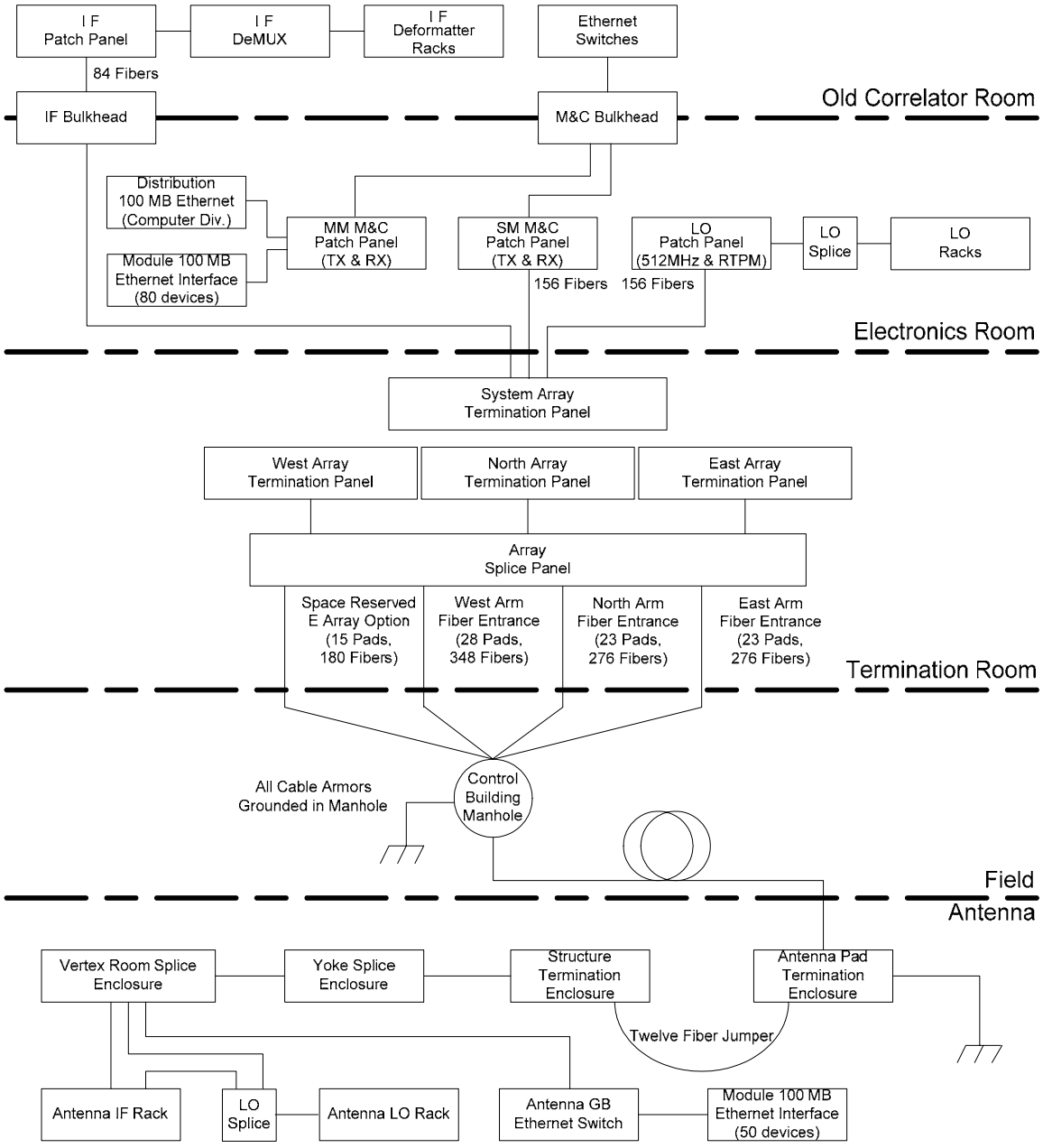

Figure 7.2.2. The fiber Configuration

The twelve fibers from each pad are grouped into trunks. These trunks either consist of 36, 60 or 96 fibers. A total of twelve trunks enter the control building, four from each arm. Figure 7.2.3 shows the configuration of the north arm. Similar configurations are used in the west and east arm.

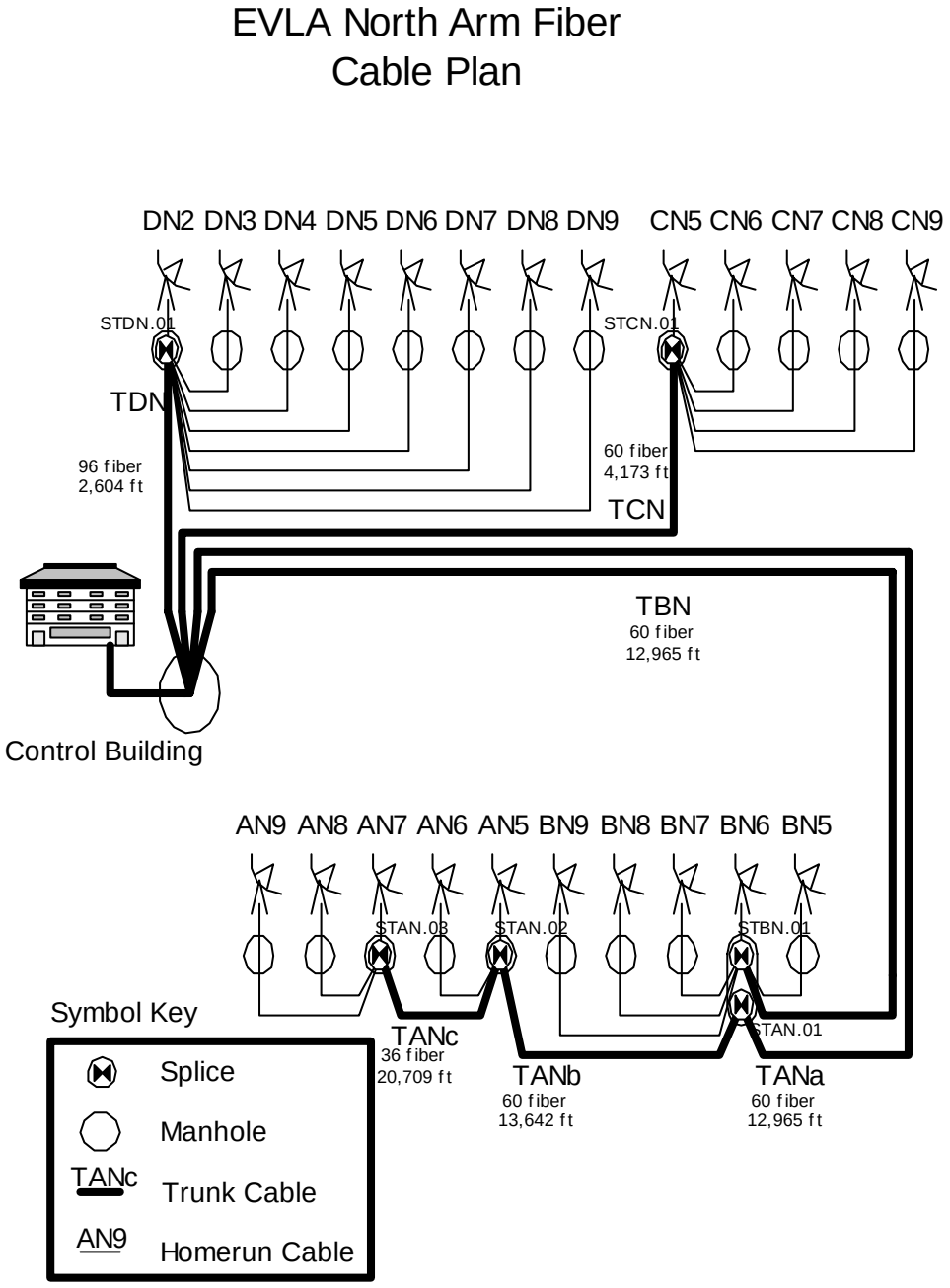

Figure 7.2.3. North Arm Trunk Configuration

The estimated lengths of the cables to each pad are shown in table 7.2.1.

Table 7.2.1 Fiber Optic Cable Lengths

EVLA Fiber Underground - Cable Lengths

East Arm

Pad	Origin	Length Feet
DE2	TDE	767
DE3	TDE	605
DE4	TDE	395
DE5	TDE	150
DE6	TDE	439
DE7	TDE	760
DE8	TDE	1,117
DE9	TDE	1,510
CE5	TCE	150
CE6	TCE	1,092
CE7	TCE	2,152
CE8	TCE	3,325
CE9	TCE	4,609
BE5	TBE	150
BE6	TBE	3,238
BE7	TBE	6,425
BE8	TBE	10,107
BE9	TBE	14,136
AE5	TAEa	150
AE6	TAEa	9,838
AE7	TAEb	150
AE8	TAEb	12,252
AE9	TAEb	26,690

West Arm

Pad	Origin	Length Feet
DE1	TDW	1,276
DN1	TDW	1,276
DW1	TDW	1,138
DW2	TDW	1,056
DW3	TDW	893
DW4	TDW	684
DW5	TDW	439
DW6	TDW	150
DW7	TCW	150
DW8	TCW	507
DW9	TCW	900
CW5	TCW	1,323
CW6	TCW	2,264
MP	TCW	2,701
AAB	TCW	3,101
CW7	TBW	150
CW8	TBW	1,323
CW9	TBW	2,607
BW5	TBW	4,000
BW6	TBW	6,773
BW7	TBW	10,100
BW8	TBW	13,781
BW9	TBW	17,811
AW5	TAWa	150
AW6	TAWa	9,838
AW7	TAWb	150
AW8	TAWb	12,252
AW9	TAWb	25,484

North Arm

Pad	Origin	Length Feet
DN2	TDN	150
DN3	TDN	294
DN4	TDN	439
DN5	TDN	655
DN6	TDN	915
DN7	TDN	1,204
DN8	TDN	1,528
DN9	TDN	1,878
CN5	TCN	150
CN6	TCN	998
CN7	TCN	1,954
CN8	TCN	3,015
CN9	TCN	4,173
BN5	TBN	3,736
BN6	TBN	150
BN7	TBN	2,928
BN8	TBN	6,125
BN9	TBN	9,755
AN5	TANb	150
AN6	TANb	8,884
AN7	TANc	150
AN8	TANc	11,057
AN9	TANc	22,991

7.3 Digital IF Data Transmission System

A Digital Transmission System (DTS) is employed within the EVLA to transmit the digitized IF signals from the antennas to the Central Electronics Building. A sustained data rate of 96 Gbits (120 Gbits formatted) is transmitted. Each polarization uses a parallel interface of three synchronized single bit high-speed serial optical fiber transmission channels. The single channel signaling protocol defines the format of the three parallel fibers.

7.3.1 Specifications and Requirements

Figure 7.3.1 shows a conceptual diagram for the signal data paths from the receivers to the fiber output at each antenna. The front-end provides simultaneous reception of two orthogonally polarized signals. Each receiver provides an instantaneous bandwidth, per polarization, of up to 8 GHz which is partitioned into four, 2 GHz wide IF-bands by the IF system. Each IF-band is harmonically sampled at 4.096 GHz and quantized to 3 bits. This produces a data stream of 12 Gbits/s per IF-band. The digitizers incorporate a de-multiplexer that reduces the clocking rate while increasing the number of bits transmitted over the fiber. This produces a 48-bit wide parallel output word clocked at a 256 MHz rate. With two digitizers paired together, the parallel word is 96 bits wide, clocked at 256 MHz. This corresponds to a 24 Gbits/s data rate per IF-bands. Each antenna can provide four IF-bands producing a total data transmission rate of 96 Gbits/s. and 120 Gbits/s formatted.

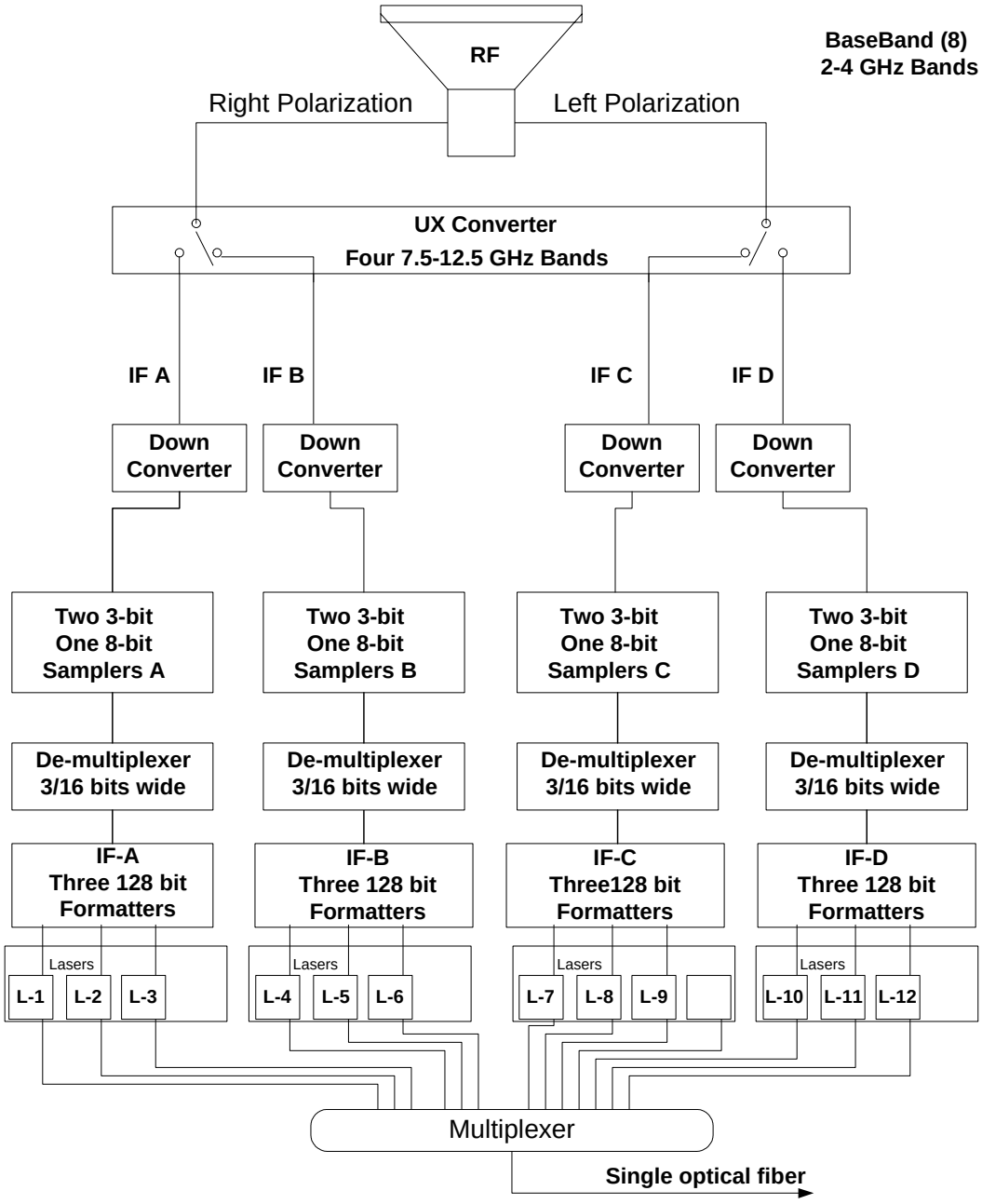

Figure 7.3.1. Conceptual Diagram of the Signal Data Path

At the central site, the DTS supplies a 96-bit wide word clocked at 256 MHz to the correlator. Each bit position in the received word corresponds exactly to an identical position in the transmitted word.

The serial protocol requirements for the DTS were derived from the end-of-life bit error rate required to support good astronomy. Typically the minimum bit error rate for good astronomy is 10^{-4} divided by the number of bits in the sync word. The EVLA sync word

is 10 bits long, thus the minimum bit error rate for good science is about 10^{-5}. Since there are twelve serial optical channels, each channel also contains a Metaframe index bit and a sequence count. These bits provide the required multi-channel synchronization to recreate the original data in the correct sequence.

The measurable system parameters are shown in Table 7.3.1.

Table 7.3.1. Measurable IF Transmission System Parameters

a.	Bit Rate:	10 Gbits/second per channel
b.	Number WDM Channels:	12 channels
c.	Channel Spacing:	200 GHz spacing
d.	Channel Wavelengths:	C Band, 1560.61 nm to 1536.61 nm
e.	Bit Error Rate:	Beginning of Life, 10^{-9}; End of life, 10^{-6}
f.	Digital SNR (Q):	Beginning of Life, 6; End of life, 4.7
g.	Maximum, fiber length	21.6 km
h.	Minimum fiber Length	0.625 km
i.	Operation Temperature	-12C to 35C

7.3.2 Samplers

7.3.2.1 High Speed (2-4 GHz) Sampler

The samplers installed in the DTS module provide the flexibility required for the fiber optic transmission of the IF. Digital conversion is of course indispensable to the correlator in order to derive the correlation function as a function of lags for spectroscopy. The samplers are thus crucial and single-point-failure elements in the system. The EVLA will incorporate 3-bit samplers thus improving the overall sensitivity compared to the 2-bit correlator. The specifications for the samplers are given in Table 7.3.2.

Table 7.3.2 High Speed 2-4 GHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	2-4 GHz	
Clock Rate	4096 MHz	
Resolution	3 bits	
Quantization	8 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/16	

Output Word Rate	256 MHz	
Power Consumption	TBD	

The sampler includes several fundamental elements briefly described below. The input adapter amplifier, the comparators and the associated latches and encoding are implemented in a single ASIC. The fast demultiplexing unit is separate from the ASIC to diminish any coupling of the digital output with the analog signal input. The ASIC and the demultiplexing unit form the sampler proper. A PLL box produces and distributes the sinusoidal 4096 MHz sampling clock and the TBD signal required by the demultiplexing unit. This is another separate unit which will be common to at least one sampler pair.

Input Adapter Amplifier
The analog signal is delivered from one of the four output of the IF downconverter modules in the 2 to 4 GHz range. It is random with Gaussian statistics. The response of this amplifier is flat within ± .5 dB over 2 GHz bandwidth and linear up to about +15 dB above R.M.S. input signal range. The voltage supply required for the adopted ASIC technology is ± 1.25 V.

The sampler input level is controlled in the IF downconverter with ±.25 dB attenuators placed in the 2-4 GHz output paths of each IF downconverter. This allow minimization of platforming effects and keeps the quantization thresholds constant and at their optimum level for maximum quantizing efficiency.

Comparators and Quantization Thresholds
The sampling function is preformed in the comparators which include two latches operated in a master-slave configuration and clocked at 4096 MHz. The 4096 MHz clock signal is equally distributed to 7 comparators. It's shaped internally in a dedicated amplifier driven by the external 4096 MHz sinusoidal signal. The seven thresholds comprise a zero reference voltage and are set around ±0.5 'sig', 1 'sig' and 1.5 'sig', where 'sig' is the R.M.S. voltage at the common input of the 7 comparators; these levels are kept constant and their exact value is tuned with an accurate division voltage chain so as to minimize the quantization losses. First simulations of SiGe samplers indicate that the sampler indecision region is small and at the level of 1% of the smallest comparison threshold.

Encoding
The sampler encoding is not yet finally adopted.

7.3.2.2 1-2 GHz Sampler

In addition to the 2-4 GHz samplers, a lower bandwidth higher resolution sampler is required. Due to higher RFI in L-Band, an 8-bit sampler will be needed. A higher number of bits allows more dynamic range and allows the correlator to better filter unwanted RFI. This sampler will be used for either harmonic or bandpass sampling, where the IF to be

sampled is in the region from 1000 to 2000 MHz. The specifications for this sampler are shown in Table 7.3.3.

Table 7.3.3 1000 to 2000 MHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	1000 MHz	
Clock Rate	2048MHz	
Resolution	8 bits	
Quantization	256 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/8	
Output Word Rate	256 MHz	
Power Consumption	TBD	

7.3.3 Transition Hardware

There will be special hardware necessary to keep the new electronics compatible with the old correlator. This hardware is necessary since the new correlator in not expected to be in place until most antennas are modified with the new electronics**.** This new hardware consists of the 8 bit sampler, a digital decimator for frequency conversion, a digital to analog converter for conversion back to an analog IF, and the current baseband filter and driver modules, T4 and T5. The 8 bit sampler data will be digitally filtered and converted back to analog and then input to the current baseband signal hardware.

7.3.4 Transition Converter

The transition converter consists of an 8 to1 digital decimator followed by an FIR filter then another 2 to 1 digital decimator followed by another FIR filter. Finally, in the transition converter there is a spectral inverter followed by a digital to analog converter. The decimators down converts the signal that was in the 1152 to 1216 MHz range to a signal that will end up in the 0 to 64 MHz range. The 1152 to 1216 MHz was chosen because of clock frequencies. The decimator clock will be 256 MHz allowing both sidebands of the IF to appear at multiples of the 128 MHz. The digital filters will be implemented in the FPGAs located in the deformatter module. The DAC will also be in this module. The final digital signal will then be fed to a digital to analog converter. The digital to analog converter needed for the transition is specified in Table 7.3.4. This D to A converter is necessary to reconstitute the digital data to analog form for the old correlator.

Table 7.3.4 Transition Digital to Analog Converter

Item	Specification	Notes
Update rate	128 MHz	256 if necessary
Resolution	10 bits	

7.3.5 IF Optical Considerations

Table 7.3.5 illustrates the power budget for the pre-amplified IF optical system. This configuration includes the gain from an EDFA and uses the ideal receiver sensitivity of -22.5 dBm to maintain the required bit error rate of 10^{-9}. The power margin for this system, with only 10 dB of gain, is 6 dB. This power margin provides headroom for system aging.

Table 7.3.5 EVLA IF Power Budget (Pre-Amplified System)

Elements	No. Units	Loss/Unit (dB)	Loss/Element(dB)
IF Rack to Vertex Room Bulkhead			
Launch Power			0.00
16ch WDM MUX	1	-6.00	-6.00
Connector	4	-0.30	-1.20
Fiber (km)	0.004	-0.30	0.00
Vertex Room Bulkhead to Antenna Pad		$P_{vtx\ bulkhead}$ = -7.20	
Connector	0	-0.30	0.00
Fiber (km)	0.02	-0.30	-0.01
Farthest Antenna Pad to CB Termination Panel		$P_{last\ antenna\ pad}$ = -7.21	
Umbilical Cable	2	-0.30	-0.60
Connector	0	-0.30	0.00
Fiber (km)	22	-0.30	-6.60
Splice	2	-0.10	-0.20
Bends	18	-0.10	-1.80
CB Termination Panel to Patch Panel		$P_{termination\ panel}$ = -16.41	
Connector	3	-0.30	-0.90
Fiber (km)	0.02	-0.30	-0.01
EDFA Gain	1		10.00
Correlator Patch Panel to Correlator Receiver		$P_{IF\ patch\ panel}$ = -7.31	
Fiber (km)	0.004	-0.30	0.00
Connector	5	-0.30	-1.50
16ch WDM DMUX	1	-6.50	-6.50
Received Power			-15.31
Aggregate Noise (N)			1.00
Receiver Sensitivity			-22.50
Loss Margin			6.19

7.3.6 Transmission Protocol

The digital protocol is based upon a 160-bit frame structure and line coding exploiting scrambling techniques. The protocol is described in detail in the EVLA Memorandum #33 - "Digital Transmission System Signaling Protocol" Version 2, November 2001.

The frame is composed of a divided 10-bit sync word, 1 meta-frame index bit, a 5-bit sequence count, a 1PPS, a 1pulse per 10 seconds, a data valid bit, a 8 bit checksum, Figure 7.3.2. The first 4 payload bits are carried in locations 12 through 19 with the remaining 124 contiguous bits beginning with the bit location 20.

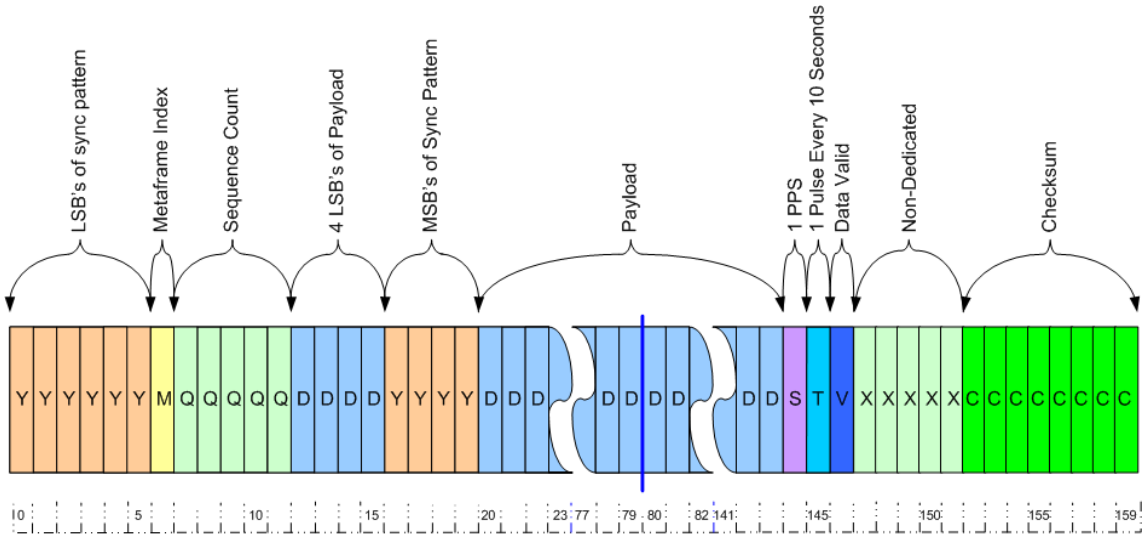

Figure 7.3.2 The Data Frame

Channel coding is used to scramble each 10 Gbits/second optical channel to facilitate proper reception. Channel coding provides better timing information and minimizes low frequency content. The EVLA uses a channel coding technique that produces almost an equal number of ones and zeros per frame. This scrambling technique reduces systematic jitter.

7.3.7 Transmitter (Antenna) Hardware Design

The formatter uses the Xilinx Virtex E/2 series Field Programmable Gate Array and a 10-Gbits/s-16:1 multiplexer IC made by several manufacturers for SONET OC192 communications. Integrated Laser/Optical Modulator devices are used to transmit the 10 Gbits/s signal onto the 12 fibers. The twelve fibers from the transmitters in each antenna are combined onto a single fiber using a passive 12:1 fiber multiplexer.

7.3.8 Formatter Configuration

The 256 MHz to 10 GHz rate conversions produces a natural 80 bit wide word. This word consists of 16 format bits and 64 data bits. Two consecutive 80-bit words are combined to produce a 160-bit frame. The 160-bit frame is produced at an effective 64 MHz clock rate and time division multiplexed by 160. To maintain the order of the frame, a 16-bit partitioning and re-ordering circuit is used. It is placed between the input selector and the two 5:1 output multiplexers inside the formatter chip. This re-ordering is necessary to correct for the shuffling of the output selector.

A simplified formatter block diagram showing a 64-bit input bus, input selector, partition and re-ordering circuit, the addition 16 overhead bits, the times 5 multiplexers, the output selector and the final times 16 multiplexer is shown in Figure 7.3.3. Sixteen format bits are associated with each 64 data bit group. These bits are used for frame and Meta-frame synchronization, timing bits and transmission of the checksum word.

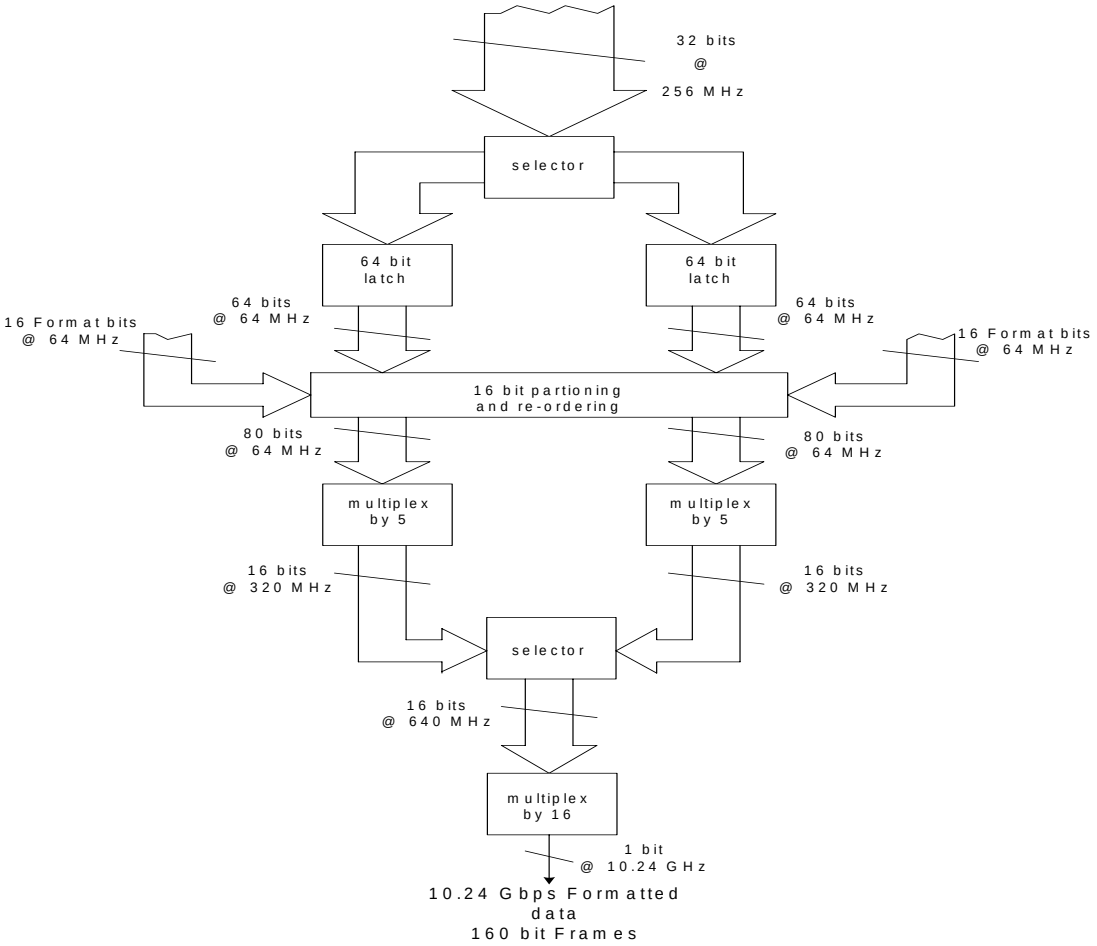

Figure 7.3.3. Simplified Formatter Block Diagram

7.3.9 Frame Synchronization

The sync word pattern is located at the same location in each frame although it is divided into two separate locations. The sync word is composed of ten bits of a unique pattern. The selected 10-bit pattern is similar to the seven-bit Barker sequence (binary 0100111). The pattern order is not important.

As with the transmitter, the receiver implementation utilizes a 16-bit wide data selector. This data selector follows the high-speed 1:16 de-multiplexer and shuffles the incoming 16-bit words. Partitioning the sync word makes it possible to correctly locate the beginning of a frame and determine the data shuffling. The location of the first six bits of the sync word corresponds to the least significant bits of the 160-bit frame.

Frame synchronization moves through three stages: the search stage, the check stage and the monitoring stage. A 160-bit candidate frame is selected from the incoming serial bit stream. The ten sync location bits are checked for the pattern. If unsuccessful, a subsequent frame delayed by one bit time is selected and the comparison repeated. This process of changing the frame selection delay and sync pattern comparison repeats until a candidate frame is located. If no delay produces a match, the alternate shuffled possibility is checked according to the same algorithm. The matching criterion for the pattern comparison requires that all ten bits must match.

Once a candidate frame is located, the synchronization process enters the second or check stage. Since it is possible to correctly detect the sync pattern in a data stream the presence of the check stage is needed to improve the accuracy of detecting the true sync pattern. At least seven out-of-eight frame sync patterns must successfully identify that the true frame has been located. The possibility of a transmission bit error must be permitted. If this procedure fails, the system returns to the search phase and begins a new search.

In the monitoring stage, the system continually monitors the sync pattern for frame slippage. Two sequential mismatched frames or the mismatch of more than one of eight sequential frames will return the system to the search stage. The search begins as soon as an erroneous frame has been detected. In any situation where the search stage is re-entered, the search begins from the current shift value and not from a zero shift.

7.3.10 Sequence Count Implementation

To maintain frame concurrence across the three optical channels used to transmit each IF polarization, the formatter inserts an identical incrementing sequence count (0-31) into each frame. This count is extracted by the three receivers, compared, and delays applied to the early arriving channels. The result is three simultaneously clocked 160-bit frames with the identical incrementing sequence count. Therefore, the received word will be identical to the transmitted word.

Together with the unique sync pattern, the sequence count (0-31) provides a duration in time that is larger than the largest expected propagation time differences between channels. These differences arise due to inherent fiber characteristics and variations in dispersion and group delay with environment. Representative dispersion values for the

Conventional band (C band: 1530 nm - 1565 nm) of single mode optical fiber optimized for use in Dense Wavelength Division Multiplexing (DWDM) applications are about 16 ps/nm/km to 18 ps/nm/km [3]. With 25 km of fiber and assuming a worst-case situation of two optical carriers separated by the maximum of 24 nm (the reddest red to the bluest blue), this only amounts to 2.4 ns (24 bit times). The maximum calculated delay is about 10.1 ns (101 bits). These values scale linearly with distance. For the assumed distance and fiber types, two 160-bit frames would be satisfactory.

7.3.11 Metaframe Implementation

The metaframe bit is set once every second for one frame. (This is presently redundant with the 1-PPS bit)

7.3.12 Data Integrity

The intrinsic bit error rate of the electro-optical components in the fiber transmission system is expected to be extremely low. However, in addition to the laser diode source, high-speed modulator, photo-diode detector, AGC amplifier, and the clock and data recovery electronics associated with each channel, the EVLA system includes a large number of manually re-configurable optical fibers and connectors. With each individual channel comprised of a number of complex high-speed components and multiple fiber segments, the need for continuous performance monitoring is obvious.

Presently 8 bits of each frame are used as a checksum of the previous 152 bits. This method detects all odd numbers of errors introduced in each 19-bit group.

7.3.13 Scrambling

Channel coding is the process of modifying the source data stream to facilitate proper reception. The source is composed of both payload information, whose characteristics are known only in a statistical sense, and overhead information. The sync pattern and sequence count parameters of the overhead are known, but not the other overhead bits. Thus channel coding is essential to provide adequate timing and to minimize low frequency content of each frame. Sufficient timing information is necessary to permit regeneration of the original data and to ensure low systematic jitter [2]. Data recovery and symbol timing is determined by a phase locked loop system operating on the high-speed channel data stream. It requires sufficient transitions per reciprocal loop bandwidth to properly operate. More data transitions produce less jitter and lower recovered bit error rates due to clock extraction timing errors.

To maintain low bit error rates low frequency content should be minimized. Equal numbers of ones and zeros produce a balanced signal with minimal low frequency content. This is important in AC coupled systems.

The Frame Synchronous Scrambling (FSS) will be is used in the EVLA to provide adequate timing and to minimize low frequency content. The entire frame, except for the ten sync bits, will be scrambled by a static random pattern. A selected scrambling pattern

is added modulo 2 to the remaining bits of the frame with the first generated scrambling bit added to the eighth frame bit. A Shift Register Generator (SRG) produces the scrambling pattern and the pattern "runs" continuously throughout the 153 bits of the pattern. A seven stage SRG producing a 127-bit length sequence is used. The 153-bit pattern produced with a generator polynomial of 1 + X^6 + X^7 and a seed or initial value of hexadecimal 46 has the required randomness properties [4]. The scrambling pattern has 77 ones and 76 zeros achieving almost perfect DC balance. Table 7.3.6 shows the run length distribution of ones and zeros.

Table 7.3.6, Run length distribution of ones and zeros for 153-bit scramble pattern.

Run Length	Number of Ones	Number of Zeros
1	19	20
2	11	10
3	5	6
4	2	2
5	1	1
6	0	1
7	1	0

Table 7.3.6 also indicates the small amount of low frequency content in the pattern. The pattern has a total of only 4 runs of length greater than 4 bits with the longest one being only 7 bits. With a frame static pattern, the scrambling operation is performed in parallel across all frame bits from a single pre-loaded 153-bit long register. This register is implemented as an array of 20 byte-sized words, which are dynamically loaded with the desired pattern.

7.3.14 Self Test

Self-testing mechanisms are essential for the operational success of the EVLA DTS. These capabilities are different from the continuous error monitoring afforded by the inclusion of the checksum. Once a basic system fault has been detected, self-testing mechanisms will be provided to enable maintenance personnel to quickly isolate and repair the fault. The MCB will control the test pattern generator located in each transmitter formatter.

To check the clock recovery circuitry, a simple alternating pattern of ones and zeros is transmitted. In this mode, no frame or meta-frame synchronization, checksum calculation, or scrambling operations occur. Adding the ten-bit sync pattern to the test pattern allows frame detection diagnostics. Enabling the five-bit incrementing sequence number provides multiple channel synchronization testing. Enabling the scrambler with fixed payloads of all zeros or all ones tests scrambling. In the previous two cases, the checksum generation is disabled.

The final diagnostics evaluates the checksum system. Pattern 6 involves the checksum generation and checking of a 128-bit pattern of all zeros. Pattern 7 uses a pattern of all ones. The remaining test patterns involve forcing an error in the checksum generation using the previous simple payload patterns. Table 7.3.7 summarizes these diagnostics patterns.

Table 7.3.7. Diagnostic modes.

Pattern 1	10 GHz clock Recovery	160 bits of alternating ones and zeros
Pattern 2	Frame Detection	Sync pattern + 153 bits of alt. ones & zeros
Pattern 3	Multiple channel synch	Sequence word + 148 bits ones and zeros
Pattern 4	Scramble + data pat #1	enable scrambler plus 148 bits of zeros
Pattern 5	Scramble + data pat #2	enable scrambler plus 148 bits of ones
Pattern 6	chksum with pattern #1	checksum of 128 + 3 bits of zeros
Pattern 7	chksum with pattern #2	checksum of 128 + 3 bits of ones
Pattern 8	forced chksum error #1	erroneous checksum of 128 + 3 bits of zeros
Pattern 9	forced chksum error #2	erroneous checksum of 128 + 3 bits of ones

Most of these diagnostic tests patterns use a twenty (20) byte dynamically loadable scrambling register. By combining the ability to disable the two 64-bit input words and changing the scrambling pattern all tests all of the above patterns can be generated, except those involving checksum generation.

7.3.15 IF Optics and WDM Systems

The twelve 10Gbits/s channels in each antenna are transmitted on the fiber by 5mw 1550nm lasers with integrated Electro-Absorption (EA) modulators. The current and temperature in the lasers is closely regulated to ensure wavelength stability and long life. Temperature, current and optical power are continuously monitored to provide information on the health of the laser to ensure reliable operation of the system at the lowest possible bit error rate.

The twelve optical carriers from each antenna are combined onto a single fiber using Wavelength Division Multiplexing (WDM). This requires the use of different wavelength Lasers for each of the twelve optical carriers from each antenna. These wavelengths fit onto the International Telecommunications Union (ITU) grid that defines 1550nm class wavelengths at 200GHz spacing, Table 7.3.8. The exact wavelength of each laser is factory set and is by specified when each device is purchased. This adds some complexity to configuration control and maintenance of the IF Data Transmission System. All twelve different wavelength lasers will have spares. Care must also be taken to track where these lasers are in the system and to make sure failed lasers are replaced with units operating in the same wavelength.

Table 7.3.8, DWDM Laser Frequencies and Wavelengths

Channel Number	Frequency (THz)	Wavelength (nm)	Signal
21	192.1	1560.61	D304-2^0
23	192.3	1558.98	D304-2^1
25	192.5	1557.36	D304-2^2
27	192.7	1555.75	D303-2^0
29	192.9	1554.13	D303-2^1
31	193.1	1552.52	D303-2^2
33	193.3	1550.92	D302-2^0
35	193.5	1549.32	D302-2^1
37	193.7	1547.72	D302-2^2
39	193.9	1546.12	D301-2^0
41	194.1	1544.53	D301-2^1
43	194.3	1542.94	D301-2^2

A typical semiconductor distributed feedback laser diode used as the transmitter in the optical channel has a mean time before failure, MTBF, of about 200 years. The EVLA array will contain 336 optical channels, thus on average over the 20-year design life, one laser will fail every 7 months. Reliability is very important. Unanticipated failures are very costly in terms of degraded observations. With so many expected failures, it is essential for the VPB design to use operational diagnostic and monitoring information.

7.3.16 IF Optical Performance

The optical transmitter board accepts three electrical signals; NRZI modulated board at 10Gbits/s, from the main transmitter board and converts them to three corresponding optical signals for transmission over fibers.

The main components on the board are the three Electro-absorption Modulated Isolated Laser Modules (EMLs). Each of these comprises a laser diode and an associated back detector power monitor, an electro-absorption modulator, a thermoelectric cooler (TEC) and an associated thermistor. To obtain consistent operation of the fiber optic link, the laser will be run at constant power. This is achieved by using a Laser Diode Driver, such as the Hyteck HY6330, to monitor the output power and control the current drive to the diode. To avoid wavelength changes and to fine-tune the operating wavelength of the laser it is necessary to maintain the diode at a constant temperature with a tolerance of 0.1C°. This is achieved by using a thermo electric cooler controller, such as the Linear Technology LTC1923 to measure the temperature and drive the TEC with a PWM waveform. “Atacama Large Millimeter Array Hardware Definition, ALMA-50-02-03-01, 2002-04-10, Dave Brown & Mike Bentley”

The system is controlled and monitored by a PLD microcontroller, which is interfaced to the EVLA Monitor and Control Bus. The microcontroller is connected to DAC and ADC devices to measure power-supply voltages and TEC currents. The laser power, current

drive and temperature are measured by 12-bit ADCs. The required laser power and temperature and the maximum permitted laser current are set by 12 bit digital to analog converters. Various operating points for the modulator are set in the same way.
The power for the modules is derived from the 48V system bus. The microprocessor is powered directly from the five-volt supply on the main board and can turn on and off the DC-DC converters, which power the modules.

A typical eye pattern through one meter of fiber is shown in figure 7.3.4. The signal-to-noise quality of this eye needs to be better than Q=34.

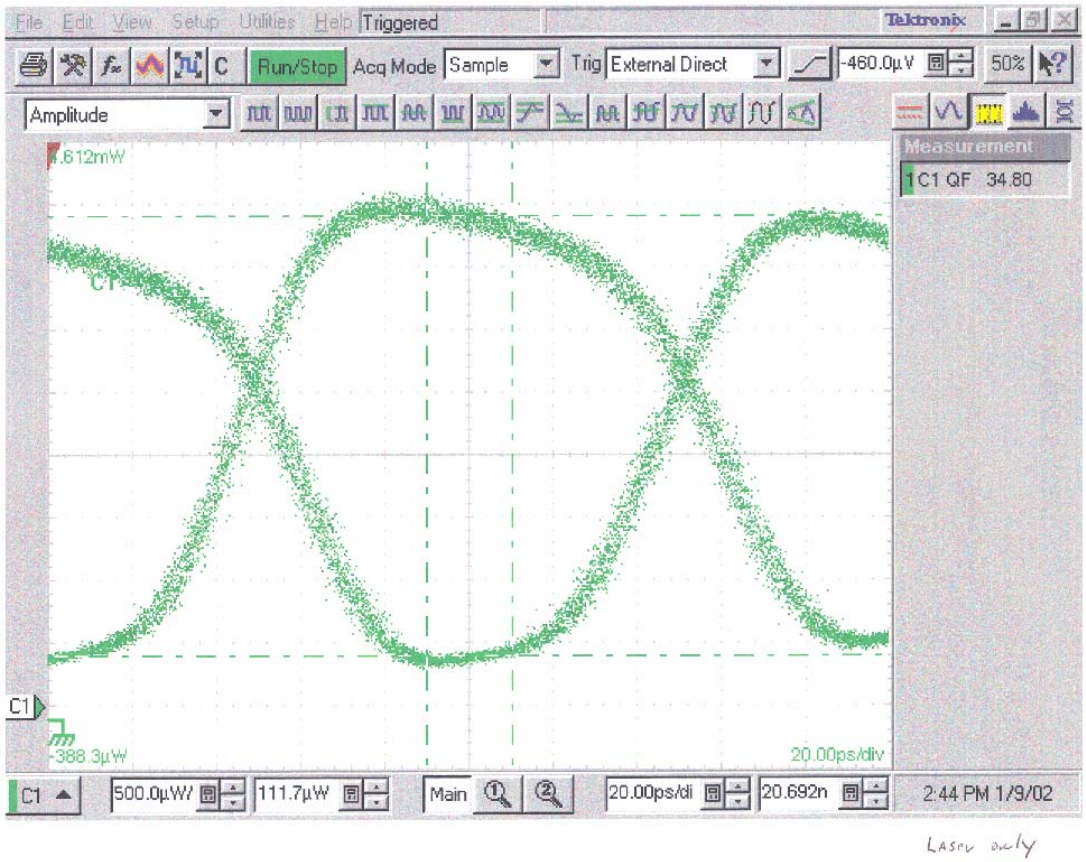

Figure 7.3.4. A Typical EVLA Eye Pattern out of the Laser

7.3.17 IF Power Supplies

All IF Digital Transmission System (DTS) hardware is powered from a single 48 Volt DC power source. The input power source is distributed to two Power Supply Boards, one for the formatter and the other for the digitizer. Individual voltages are derived from the 48 VDC power source by efficient, high reliability DC/DC converter modules located on each Power Supply Boards.

7.3.18 IF Hardware Description

The hardware used in the IF DWDM is described.

Field Programmable Gate Array

The formatter uses Xilinx Virtex –E or Virtex-2 Field Programmable Gate Arrays (FPGA's). These devices accept input data from the digitizer system, perform all formatting, generation of error checking codes, and output the data and framing multiplexed into 625MHz 16 Bit words. All designs for the Xilinx FPGA's are done in the VHISI Hardware Description Language (VHDL – IEEE std 1076.3) utilizing Xilinx's Foundation series software.

The OC-192 Multiplexer

The 16:1 Multiplexing is accomplished using commercial SONET OC192 multiplexer IC's mounted on mezzanine printed circuit boards. Devices are available from AMCC and Giga/Intel. Future devices are expected from Maxim and several other manufacturers. The IC's are mounted on separate mezzanine boards. This was done to 1) reduce costs by using 10 Gbits/s design techniques and materials only on the smaller mezzanine boards, and 2) protecting us from the volatility of the rapidly changing telecommunications market.

Manufacture and Assembly

The modules will be manufactured and assembled in Socorro, New Mexico.

7.3.19 Transmitter Module Cooling Requirements

This module is an RFI tight sealed container. RFI tight air vents cover the top and bottom of each DTS module. Chilled air forced upward through the rack passes through the modules to remove heat.

7.4 Digital IF Deformatter

7.4.1 Deformatter Hardware Design

The deformatter accepts three optical inputs modulated at 10Gbps and converts them to three corresponding electrical signals. . The main components on the board are the three optical receivers, the Multiplex MTRX192L, which each comprise of a PIN photodiode, a trans-impedance amplifier and a limiting amplifier. The gains of these receivers is sufficient to ensure that they can be interfaced directly to following clock and data recovery chips without sacrificing dynamic range. The deformatter is built around the Altera Field Programmable Gate Array and a 10 Gbits/s 1:16 de-multiplexer made for SONET OC192 communications systems.

7.4.2 Deformatter Correlator Interface.

The interface between the Fiber Receiver module and the correlator station card transfers the digital data received over the optical IF data link to the correlator station card.

The interface provides three 32 bit data paths. Each data path corresponds to one of the three fibers processed by a module. Each bit in the data path transfers data at 256 Mega bits per second. The module provides a 128 MHz double data rate clock synchronized to the data. Four consecutive data words contain the data from one received frame.

The correlator station card provides the deformatter board with a 64MHz reference clock. The multiplexer in the receiver portion of the board arranges to provide the correlator the first word of a frame as the first word delivered after a rising edge of the 64 MHz reference clock. The 128 DDR clock provided by the deformatter is derived from the 64 MHz reference clock from the correlator by a phase locked loop in the receiver FPGAs. This is done to minimize skew between data bits and their associated clock.

The deformatter board provides the correlator a 1 second and a 10 second pulse derived from the received data frames. The monitor and control system will arm counter logic in the FPGAs in the 52-millisecond period between a 1 second and a 10 second time of coincidence. The next received frame with a metaframe index bit set will start the counters. The received frame clock in the deformatter logic clocks the counters generating the 1 second and 10 second pulses.

The deformatter board provides a data invalid bit to the correlator. The bit is set by the following conditions: 1) The deformatter is not synchronized to the received data frames or 2) The frame counters of the three channels are not equal or 3) When the eight bit data is in over range.

The 8 bit digitizers are flash type analog to digital converters. As a result, they saturate on input over range. The deformatter logic uses the codes corresponding to highest and lowest input voltage to detect input over range and sets the data invalid bit when these are detected. Over range operation with the three bit digitizers is TBD.

7.4.3 Power Supplies

All IF Digital Transmission System receiver hardware is powered from the 48 Volt DC battery power system in the WIDAR Correlator. The following local voltages required:

+1.5 VDC
+3.3 VDC
+5.0
-5.2 VDC
+12 VDC

These voltages are derived from the 48 VDC power source by efficient, high reliability DC/DC converter modules located on each printed circuit board.

7.4.4 IF De-Formatter Description

The hardware used in the IF De-Formatter is described.

Field Programmable Gate Array

The receiver uses an Altera Field Programmable Gate Arrays (FPGA's). This device accepts data from the 1:16 de-multiplexer IC, performs all synchronization, error checking, buffering and multiplexing functions. Data is output as 250 MHz 48 Bit words to the WIDAR Correlator. All designs for the FPGA's are done in the VHISI Hardware Description Language (VHDL – IEEE std 1076.3).

The OC192 De-multiplexer

The 1:16 de-multiplexing is accomplished using commercial SONET OC192 de-multiplexer IC's mounted on mezzanine printed circuit boards. Devices are available from AMCC and Giga/Intel. Future devices are expected from Maxim and several other manufacturers. The IC's are mounted on separate mezzanine boards to 1) reduce costs by using 10 Gbits/s design techniques and materials only on the smaller mezzanine boards, and 2) reduce the impact of parts becoming obsolete.

Optical Electronics

The optical portions of the receiver modules are built on to a second mezzanine printed circuit board. These modules contain the photo receiver and all associated monitor and control circuitry.

Physical Packaging

The receiver module is built as an open frame module designed to be used as a mezzanine module on the Widar Correlator Station Card. It is built using a main Printed Circuit Board (PCB) with the fiber optic receiver and 1-16 de-multiplexer cards attached above it as mezzanine cards. It is designed to receive data from fiber optic cable from the WDM de-multiplexer, output data to the Widar Correlator through its mezzanine connector(s), and output data through a secondary port to be used during the transition period to feed data to the existing VLA systems.

Manufacture and Assembly

Due to the number of units required and the type of components used, these modules are best suited to fabrication on a commercial assembly line**.**

7.4.5 Optics and WDM Systems

The twelve 10Gbits/s channels in each antenna are transmitted on the fiber by 5mw 1550nm lasers with integrated Electro-absorption (EA) modulators. The twelve optical carriers from each antenna are combined onto a single fiber using Dense Wavelength Division Multiplexing (DWDM). This requires the use of different wavelength Lasers for each of the twelve optical carriers from each antenna.

The twelve different wavelength carriers are separated at the receiving end using a DWDM de-multiplexer. The resulting carriers are now on twelve discrete fibers and are to be distributed to the receiver modules as required. The fibers terminate into an integrated photo receiver device. This device contains a biased photodiode that converts the signal back into electrical form. The output of this diode is AC coupled to a trans-impedance amplifier to drive the 50-ohm impedances of the following stages. This signal is then amplified and leveled and fed to the input of the 1:16 OC-192 de-multiplexer IC.

7.4.6 IF Receiver Signal Interfaces

VPB Transmitter Module:
Inputs: 250/256 MHz, LVDS Digital Data from Digitizers

VPB Receiver Module
Outputs: 250/256 MHz, LVDS Digital Data to WIDAR Station Card and/or Transition Data Converter

7.4.7 Reference Signal Interfaces

VPB Transmitter and Receiver Modules
Inputs: 250 MHz Sine wave or LVDS System Clock and the 19.2 Hz LVDS timing signal

7.4.8 Monitor Control Interface

VPB Transmitter and Receiver Modules
I/O: M&C Ethernet Interface – 10/100BaseT or Fiber Pair
Module ID: 3 or 4 wire SPI interface to ID PROM on the Backplane

7.4.9 Power Supply Interfaces

VPB Transmitter and Receiver Modules

Power: 48 Volts DC

7.4.10 Receiver Module Cooling Requirements

This module is built as a vertically oriented, open-frame type module that is mounted to the station card in the WIDAR Correlator or to a temporary card plugged into a backplane during the transition. This module is directly cooled by chilled air forced upward through the rack passes over this heatsink to remove heat from the module. Heat producing components in this module are either designed for this type of application or have small, finned heat sinks attached to them to dissipate heat.

7.5 LO Reference Distribution System

This section addresses the requirements for the distribution of the LO references over the fiber optic link. This includes the measurement of the round trip phase. This part of the LO reference distribution system consists of four modules, the LO Offset Generator (L351), the Round Trip Phase Receiver (L352, the Central LO Transmit/Receiver (L353), and the Antenna LO Transmit/Receiver (L304). This system sends out a 512MHz signal on the LO-transmit-fiber then this signal is returned on the LO-receive-fiber and compared with a 512MHz that has been offset by 128Hz. The resulting 128Hz is then

compared to the central 128Hz to complete the measurement of the residual round trip phase. The 512MHz sent to the antenna is cleaned-up and is used for the primary reference for the antenna LO system. A reset or synchronization pulse is transmitted over the LO fiber. The pulse is sent on command and is not periodic. The reset or synchronization pulse is thoroughly explained in chapter 6, the LO chapter.

7.6 Monitor Control System (Antenna & CEB electronics systems)

The EVLA monitor and control system will be based almost entirely on commercially available fiber optic based 1-Gigabit Ethernet technology. 1-Gigabit Ethernet is installed between the control building and the antennas. 100 Megabit Ethernet will be distributed throughout the antenna for Monitor and Control of each module.

7.7 Fiber Optic and Laser Safety Requirements and Procedures

The fiber optic and laser safety procedures are written and adopted by the Safety Office and the Laser Safety Officer. Based on ANSI Z136.2-1997, the *American National Standard for Safe Use of Optical Fiber Communication Systems Utilizing Laser Diode and LED Sources*, the potential hazards are identified and procedures written for the safe operation of lasers. The potential hazards are identified in Figure 7.7.1.

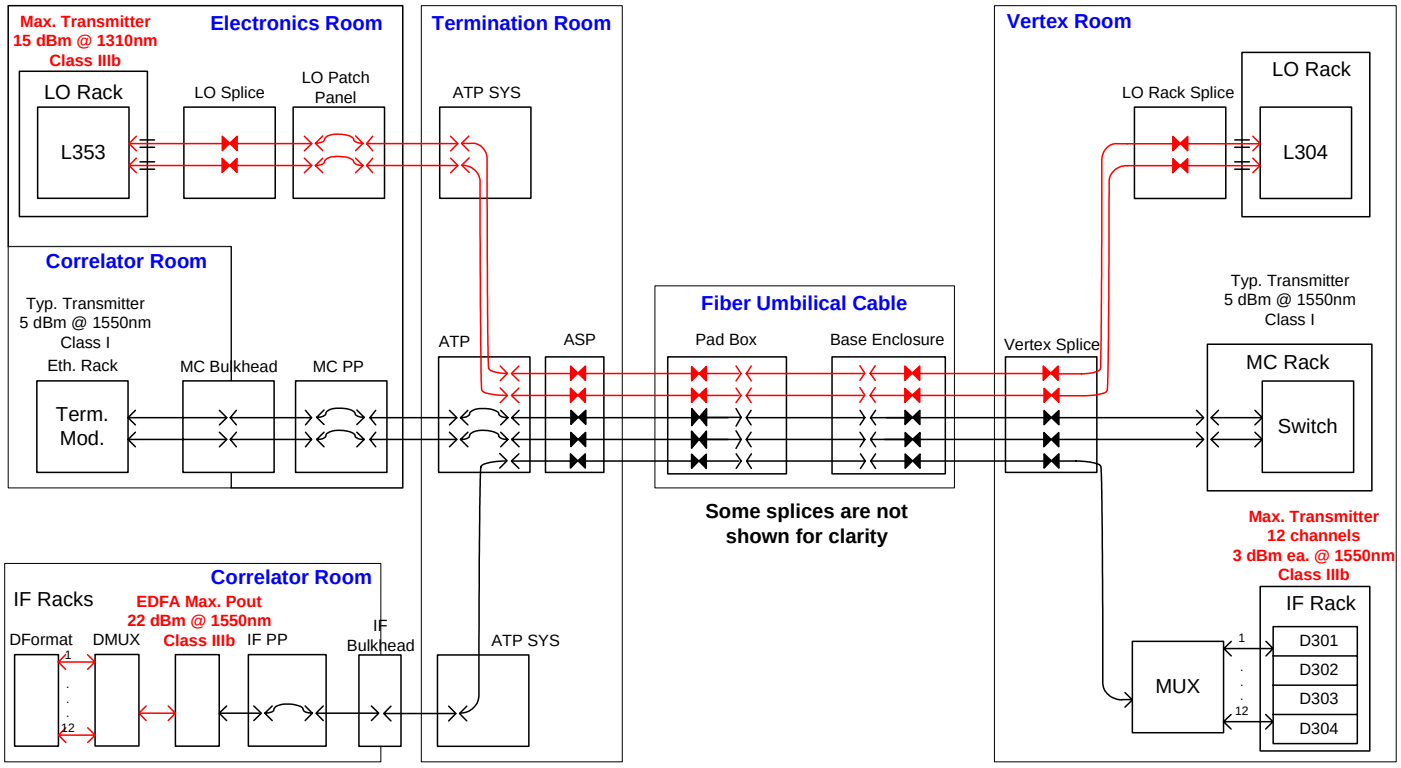

Figure 7.7.1 Potential Laser Hazards for EVLA.

Fiber optic cables shall be specified and installed in accordance with the latest version of NFPA 70, National Electrical Code (NEC).

7.7.1 Fiber Optic Installation Standards and Procedures

Installation of direct burial cable shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Direct Buried Cable Installation', IP012 Direct Buried Cable Installation, lists tools and materials, precautions and procedures of installation of direct burial cables. The procedures described in IP012 are similar to any standard cable trenching procedure, but with particular emphasis on minimum bending radius and cable loading issues.

In no case shall the minimum bend radius be less than 15 times the cable diameter. Maximum cable tension shall not exceed 600 pounds (2700N). Twisting shall be avoided.

The minimum burial depth shall be 1 meter, and a marking tape shall be placed at 0.5 meters. The minimum burial depth may be relaxed to 0.6 meters, and the marking tape placed at 0.3 meters, to maintain adequate spacing to other utilities. The extent of this relaxed specification shall be limited to 3 meters in length, and may only be relaxed when any reasonable measure to avoid the obstacle is not practical.

The minimum separation of the fiber-optic cable from a parallel utility cable shall be 1 meter. The minimum separation of the fiber-optic cable from a perpendicular utility cable shall be 0.5 meters. The minimum separation shall be observed regardless of voltage range. Refer to EVLA Memorandum 41, Lightning Protection for Fiber Optic Cable.

Reel preparation shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Reel Preparation for Installation (Export) Procedure', IP045 Reel Preparation (Export), lists tools and materials, precautions and procedures for reel preparation.

7.8.1.8 Grounding of Fiber Optic Cables

Cable armors shall be bonded to an existing structure counterpoise with no smaller than 6AWG copper wire. Where double armor cable is used, both armors shall be bonded together. Bonding of direct burial cable armors shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Bonding and Grounding Procedure for Loose Tube Cable Designs', IP024 Cable Bonding, lists tools and materials, precautions and procedures for grounding of cables.

Where an existing structure counterpoise is not available, a four-leg star counterpoise shall be constructed over the cable bonding point using 6AWG copper wire. Each leg of the star counterpoise shall be no less than 6 meters (20 ft.) in length. The counterpoise shall be placed at 0.5 meters depth, and the cable shall be placed at 1 meter depth. Refer to EVLA Memorandum 41, Lightning Protection for Fiber Optic Cable.

All bonds shall be made using exothermic welds or compression terminals. Bolted connections shall be made tight using anti-corrosion copper conductive compound.

7.7.2 Fiber Optic Cable Repair Standards and Procedures

Repair of direct burial cable shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Sheath Repair for Armored and Non Armored Cable', IP037 Sheath Repair, lists tools and materials, precautions and procedures for repair of cables. Procedures are described for various types of damage including armor damage. Damaged sections described as severe in IP037, section 8.5, where the inner core is exposed, shall be removed and replaced to the extent that no cable damage remains.

7.7.3 Splicing of Direct Burial Fiber Optic Cable

Spicing of direct burial cable shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Guideline for Optical Fiber Splicing', IP028 Fiber Splicing Guidelines, lists tools and materials, precautions and procedures for splicing of cables. Additionally, all cable armors shall be bonded together as described in section 7.8.1.8 of this Project Book chapter.

The preferred location of cable splices is one of the existing waveguide manholes. Where no manhole is near the splice may be buried at a minimum depth of 1 meter. The cable armors shall be grounded to a star counterpoise as described in section 7.8.1.8. The splice location shall be marked with a concrete monument.

7.7.4 Emergency Cable Restoration

Emergency restoration of direct burial cable shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Emergency Cable Restoration for Fiber Optic Cable Systems', IP015 Emergency Restoration, lists tools and materials, precautions and procedures for restoring of cables.

7.7.5 Acceptance Tests for Fiber Optic Cables

Testing of fiber optic cable shall follow the standards of the manufacturer, OFS Brightwave Carrollton, Carrollton, GA. The OFS Installation Practice 'Guideline for Field Testing of Singlemode Fiber Optic Cable Systems', IP029 Field Testing, lists tools and materials, precautions and procedures for testing of cables. Further guidelines for testing fiber optic cables are described in EVLA Memo 40, Fiber Optic Cable Acceptance Tests.

REFERENCES

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[2]: Fair, I. J., Grover, W. D., Krzymien, W. A. and MacDonald, R. I., "Guided Scrambling: A new line coding technique for high bit rate fiber optic transmission systems," IEEE Transactions on Communications, vol. 39, no. 2,
pp 289-297, February 1991.

[3]: Corning Incorporated, "Corning single-mode optical fiber", Data sheet PI1036, July, 2000.

[4]: Golomb, S. W., "Shift register sequences", pp 24-27,43-47, Holden-Day, Inc., San Francisco, 1967.