EVLA Project Book, Chapter 9

EVLA Monitor and Control System

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Summary

This chapter outlines the general requirements and design considerations for the EVLA Monitor and Control System, including hardware, software, and computing systems.

Current milestones for the Monitor & Control System are as follows:

Milestone	Date
EVLA System PDR	2001/12/04
Monitor & Control PDR, Software & Hardware	2002/02/18
EVLA System CDR	2002/12/02
Monitor & Control CDR	2003/01/02
Begin Test & Debug of 1st EVLA Antenna	2003/01/02
Freeze Electronics Design, Begin Production	2003/10/01

9.1 Introduction

9.2 Specifications and Requirements

Currently (11/2001), the process of gathering requirements for Engineering and Operations is just beginning. Initial drafts of the documents have been written and distributed. Some comments on the initial drafts have been received. After all interested parties have submitted their comments, they will be reviewed and analyzed. The documents will then be revised and distributed to a larger group for further comment and discussion. Some Scientific requirements have been compiled, but those requirements are still in a raw form. They have not yet been analyzed for system specifications.

9.2.1 Scientific Requirements

The document being used as the basis for the Scientific Requirements can be found at http://www.aoc.nrao.edu/evla/memolist.shtml, under the title "Scientific Requirements for the EVLA Real-Time System", edited by John Benson and Frazer Owen, dated 09/26/2001.

9.2.2   Engineering Requirements

The initial draft of the Engineering Requirements document can be found at
http://www.aoc.nrao.edu/evla/techdocs/computer/workdocs/index.shtml, under the title "Antenna M&C Subsystem Preliminary Requirements Specification", by Kevin Ryan, dated 11/15/2001.

9.2.3   Operations Requirements

The initial draft of the Operations Requirement document can be found at
http://www.aoc.nrao.edu/evla/techdocs/computer/workdocs/index.shtml, under the title "EVLA Operations System Software Requirements Specification, V1.0", by Rich Moeser, dated 11/09/2001.

9.2.4   Correlator Requirements

It has recently been decided that a separate requirements document is desirable for the correlator. Thomas Morgan, a new hire who is scheduled to assume his position on 01/07/2002, will probably do the initial draft of the formal requirements document. Dr. Morgan has the requisite experience with computing clusters, parallel processing, and very large data sets.

9.3 Design Considerations

9.3.1   General

- Use of COTS (Commercial-Off-The-Shelf) components wherever possible, including computers, network equipment, hardware and software.
- Slot-based addressing of modules, i.e., the ability to swap boards with no requirement for a user maintained table to map board addresses to slots.
- Time stamping of monitor data
- Time stamping of command & control information
- Technician access/interface to equipment at the antennas, even in the absence of the main control computers.

9.3.2   Command & Control Requirements

9.3.2.1 Hard Real-Time Deadlines

A "hard" real-time deadline is a deadline that if not met is a fatal failure, i.e. the system will not perform as needed to accomplish its goals. At this time no hard real-time deadlines have been identified for commands to the antenna and the correlator. However, it is expected that some deadlines for commands will emerge. Two approaches can be taken to satisfy the deadlines – 1) the use of time-tagged commands, sent in advance and maintained in an ordered queue either at the device or at the antenna computer, or 2) just-in-time commands, relying upon the network to deliver the commands with minimal delay. The first approach will increase software complexity. The second may or may not prove adequate to satisfy the deadlines.

9.3.3   Monitor Data Requirements

9.3.3.1 Hard Real-Time Deadlines

As with Command & Control, no hard real-time deadlines have been identified for monitor data. Unlike Command & Control, it is less likely that such deadlines will emerge. If deadlines are identified, it is likely that 1) the deadlines will not be extremely tight, i.e. on the order of 10s or 100s of milliseconds rather than microseconds, and 2) network delays will not be a significant consideration.

9.3.4   Real Time Failure Detection

9.3.5   Backup Monitor & Control System

The backup monitor and control system will monitor and control certain critical portions of the antenna in the event of a power outage. While most or all of the components of the monitor and control system that are located in the control building will be on an UPS, the M&C components in the antenna are not. As a backup, small UPS units will be used in the antenna to provide power to critical M&C functions. This system will enable the operator to monitor and control portions of the system even if power along the arms of the Wye fails. It will also periodically save to memory the contents of certain addresses, so that during a power outage an operator can determine what the values were shortly before the outage. Examples of systems that would be accessible to the backup monitor and control are the antenna control unit, monitors of the HVAC system, and the alarm system.

The backup monitor and control system is not intended to provide backup for a communication outage between the control building and the antennas. The hardware will be designed in such a manner that if a communications failure occurs, the antenna control unit will auto stow the antenna.

The backup monitor and control system is not intended to provide safety features. Separate safety procedures must be followed.

A document that gives a more complete description of the requirements for the EVLA Backup Monitor and Control System has now been completed. This document can be found at \\Filehost\evla\techdocs\moncntrl under the name "A23710N0002.pdf" for a version in portable document format, or under the name "backup_system.doc" in MS Word format." The \\Filehost… designation is compatible with Windows based systems and software, including Internet Explorer. For access under unix, the path would be /home/evla/techdocs/moncntrl.

9.3.6   Correlator Monitor & Control

During the correlator meetings of 8/27-8/28/2001 the possibility of the correlator monitor & control system using the same interface board that is now being developed for the antenna subsystems was discussed. It now appears likely that the same module interface board (MIB) will be used throughout the EVLA. This approach, if adopted, will simplify the software.

The minimum requirements for a processor on the MIB adequate to the needs of station board monitor and control are
- 8 bit data
- 64K addressing (16-bit)
- At least 1 interrupt available

During the correlator meetings of 8/27-8/28/2001 a few details concerning control of the correlator became available.

FPGA Personalities
- The issue was raised, but not answered, as to whether the personalities should reside on the boards which load them or if they should be loaded over the network. One possibility discussed was to place the personalities in local flash, with the ability to update the personalities.
- Most configuration changes will not require new personalities.

Filter taps
- Per station board there will be 38 filters, with 512 (1024 ?) taps per filter. Each tap will have an associated lookup table of 16 addresses (4 bits) with each address associated with a 12-bit coefficient.   A bit of multiplication gives a result of ~ .9Mbits (1.8Mbits ?). This figure is just the number of bits. It does not allow for unused bits that may arise from packing the needed bits into a byte or word format.

- The filter taps can be pre-computed using a filter design program.
- Successful stitching of subbands may require normalization/scaling of tap coefficients

Models
- A master station board generates the model that goes to the baseline boards.
- Baseband delay model update rate – every 50 ms (10 ms for VLBI applications?)
- Phase & rate models will require that every 50 ms a total of 38 X 4 (the number of station boards for 4 baseband pairs) 32-bit phase and rate numbers be loaded onto the station boards and transferred through the correlator via the phasemod signal. A bit of arithmetic gives a figure of ~ 12 Kbytes/second.
- The delay and phase lookup model changes if the subbands change.
- Double buffering was suggested as a technique to allow quick switching of models. Should the buffers reside on the station board and be managed by the MIB CPU ?
- There will be autocorrelations, state counts and other information to be read out from the station boards.

9.3.7 Monitor & Control of the Hybrid Array
April 2003 is the current goal for testing of the first EVLA antenna to begin, while Q4 2009 is the current goal for shutdown of the old correlator. The array will, therefore, be in a hybrid state for a period of approximately 6 years. Clearly, monitor & control of the hybrid array is a major issue, and it will require a considerable investment of man-hours. The current plan for development of a hybrid array M&C system is to grow it from initiatives already underway. Three components are critical – 1) the interim control & monitor processor (CMP) which taps the monitor and control data stream of the current VLA, 2) an upgraded, network accessible controller for the current VLA correlator, and 3) a user interface testbed for the EVLA monitor and control system. The CMP already exists. The upgraded VLA correlator controller is under development now, and the beginnings of a user interface testbed will be developed as a part of the process of gathering requirements for Operations. When combined, these elements form a basis from which a system for monitor and control of a hybrid array can be developed.

9.3.8 Storage, Retrieval, & Analysis of Historical Monitor Data
Monitor data will be stored in the data archive, and will be retrievable for the purpose of analysis. The likely storage format for the monitor data in the archive is an extension to the AIPS++ Measurement Set format.

9.4 Data Rates & Format

9.4.1 Monitor & Control
The current estimate for monitor data from the antennas is 12.5 Kbits/sec/antenna.

9.4.2 Correlator Data Rates
There are two stages of correlator output that need to be considered. One is the output from the baseline boards, and the other is the output from the yet to be designed backend processing system. The baseline boards (actually, the correlator chips) will produce data frames. For a 40 station correlator, there will be 240 baseline boards, each capable of an output rate of 100 Mbytes/sec, for a theoretical maximum aggregate output rate of 24 Gbytes/second.

The backend processing system will be responsible for concatenating the data frames produced by the baseline boards, assembling the concatenated data frames into the data streams that represent the subbands, and then performing FFTs on the data for each subband. The initial design for the backend processing system will not attempt to accept data from the baseline boards at the full data rate. Instead, the correlator will be throttled such that the output from the backend processing stage (after data frame concatenation and FFTs) will be a maximum of 25 Mbytes/second. The figure of 25 Mbytes/second is an <u>aggregate</u> data rate. I.e., it represents the correlator backend output, summed across all baseline boards and the subsequent backend processing. It is the initial data rate that will be seen by the data archive. The expected format for output from the backend processing system is the AIPS++

Measurement Set.

As the above paragraph implies, the expectation is that FFTed subbands, rather than correlator lags, will be the usual archive product. "Van Vleck" corrections are done on lags. If the possibility of performing this correction is not to be eliminated, then all of the metadata needed to perform the inverse FFT and return to lag space must be saved with the data. Nothing that cannot be reversed must be done to the data product prior to archiving.

It is expected that a burst dump mode will be implemented. For this mode, it may not be possible to do the FFTs fast enough. For such a case it might be necessary to archive the lags, and perform the FFTs on the archived data.

The design of the backend processing stage must be scalable to allow increases in the aggregate data rate as additional resources become available.

All of the above given considerations relate to the cross-correlations coming from the baseline boards. Two points not yet discussed or considered in any detail are the data flows coming from the station boards and from the phasing boards. The station board will produce wide-band autocorrelations. The phasing boards will produce outputs suitable for a VLBI recorder.

9.5 Conceptual Design
The EVLA Monitor and Control system will be implemented as a heterogeneous distributed system. Figure 1 gives a strawman diagram of the current concept. Conventional Ethernet using the TCP/IP and UDP protocols will be used as the underlying network. It is likely that some sort of middleware will be layered over those protocols for communications among distributed objects. The middleware domain will include those components of the software within the portion of the control domain indicated by the rectangular box (dashed lines) seen in the left-hand center portion of the diagram. Candidates for the middleware include CORBA, a real-time implementation of the publish-subscribe paradigm, or even some adaptation of RPC++ as developed for the GBT. It is doubtful that use of the middleware will be extended beyond the antenna computers or the operations server. For communication with operators and outside observers, Java RMI and browser-based approaches are being considered. In part, the approach chosen for development of the operator monitor and control software will determine this decision.

9.5.1   Array Control Computer

9.5.2   Antenna Computer

9.5.2.1 Location and Number of Antenna Computers
The location and number of the antenna computers are matters that are still under discussion. One possibility is that the antenna computers will be located in the antennas, and that there will be one for each antenna. Another possibility is that the antenna computers will be located in the control building, with more than one antenna supported by each antenna computer. Many factors, including cost, RFI characteristics of the antenna computers, monitor and control hardware design, and the modularity of the software functions will contribute to the final decision. At this time, plans and design are insufficiently developed to allow for a final determination.

9.5.2.2 Antenna Objects

9.5.3   Correlator Backend Processing
The strawman concept for the correlator backend processing is a Linux-based Beowulf cluster using commodity PC components. Alternatives are being explored.
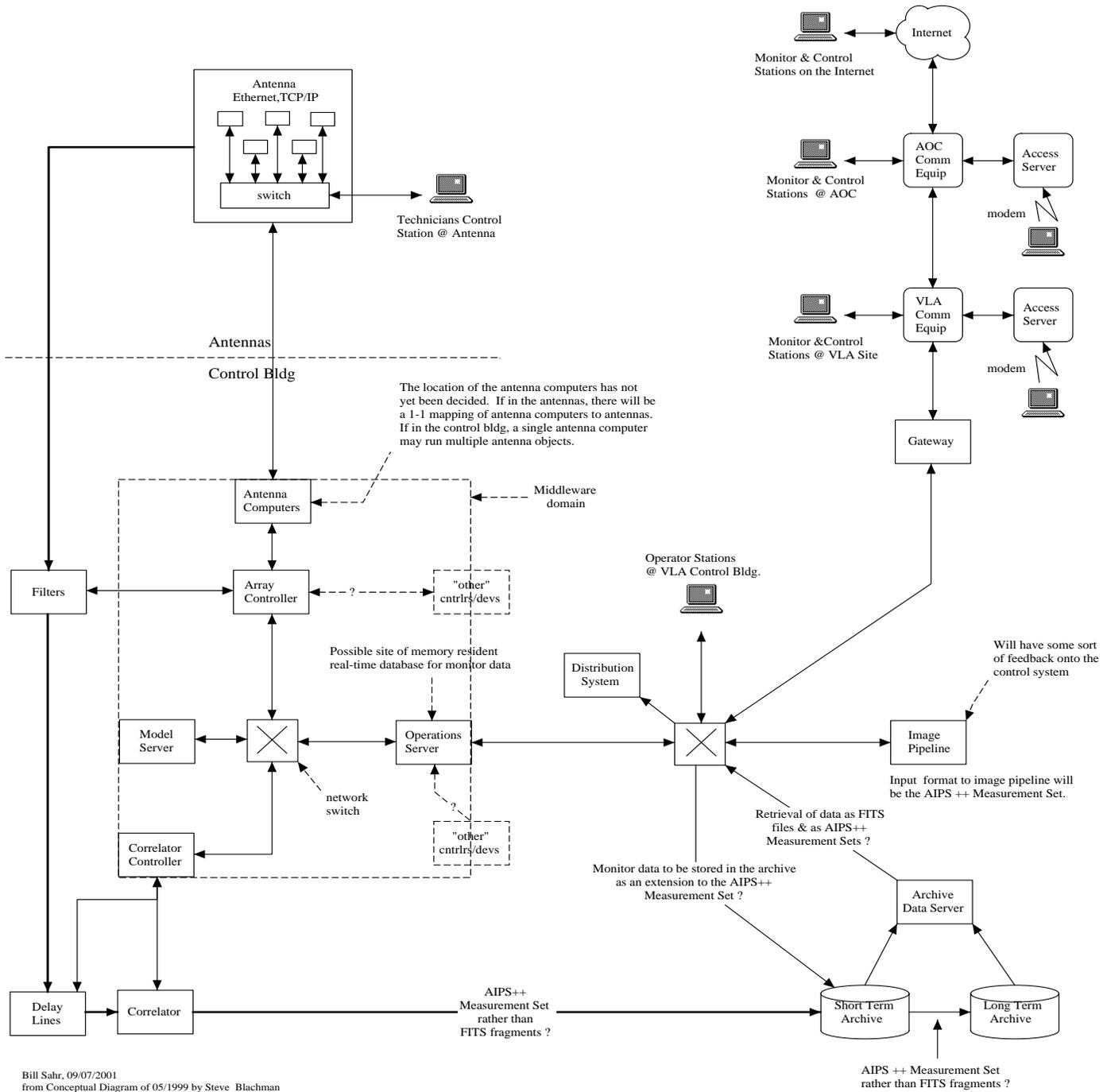
**EVLA M&C System
Strawman Diagram**

Monitor & Control
Stations on the Internet

Internet

Monitor & Control
Stations @ AOC

AOC
Comm
Equip

Access
Server

modem

Monitor &Control
Stations @ VLA Site

VLA
Comm
Equip

Access
Server

modem

Gateway

Antenna
Ethernet,TCP/IP

switch

Technicians Control
Station @ Antenna

Antennas

Control Bldg

The location of the antenna computers has not
yet been decided. If in the antennas, there will be
a 1-1 mapping of antenna computers to antennas.
If in the control bldg, a single antenna computer
may run multiple antenna objects.

Antenna
Computers

Middleware
domain

Array
Controller

?

"other"
cntrlrs/devs

Filters

Possible site of memory resident
real-time database for monitor data

Operator Stations
@ VLA Control Bldg.

Distribution
System

Will have some sort
of feedback onto the
control system

Model
Server

Operations
Server

Image
Pipeline

network
switch

?

Input format to image pipeline will
be the AIPS ++ Measurement Set.

"other"
cntrlrs/devs

Retrieval of data as FITS
files & as AIPS++
Measurement Sets ?

Correlator
Controller

Monitor data to be stored in the archive
as an extension to the AIPS++
Measurement Set ?

Archive
Data Server

Delay
Lines

Correlator

AIPS++
Measurement Set
rather than
FITS fragments ?

Short Term
Archive

Long Term
Archive

Bill Sahr, 09/07/2001
from Conceptual Diagram of 05/1999 by Steve Blachman
& from Network Flow Diagram of 04/1999 by Bill Sahr

AIPS ++ Measurement Set
rather than FITS fragments ?

Figure 1

9.5.4   Module Interface Board (MIB)

9.5.4.1 Hardware

The Module Interface Board (MIB) will communicate with the Antenna Control Computer via Ethernet.   It will be capable of communicating with the object device via both serial and parallel connections. It is planned that every module or device on the EVLA will contain a MIB. A/D and D/A capability could be included in the interface. Other planned capabilities include Reset Logic and Timing Logic. Reset Logic would include power-on reset, power perturbation reset, watchdog timing reset, and user-requested reset. Timing logic could time events with external timing signals that the board could receive.

The MIB could either be an integral part of each device, or it more probably will be a separate small board.   If it is a separate board, it will be placed very near the device that it monitors and controls.

The core of the MIB will be an embedded processor that has all of the necessary communications interfaces (Ethernet, serial, parallel) built in. This processor will implement the necessary software protocols (such as TCP/IP) in real time. There will be enough Flash Memory, probably on board the embedded processor, to store the software that runs the processor. There will also be Data Storage Memory, to store commands and monitor requests for the antenna computer. The amount of memory needed will be determined, in part, by software requirements.

It is preferred that a fiber will directly connect each MIB to the Ethernet. If this proves to be too costly, a twisted pair will be used.

It is planned to design the MIB and the racks such that the MIB will detect which slot it is plugged in to, thus eliminating the need to change the module address when the module is moved.

9.5.4.2 Software

9.5.4.2.1   Protocols

The protocol under consideration in this section is the software protocol that will be used for communication between the antenna computer and the module interface boards. The underlying transport will likely be Ethernet using TCP/IP &/or UDP. However, a protocol or set of software conventions layered on top of TCP/IP (UDP) will be required for the communication of commands to devices and for the return of monitor data from devices. Possible approaches to this issue include 1) a message-based scheme, 2) the creation of read_block & write_block primitives, and 3) the exchange of parameter blocks. A message-based scheme would probably have little or no impact on the hardware design of the MIB or devices, but would require that a parser be resident in each MIB or device. (The MIB would probably be the logical location for the parser.) The use of Read/Write primitives might have an impact on the MIB &/or device design. At this time, it is unclear how each device could be treated as an address space referenced by the read or write command given the use of a network rather than a bus for communication between devices and the antenna computer. An approach mid-way between message passing and read/write primitives is the simple exchange of parameter blocks. Parameter blocks going to a MIB/device are assumed to contained commands & setup values. Parameter blocks coming from a MIB/device are assumed to contain monitor data. A (simple ?) parser would be required to unpack parameter blocks received by a MIB, and the device or MIB would be required to format parameter blocks that are to be sent to the antenna computer. Some standard, but extensible definition of the parameter blocks would be required.

9.5.4.2.2   Real-Time Kernal &/or Software Libraries

The core of the Module Interface Board will likely be one of the new generation of microprocessor-based "communication systems on a chip" (SoC). At least one of the chips under consideration offers an embedded RTOS

kernel as an option. Current thinking is that if the chip finally chosen does offer an on-chip RTOS, that RTOS kernel will be used as a part of the MIB software.

A TCP/IP protocol stack is generally supplied with the SoC chips.

9.5.5   EVLA Monitor and Control Network

9.5.5.1 Network Characteristics

9.5.5.2 Within the Control Building

9.5.5.3 From the Control Building to the Antennas

9.5.5.4 Within an Antenna

9.5.5.5 Remote Access

9.6 VLA to EVLA Transition
The VLA to EVLA transition will be an incremental process. Figure 2 gives a diagram that illustrates one of the steps in the process – the point at which EVLA antennas are being introduced into the array, but prior to the arrival of the EVLA correlator.

9.6.1   Control of Modified VLA Antennas (EVLA Antennas)

9.6.2   Interfacing EVLA Antennas to the Current (VLA) Correlator

9.6.3   Switchover to the EVLA Correlator
The current timelines for the EVLA correlator are as follows:
- Q3 2005: A prototype 3 baseline correlator will be available at the VLA site. The test correlator will provide a bandwidth of 125 MHZ, and be able to handle at least two subbands. Autocorrelation products for the wideband signal will be available. Software for this test correlator must be available by this date. The test correlator will remain at the VLA site for use as a testbed.
- Q4 2006: Systems integration and testing of the EVLA correlator will begin in Penticton. As system integration and testing proceeds, it is possible that delivery of correlator boards to the VLA may begin, allowing installation of some functional fraction of the EVLA correlator.
- Dec 2006: Earliest likely date of systems integration and testing of a partial correlator at the VLA site.
- Q4 2007: Installation, systems integration, and testing of full correlator at VLA to begin.
- Q1 2008: Begin test observations using full EVLA correlator.
- Q1 2009: Begin full operational testing of full EVLA correlator.
- Q4 2009: EVLA correlator fully operational. Shutdown of old correlator.

During the period Q3 2005 – Q4 2009 either a test correlator or the EVLA correlator will run in parallel with the VLA correlator. The VLA correlator will be doing the science while the EVLA correlator undergoes integration and testing.

9.6.4   Coordination & Communication Between the VLA & EVLA Monitor & Control Systems
During the VLA to EVLA transition some exchange of information between the old and new control systems will be required. Software to mediate this data exchange will be written. The two systems will communicate via Ethernet.

The hybrid array after the introduction of
EVLA antennas, and before the arrival of the
EVLA correlator.

09/25/2001

Figure 2