EVLA Project Book, Chapter 8.

8 CORRELATOR

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<u>**Revision History:**</u>
2001-June-06: Initial release.
2001-July-17: Updates from M. Rupen, J. Romney comments. Add milestone table, table of "impacts and interfaces" to the rest of the system, and risk assessment table. Add clarification text to many sub-sections. Add sub-section on sub-band stitching. Upgrade the correlator layout diagram. Revise module costs to include refined pricing and circuit boards and cables for 32 stations, with racks for 40 stations.
2001-August-14: Minor revisions based on additional Rupen and Romney comments. First draft full release.
2002-February-1: Overhaul based on new Gigabit Ethernet output and backend configuration. Add more M&C S/W and H/W details. Many refinements to many sections based on design refinements over the last several months. Due to cost increases, NRC will now only pay for and install a 32-station correlator (i.e. not racks for 40 stations).

Summary

The delivered system will be a 32-station correlator, however the scaleable architecture supports up to 256 stations in 8-station increments. Each station will be capable of handling a total bandwidth of 16 GHz, arranged as 8, 2 GHz **basebands**. The correlator contains dedicated hardware (lags) for 16,384 spectral channels per baseline at the widest bandwidths and uses "**recirculation**" to provide up to 262,144 spectral channels at narrow(er)-bandwidths (or wide bandwidths with sensitivity losses). The system can flexibly use and deploy spectral channel resources within internally generated and user defined **digital sub-bands**. High performance pulsar processing capabilities are an integral part of the design. The system will be delivered with a total 1 GHz phased-VLA capability—enabling up to 4 Gbits/sec of VLBI recording bandwidth at 2 bits/sample. The architecture supports phasing all 16 GHz of bandwidth and doing so is strictly a cost issue. In this chapter, correlator performance specifications are outlined and a reasonably complete design is presented that will meet the specifications. The principal performance specifications for the correlator are shown in Table 8-1. Development milestones are shown in Table 8-2.

Table 8-1 EVLA correlator principal performance specifications.

No. of stations (antennas) (Sec. 8.2.1)	32 (architecture supports up to 256).
Max spectral channels/baseline @ max bandwidth of 2 x 8 GHz = 16 GHz (Sec. 8.2.2, 8.2.8)	16,384 (more with "wideband recirculation" and sensitivity losses).
Max spectral channels/cross-correlation with recirculation (Sec. 8.2.2, 8.2.8)	262,144
Polarization products (Sec. 8.2.3)	1, 2, or 4
No. of basebands/antenna (Sec. 8.2.4)	8 x 2 GHz each (more with narrower bandwidths)
Quantization (Sec. 8.2.10)	1, 2, 3, 4, or 8-bit initial quantization; 4 or 7-bit re-quantization after sub-band filter.
Correlator efficiency (Sec. 8.2.10)	~95% (4-bit initial quantization, 4-bit re-quantization, 5-level fringe rotation)
No. of sub-bands per baseband (Sec. 8.2.6)	16 (provision for up to 18 for "N+1" redundancy).
Sub-band bandwidth (Sec. 8.2.8)	128 MHz, 64 MHz, 32 MHz, …, 31.25 kHz (2-stage radar-mode). Each sub-band's width and position can be set independently of any other sub-band.
Sub-band tuning (Sec. 8.2.9)	Each sub-band should remain within an appropriate integer slot to minimize band-edge SNR loss. E.g. a 128 MHz sub-band should be within 1 of 16 equally spaced slots in a 2 GHz band.
Spectral dynamic range (Sec. 8.2.10)	(Initial quantization) 3-bit: ~44dB; 4-bit: ~50dB; 8-bit: ~58dB. [Test: 2 "bunches" of 4 tones/bunch, each "bunch" contained within one sub-band (128 MHz); 99% tone (interference) power; ideal samplers; dynamic range measured outside sub-bands containing interference.] With 2 tones only, results are ~10dB, ~2dB, ~4dB (respectively) worse.

Auto-correlations (Sec. 8.2.20)	Wideband (4x2 GHz pairs): 4 products of 1024 spectral channels each, SNR loss >4. Sub-band: 16,384 total spectral channels per station (widest sub-band), no SNR loss.
Pulsar processing (Sec. 8.2.14)	2 banks of 1000 time bins each/baseline. Up to 65,536 bins/baseline with software accumulation. Min. bin width: ~200 μsec (all spectral channels) ~15 μsec (64 spectral channels/sub-band/baseline). Also, pulsar gating with one timer+multi-gate generator per 2 GHz baseband.
Min. dump period (initial installed configuration) (Sec. 8.2.15)	100 milliseconds (all spectral channels). Faster with more back-end computers and/or fewer channels and/or baselines.
Max. dump period (Sec. 8.2.15)	Unlimited (with tertiary software LTA).
Maximum baseline (Sec. 8.2.16)	25,000 km with 0.5*c* FOTS transmission velocity (0.25 sec total delay buffer).
Sub-arrays (Sec. 8.2.18)	Cross-correlation: unlimited. Phased-VLA: 5 sub-arrays with "antenna grouping" granularity of 4 antennas.
Phased-VLA (Sec. 8.2.19)	8 digitally-phased sub-bands; architecture supports phasing all sub-bands. Simultaneous operation with interferometer modes using same array phase-center.
VLBI (Sec. 8.2.21)	VLBI-ready. Requires additional software and VLBI recorder-to-fiber interface.
Interference mitigation (Sec. 8.2.23)	Post-corr. Temporal/spectral excision—narrowband interference modulation robust. Possibly provision for post-correlation interference cancellation.

Table 8-2 EVLA correlator development milestones

Milestone	Approximate Date	Notes
Conceptual Design Review (CoDR)	November, 2001	Architecture/features review, specifications/design freeze.
Station, Baseline Board USER MANUALs ready	Q2, 2004	Required for S/W device driver coding.
Preliminary Design Review (PDR)	Q2, 2004	Prototype design ready, review before proto. construction.
Single (or 3?) baseline test at VLA	Q1, 2005	Requires dedicated new antennas, calibration/closure tests.
Critical design review (CDR)	Q4, 2005	Review before full production.
Begin installation at VLA (off-line)	Q3, 2006	Racks and cables: new correlator room required.
Begin full installation at VLA	Q1, 2007	Install boards. Earliest possible start of installed correlator testing.
Earliest possible "shared-risk" science	Q3, 2007	Middle of full installation and test schedule
Correlator commissioning	Q1, 2008	Full observational mode, no apparent bugs.
Project complete	Q2, 2009	Scheduled NRC support no longer required.

8.1 Introduction

The EVLA correlator design is based on the WIDAR concept (Carlson, IEE 2000) (Carlson, Memo# 001) (Carlson, Memo# 014) where wide (2 GHz) bands are sampled, split into smaller sub-bands with digital filters, and then correlated. A key anti-aliasing technique, along with stable calculable digital filter characteristics, allow the sub-bands to be seamlessly "stitched" together to yield the wideband cross-power spectrum. Using this technique it is possible to correlate data efficiently so that about an order-of-magnitude more spectral channels can be provided compared to what other time-domain parallelization techniques can yield. A design requirement for the EVLA is to provide 16,384 spectral channels per baseline in wideband modes, with more spectral channels available using "recirculation". Digital sub-banding has the additional benefit of increasing the flexibility of the correlator so that only those spectral regions of interest need use correlator resources. An 'XF' correlator has been chosen primarily to minimize the station hardware-to-baseline hardware bandwidth/cabling requirements—a significant consideration for a correlator system of this size.

8.2 Specifications

8.2.1 Number of Stations (Antennas)

The installation will include a full population of 32 stations. The architecture supports up to 256 stations in 8-station increments. Final installation may be 48 stations to support EVLA "Phase-II" requirements. Thus, supporting infrastructure should plan for a 48 station correlator. Full (16 GHz) bandwidth stations can alternatively be configured for 2 stations at 4 GHz bandwidth, or 4 stations at 1 GHz bandwidth. The architecture supports implementing this tradeoff dynamically, but requires additional front-end switching hardware not included in the delivered system to realize this potential.

8.2.2 Spectral Channel Capability

Dedicated correlator resources (lags) for 16,384 spectral channels/baseline at the widest bandwidths are available. Spectral channels can be flexibly deployed to desired sub-bands/basebands. "Recirculation" provides a maximum of 262,144 spectral channels per *cross-correlation* on up to 2 (and possibly up to 4) sampled data streams (sub-bands) that can be different in each sub-band correlator. Recirculation works by time multiplexing the acquisition of correlator lags using synthesized lag delays in a memory buffer. The amount of time multiplexing is known as the **recirculation factor**. In narrow(er)-band modes where the bandwidth reduction is the same as the recirculation factor, no sensitivity degradation is realized in the cross-power spectrum. If the recirculation factor is *greater* than the bandwidth reduction, there is a *root(recirculation factor/bandwidth reduction factor)* decrease in sensitivity. Recirculation can be used at maximum sub-band bandwidth (128 MHz) with the above indicated sensitivity reduction (referred to as **wideband recirculation**). When recirculation is used, the correlator dump time and/or minimum phase-bin time is increased since it is necessary to obtain at least one pass of all lag data in each dump to produce a proper spectrum. The time increase factor is the same as the recirculation factor.

8.2.3 Polarization

Basebands can be flexibly arranged as combinations of dual-polarization **baseband pairs** and single-polarization basebands (subject to antenna system flexibility). 1, 2, or 4 polarization products can be correlated and these are selectable on a baseband/sub-band basis.

8.2.4 Sampled Baseband Capacity

Each "station input" can handle 8, 2.048 GHz basebands sampled at 4.096 Gs/s. More sampled bands—up to 128 per station input—*could* be handled if they had less bandwidth each. This could be useful if it is desired to process more (narrower) sampled basebands (for example, to avoid regions of extreme RFI), but this is currently not an EVLA requirement. The correlator can flexibly handle various combinations and numbers of sampled bands provided sample rates are properly related. For example "native" VLA antennas with 16 GHz of bandwidth each could be correlated with "foreign" antennas with 1 GHz of total bandwidth in 8, 128 MHz chunks (or 16, 64 MHz chunks etc). For these correlations to make sense, the digital VLA sub-bands must overlap in frequency and be the same bandwidth as the foreign antennas' basebands. The overlap does not have to be exact, since the difference can be removed with the correlator's fringe rotators—with the expected reduction in cross-power bandwidth. Simultaneous with VLA-foreign antenna correlations, can be full-bandwidth VLA-VLA correlations.

8.2.5 Baseband Tuning

Basebands can be at any "sky" frequencies and any restrictions are governed entirely by antenna LO system flexibility.

8.2.6 Digital Sub-band Capability

The correlator has provision for up to 18 digital **FIR** (**Finite Impulse Response**) filters for each 2 GHz baseband input. Sixteen of these are general-purpose sub-band filters, one is for receiver switching noise diode measurements (i.e. so it can use a sub-band of the baseband with no [time-variable] interference in it for system noise temperature calibration), and one is a high-performance (many tap) "**radar-mode**" 2-stage filter. The design goal is for 1024 taps, 2-stage for the general purpose filters, and 2048 taps for the radar-mode filter. If the FIR chip can be designed for 2048 taps, then the separate radar-mode filter may be eliminated (since any filter can then perform the radar-mode function).

The *delivered* correlator will be populated with 16 **sub-band correlators** and each of these can connect to any of the 18 filter outputs. Each sub-band correlator correlates all basebands of all baselines for a particular sub-band. There is provision for up to 18 sub-band correlators. Each sub-band correlator can connect to any of the 18 FIR filter outputs (per baseband) so that "N+1" redundant capability could be achieved ("N+1" generally refers to a system's capability of losing one module with no loss of performance or data). Additionally, provision will be made so that each *sub-band* could be on a different delay-center on the sky to support multi-beaming *within* a baseband. The maximum delay-center offset from the baseband's delay center is TBD.

8.2.7 Sub-band Stitching

Adjacent sub-bands can be seamlessly "stitched" together with a maximum sensitivity loss of a factor of 2 at the **sub-band boundary**. The rate of reduction in sensitivity away from the boundary depends on the "steepness" of the filter transition band. (Typically, with a flat passband –6 dB cutoff filter and 1023 taps, the sensitivity loss is less than 20%, 1 MHz away from the sub-band boundary for a 128 MHz passband. This includes sensitivity loss effects from re-quantization and fringe rotation. With 511 taps, this mark moves to ~2 MHz.) Stitching is performed by applying the total power measurements obtained in the FIR filters *before re-quantization* and by applying calculated digital filter bandshape corrections (Carlson Memo# 001, Carlson IEE 2000). Since the filter is applied with the LO offset in place, and this is removed in the cross-power spectrum result, baseline-based filter bandshape corrections should be applied that include the effective baseline LO offset as it affects the filter amplitudes. Depending on transition-band steepness, this special consideration is normally only required if the LO offset is greater than ~1/10th of the spectral-channel bin width. Each filter's total power measurement (before re-quantization) can only be used properly if the total power gain of each filter is known. This gain is calculable, but also depends on tap-weight scaling (i.e. the scaling of floating-point tap weights to integer bits used in the filter) that should (effectively) be relative to some common reference value for all filters on every Station Board. Depending on sub-band roll-off and narrowband signal strength in the proximity of the sub-band boundary, stitching may require the use of adjacent sub-bands' spectral points and careful windowing operations. Initial quantizer statistics and re-quantizer statistics are obtained in the correlator and will be required for accurate data normalization.

8.2.8 Sub-band Bandwidth

Each of the 16 general-purpose digital FIR filters can be configured for an output bandwidth starting at 128 MHz and decreasing in powers of 2 down to about 125 kHz. The final minimum bandwidth depends on desired filter shape characteristics and whether 1 or 2-stage operation is chosen. (Two-stage filtering provides sharper transition bands and potentially narrower filters but at the expense of an additional 4-bit re-quantization step (~1.5% sensitivity loss). Also, the second stage filter cannot be placed in an "edge slot" of the first stage without significant sensitivity degradation across the resulting sub-band [Carlson, Memo# 003].) Generally, the narrower the filter, the more rounded the passband becomes and the larger the percentage of the passband taken up by the transition band. Since the filters are completely configurable, any desired characteristics can be employed within the constraints of the number of taps available. These characteristics include the flatness of the passband, the "steepness" of the transition band, and the stopband attenuation. The radar-mode filter—in 2-stage mode—has a minimum bandwidth of 31.25 kHz. *All* filters are independently configurable in bandwidth and placement within the baseband.

8.2.9 Sub-band Tuning Flexibility

Digital pass-bands can be placed anywhere within integer "sub-slots" corresponding to the sub-band (slot) width. For example, if the filter has a 1/64 bandpass, then the filter can be placed in any of the 64 evenly spaced slots in the band.

8.2.10 Sample Word Sizes and Correlator Efficiency

The initial baseband sampled word size can be any one of 8, 4, 3, 2, or 1 bits. Each sampled baseband in each antenna could have a different word size as long as the total digital transmission bandwidth does not exceed the fiber-optic transmission system bandwidth. The correlator supports 4-bit initial quantizer word sizes, but for cost reasons, the antennas will only deliver 3 bits at 2 GHz baseband bandwidths. Refer to Table 8-1 and (Carlson, Memo# 009) for spectral dynamic range estimates. The correlator supports 8-bit initial sampling, but if used, only ½ the baseband bandwidth will be available since the sample word width has doubled. (Each baseband is independently configurable in sample word width.) (N.B. because of frequency shifting, it is possible to use time-interleaved samplers since spectral by-products generated from amplitude mismatches do not show up in the correlator cross-power spectrum.)

After digital FIR filtering, the correlator re-samples the data to 4 bits. Alternatively, in high SNR, high dynamic range regions of the spectrum, the correlator can re-sample and correlate 7 bits (Carlson, Memo# 010). If 7-bit correlation is used, then ½ the spectral channels and ½ the sub-band bandwidth is available (because of internal correlator data-path routing limitations). Choice of re-sampling word size can be done on a per sub-band basis. Also, the re-sampling word size does not depend on the initial sampler word size (and vice versa).

Three-bit initial sampling and 4-bit re-sampling, along with 5-level correlator fringe rotation loss, results in a correlator efficiency of about 93% (Carlson, Memo# 011). (Four-bit sampling is ~98.5% efficient, 3-bit is ~96.5% efficient, and 5-level fringe rotation is 97.75% efficient (Carlson, Memo# 002). Eight-bit sampling is very close to 100% efficient and thus has a negligible sensitivity loss.) For spectral dynamic range refer to Table 8-1.

8.2.11 Correlator Chip

The planned correlator chip contains 2048 complex-lags, arranged as 16, 128 complex-lag correlators. Adjacent internal complex-lag correlators can be concatenated together. There is no provision for directly concatenating correlator chips. Each accumulator is a minimum of 26 bits long and is *not* truncated for high dynamic range correlation. 26-bit accumulators require a readout time of 1 millisecond—also a requirement of recirculation because of technology (memory size) and cost limitations. Lag-based, quantized-phase fringe stopping is performed with a planned 5-level fringe rotator (Carlson, 1999) (Carlson, Memo# 002). The maximum chip data rate is 256 Ms/s.

8.2.12 Digital FIR Filter Chip

The target digital filter chip is a 1024-tap, *poly-phase* FIR filter with configurable 1 or 2 stage operation (Carlson, Memo# 003). A 2048-tap chip may be possible depending on power dissipation and cost. Internal word size is sufficient to enable a reject-band attenuation of ~55 dB. The nominal configuration (when handling a 2 GHz baseband) is to use 16-phase operation. However, each filter can be independently configured for 8, 4, 2, or single-phase operation depending on input bandwidth requirements. The chip contains "pre-re-quantization" power meters and re-quantizers. These power meters are required to provide measurements for sub-band stitching (see section 8.2.7). The meters can synchronously switch their accumulated outputs into two bins for receiver noise diode calibration measurements. The re-quantizers are capable of 4 or 7-bit (Carlson, Memo# 010) re-quantization. Additionally, the filters will contain delay memory to support sub-band multi-beaming (Carlson, Memo #014). The amount of delay memory provided is TBD.

8.2.13 Radar Mode

A dedicated 2-stage filter with 1024 taps per stage (i.e. 2 FIR filter chips) is provided for each 2 GHz baseband input to the correlator (for a total of 8 per "station input"). This filter will be capable of generating a 31.25 kHz bandpass from a 2 GHz bandwidth sampled input so there is no need for additional narrowband baseband electronics in the antennas. The FIR chip will be designed so that it is capable of handling a 1/256 bandpass signal with a narrowband tone that is 50% of the total power in the bandpass. With recirculation, it will be possible to obtain better than 1 Hz spectral resolution on the 31.25 kHz, while at the same time correlating the entire 2 GHz band that the narrowband radar signal resides in. The minimum integration time on the 31.25 kHz bandwidth in this configuration is about 0.5 seconds. The radar filter outputs will be available via front-panel connectors on the Station Board (Carlson, Memo# 005). If 2048 taps are realized in the general-purpose filter chip, then a separate filter for radar-mode may be eliminated, or the function may be retained in an FPGA for future flexibility considerations.

8.2.14 Pulsar Processing

There are 2 banks of 1000 time bins each per baseline. One bank is active while the other bank is being downloaded to back-end computers. Alternatively, 1 bank of 2000 time bins can be used if correlator dead time while downloading data is acceptable. If all spectral channels are dumped, then the minimum bin width is ~200 µsec; if only 64 spectral channels/sub-band/baseline are dumped, then the time bin can be as narrow as ~15 µsec. Up to 65,536 bins/baseline can be accommodated with back-end computer software accumulation. Pulsar gating with one timer and multi-gate generator per 2 GHz baseband is available. The multi-gate generator can produce 16 pulsar gates with configurable delays relative to the timer epoch so that each sub-band can be gated "on" at different times to track different pulse arrival times at different frequencies.

8.2.15 Real-Time Data Output Performance

The real-time data output performance is governed by several factors. The correlator hardware itself has a very wideband data output pipeline so it is most likely that any performance limitations will be determined by the performance and configuration of the correlator's back-end computers. The minimum dump period for all spectral channels if the extreme, highest-performance output pipeline is used (4, 1 Gbit/sec links) is ~2.6 msec. This is a dump rate of over 12 Gvis/sec in a 40-station correlator. The delivered system will have a pipeline—*out of the Baseline Boards*—capable of dumping all spectral channels every ~11 milliseconds. With the *planned* number of back-end computers (Figure 8-3) <u>all spectral channels should be able to be dumped about every 100 milliseconds</u> (~315 Mvis/sec in a 40-station correlator). If fewer spectral channels are dumped, then shorter dump times could be obtained. The maximum correlator hardware **LTA** (**Long Term Accumulator**) integration time is signal-characteristic dependent but is about 1 second (noise, lag 0 auto-correlation). Back-end computers can integrate data for an arbitrarily long period of time.

8.2.16 Delay

The delivered correlator contains enough delay buffering for 0.25 seconds of delay and this translates into 25,000 km baselines if there is a $0.5c$ FOTS data transmission velocity over the same distance. The delay may increase depending on cost and availability of SDRAM memory chips. Also, provision may be made to increase the delay by adding memory SIMMs and/or by upgrading the memory (mezzanine) card (on all Station Boards). The delay rate that the correlator can handle is essentially unlimited. Each baseband can have its own independent delay model and hence independent delay center on the sky. Precision, fully digital ±1/32nd of a sample delay tracking on 2 GHz basebands is a feature of the WIDAR architecture (Carlson, Memo# 007). There is no associated data blanking as the correlator tracks delay. WIDAR sub-sample delay tracking eliminates the need and uncertainty associated with sampler clock phase modification. The ability to finely track delay on narrower baseband inputs by changing FIR tap coefficients may be included in the design if there is a negligible cost impact.

8.2.17 Doppler/Frequency Shift

The correlator chip contains digital complex phase-rotators with effectively no limitations in Doppler phase rate or artificial frequency shift. The rotators are driven by linear digital frequency synthesizers that can be updated every 10 msec. The fundamental limitation is the sub-band bandwidth, but it is suggested that the maximum phase rate not exceed ½ the widest sub-band so that phase does not contribute to correlator chip heating (through fast toggling of CMOS transistors). Digital filter anti-aliasing requires offsetting each antenna's Local Oscillator by a small amount. It is suggested that this be about 10 kHz, but tunable in 100 Hz steps for narrowband radar mode (Carlson, Memo# 005). There should be an adequate frequency shift between signals/antennas being correlated so that digital mixer edge effects are not apparent and so that sufficient anti-aliasing attenuation occurs. A minimum of 100 cycles of differential phase rotation within an *incoherent* integration period is recommended. If desired, frequency shifts could be dynamic so that anti-aliasing occurs even over arbitrarily long *coherent* integration times.

8.2.18 Sub-arrays

There is no limit to the number of interferometer sub-arrays. Additionally, separate sub-arrays can have mutual antennas as long as the configuration within a sub-array is consistent within the constraints of correlator data routing (and as long as the configuration software is capable of doing this!). Phased-VLA sub-arrays *may* be defined differently on different sub-bands since phasing hardware sums data independently on each sub-band. There is a maximum of 5 phased sub-arrays per sub-band, and antennas must be included in a given sub-array in "fixed" groups of 4. (The actual "fixing" of the groups of 4 is determined by correlator cable connections, and could be modified by changing connections in front of the correlator.) In this case, if an antenna is in a particular group of 4 and in a particular sub-array, it can be disabled but it can't be assigned to another sub-array.

8.2.19 Phased-VLA

The delivered system will include 8 digitally phased sub-bands, on up to 48 antennas, for a total bandwidth of 1 GHz. Exactly which sub-bands of which basebands are phased is a free parameter and is determined and fixed by rack wiring (i.e. the wiring can be changed, but not dynamically and not under program control). The architecture supports phasing all (18) sub-bands of all basebands—phasing more than the 8 planned sub-bands is strictly a cost/ configuration consideration and no additional design effort (or installed cable replacement) is required for post-installation upgrades. The EVLA will operate using VLBI-standard frequencies, and so all-digital phasing will be done. One wide-word (~8-bit) output that contains one phased sub-array's data stream before re-quantization will be provided on a front-panel connector. This allows expansion for phasing more than 48 stations with an external synchronizer and digital adder. The delivered system will not include the hardware required to feed the phased outputs back into the correlator for auto-correlation or cross-correlation processing. Also, additional hardware that is not part of the delivered system will be required to connect phased outputs to VLBI data recorders.

8.2.20 Auto-correlations and Data Statistics

Four wideband auto-correlation products will be provided for every baseband pair. Each product will have 1024 spectral channels, but with a factor of 4 or more sensitivity loss over an ideal auto-correlation. *Sub-band* auto-correlations will be performed with cross-correlator hardware and 16,384 spectral channels per antenna will be possible. Sub-band auto-correlation results may contain transition-band aliasing so it is not possible to seamlessly stitch sub-band auto-correlation spectra together (except where a "cross-auto-correlation" is performed—if the antenna LO system is sufficiently flexible). State counts of each baseband's sampled data before digital filtering and each sub-band's data after filtering will be acquired. *Currently, there are no dump-rate performance requirements for these state counts*. At least one phase-cal tone extractor will be provided per baseband. This extractor can be time-multiplexed across sub-bands and frequencies.

8.2.21 VLBI

The correlator is fundamentally a VLBI correlator and the system will be delivered with all of the "hooks" in place for VLBI. An additional tape-interface card will need to be developed before connecting to a tape machine is possible. System timing is such that it is well suited to conform to the new VSI-H standard. It will be possible to split the correlator system where one part connects to real-time VLA antennas and the other part to VLBI tape machines. Hardware required to dynamically switch inputs between real-time and tape-based hardware is not included in the delivered system.

8.2.22 Maintenance

All (semi-conductor-populated) modules and module-to-module communications will be designed for hot-swap capability. Additionally, the design is such that swapping out one module will have the minimum possible impact on other modules and their data products. The estimated MTTR is about 10 minutes (with maintenance personnel on-site). The estimated MTBF is not known, but state-of-the-art commercial devices, design, and production techniques will be employed for maximum benefit. It is not anticipated that regular semiconductor failures will occur. All hardware modules will have active (via computer) and dead-man (thermal switch) temperature monitoring and shutdown. Separate cooling fan monitors will be employed so that fan failures can be detected immediately, rather than waiting for components to heat up. It will be possible to remotely power-cycle individual modules using a power control computer that is not part of normal correlator processing (for increased reliability). While the correlator is on-line, embedded synchronization codes will allow for constant monitoring of module health and module-to-module communication integrity. When off-line (for example, when slewing antennas) it will be possible to enable internal test vectors for complete correlator system testing. The intent is that a test is treated like a normal observation, except that instead of processing data "from the sky", test vectors are processed instead. *The degree to which antenna and* *antenna transmission systems are included in this kind of testing is currently undefined.*

8.2.23 Interference Mitigation

The correlator itself does not contain any special interference nulling hardware. However, high-speed dumping (with scaleable performance back-end computing), and high spectral dynamic range provided with many-bit samples will enable post-correlation, temporal/spectral excision. The WIDAR design strongly attenuates the modulating effects of time-variable narrowband interference on normalized correlation coefficients (Carlson, Memo# 009), so post-correlation excision of burst-like interference should be quite effective. Post-correlation interference cancellation, should it be found to be effective, can easily be handled since the interference detection antenna is just another antenna to the correlator. The correlator also has the capability of processing 8-bit sampled data for high-spectral dynamic range even in the presence of overwhelmingly powerful narrowband interference.

8.2.24 System Timing

All actions in the correlator are synchronized to distributed "TIMECODEs" and a 128 MHz clock. Correlator delivery will include a "TIMECODE Generator Box" (TGB) that generates the TIMECODEs. The TGB requires an externally-provided 128 MHz clock and 1 PPS time tick synchronized to the UTC 1 PPS. To support simultaneous VLA/VLBI operation, four TIMECODEs will be distributed. One TIMECODE is the current real-time UTC for the VLA, and three TIMECODEs are programmable to any UTC epoch for VLBI. Each TIMECODE that is generated can be delayed a programmable amount (from the input reference 1 PPS, with some TBD maximum), to take into account delays through the FOTS and the large baseband delay buffer on the Station Board. One 128 MHz clock and four TIMECODEs are distributed and available to every Station Board. Station Boards, in turn, synchronize and generate timing for downstream Baseline Boards and Phasing Boards.

8.2.25 Computing and Data Highways

The correlator installation will include 3 types (or grades) of computers. The top-level monitor and control and power control computers will be high-reliability, CompactPCI rack-mount computers. Each Station, Baseline, and Phasing Board will include an embedded PC/104+ computer called a CMIB (Correlator Monitor Interface Board) installed as a mezzanine card. Finally, backend data processing computers will be COTS (Commercial Off-The-Shelf) desktop PCs arranged in N+1 redundant configurations and tied together as Beowulf clusters. Communication between the top-level monitor and control computer and the embedded computers will be via 100 Mbps Ethernet. The top-level computer will also have 100 Mbps connections to the backend computers. Lag data from Baseline Boards will be transmitted to the backend computers using 1 Gbps Ethernet through Gigabit Ethernet switches as first proposed by Bruce Rowen (Rowen, 2001). The correlator's network topology is shown in Figure 8-3. A design goal is to use Linux in all of these computers, but further evaluation is required to determine if real-time Linux is suitable for the CMIB RTOS (Real-Time Operating System). Further straw-man details of monitor and control and backend processing can be found in (Carlson, Memo# 015).

8.2.26 Environment

The correlator will be designed for a "benign office environment" with an ambient temperature of ~25^{o}C at the altitude of the VLA. Board and rack design will be such that its operating temperature range will be 0^{o}C to +35^{o}C. However, for reliability the ambient temperature should be kept at about +20^{o}C. The correlator is expected to require ~120 kW of power. Correlator delivery will include installation and configuration of the system power supply (by the manufacturer). The system power supply will be a 48 VDC plant with battery backup as used in central-office telephony systems. This plant should have very high reliability, be very efficient (compared to an AC-AC UPS), and will be on-line serviceable and hot-swappable. This plant requires three-phase 208 VAC, has a power factor of 0.9, is approximately 90% efficient, and meets FCC Part 15 Class 'A' EMI specifications. Overload protection and remote monitoring and control will be as supplied by the manufacturer. This power plant could have a back-up time of ~1 hr 15 min at full load (although the requirement is for only 15 minutes of backup). It may also be necessary to install one or more AC-AC UPSs for supplying power to correlator COTS PCs and CompactPCI computers. These additional UPSs will be included in the installation. NRAO will be responsible for providing the (sufficiently clean) office space, ventilation, cooling, and mains power service for the correlator. The correlator (with enough room for 48 stations and up to 16 phased sub-bands) will require a floor surface approximately 45 ft x 45 ft (~2000 ft^2—refer to Figure 8-4). This is based on 12 station racks each with a footprint of 2.5 x 3 ft, and 24 baseline racks each with a footprint of 2.5 x 6 ft. It is expected that racks are to be at most 7 ft high.

8.3 Correlator Architecture

8.3.1 System Overview

A simplified block-diagram of key correlator systems is shown in Figure 8-1

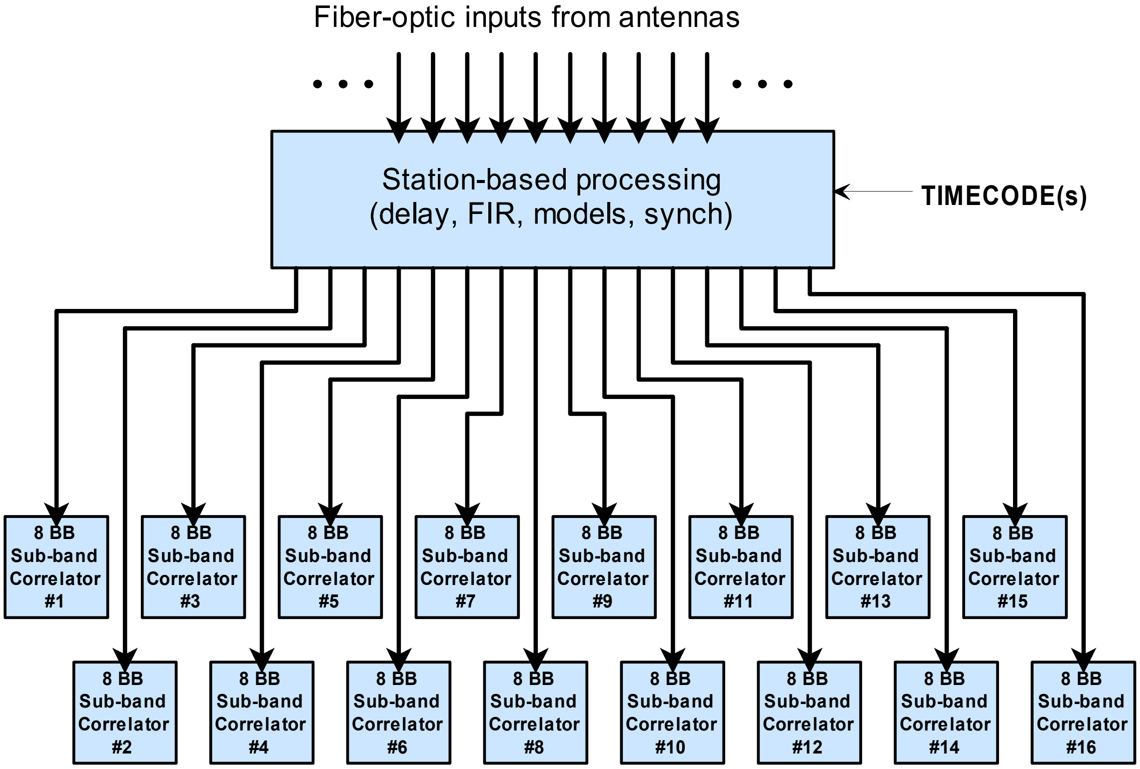

Figure 8-1 Simplified correlator system block diagram.

Sampled data arrive from the antennas into the station-based processing subsystem where coarse delay compensation occurs, the data are digitally FIR-filtered into sub-bands, and then data along with models and synchronization information are transmitted to the 16 downstream sub-band correlators. *Each sub-band correlator correlates (or, is capable of correlating) one sub-band from all 8 basebands on all baselines*. *Each* sub-band can be any width and placement (within slot constraints mentioned previously) within its associated baseband. The width and placement of a sub-band is *entirely* governed by the FIR filter tap weights and chosen decimation factor. In a particular correlator chip (bearing in mind that each correlator chip in a row or column is fed the same X or Y data), it is perfectly acceptable to be correlating one or more sub-bands with different bandwidths and placement within their respective basebands. For example, within a correlator chip, one correlation could be slot 1 of 16 slots within baseband 1 with a 128 MHz bandwidth, while another correlation could be using recirculation on slot 63 of 128 slots within baseband 5 with a 16 MHz bandwidth. Switching circuitry on the output of the station-based processing block effectively allows any sub-band FIR filter output to be routed to any sub-band correlator. Thus, redundant correlations across sub-band correlators could be performed for test or on-line redundancy purposes.

8.3.2 System Module Connectivity

Figure 8-2 is a diagram showing the interconnectivity of all correlator modules. Also indicated in the diagram is the quantity for each module for a 40-station correlator configuration. A brief description is provided here and more details for each module can be found in (Carlson, Memo# 014).

Data from the antennas arrive via fiber-optic links where they are wavelength demodulated before being presented to mezzanine cards on the Station Boards. On these cards, the fiber-optic signal is demodulated into electrical signals for use by Station Board electronics. Each “station input” in the correlator consists of four Station Boards. Each Station Board handles two, 2 GHz sampled basebands—also referred to as a baseband pair. The Station Board delay mezzanine card compensates for wavefront geometrical delay as well as delay through the fiber-optic system. Data then go to the sub-band FIR filter banks, the output of which are 16 (up to 18) sampled data streams no longer in de-multiplexed parallel form as they were going into the filters. These data go through crossbar switches before going to the Sub-band Distributor backplane, which passively re-arranges data so that there are 16 (with provision for 18) sub-band cable outputs. Each sub-band cable output contains data, timing, model, and synchronization information for one sub-band of all 8 basebands from one station. All real-time information required for the down-stream Baseline Boards (recirculation, phase-binning, dumping, phase models, delay models) is generated on the Station Boards and flows with the data on each sub-band cable. Data get distributed and fanned-out to all of the Baseline Boards and the Phasing Boards via Station Data Fanout Boards and data routing backplanes.

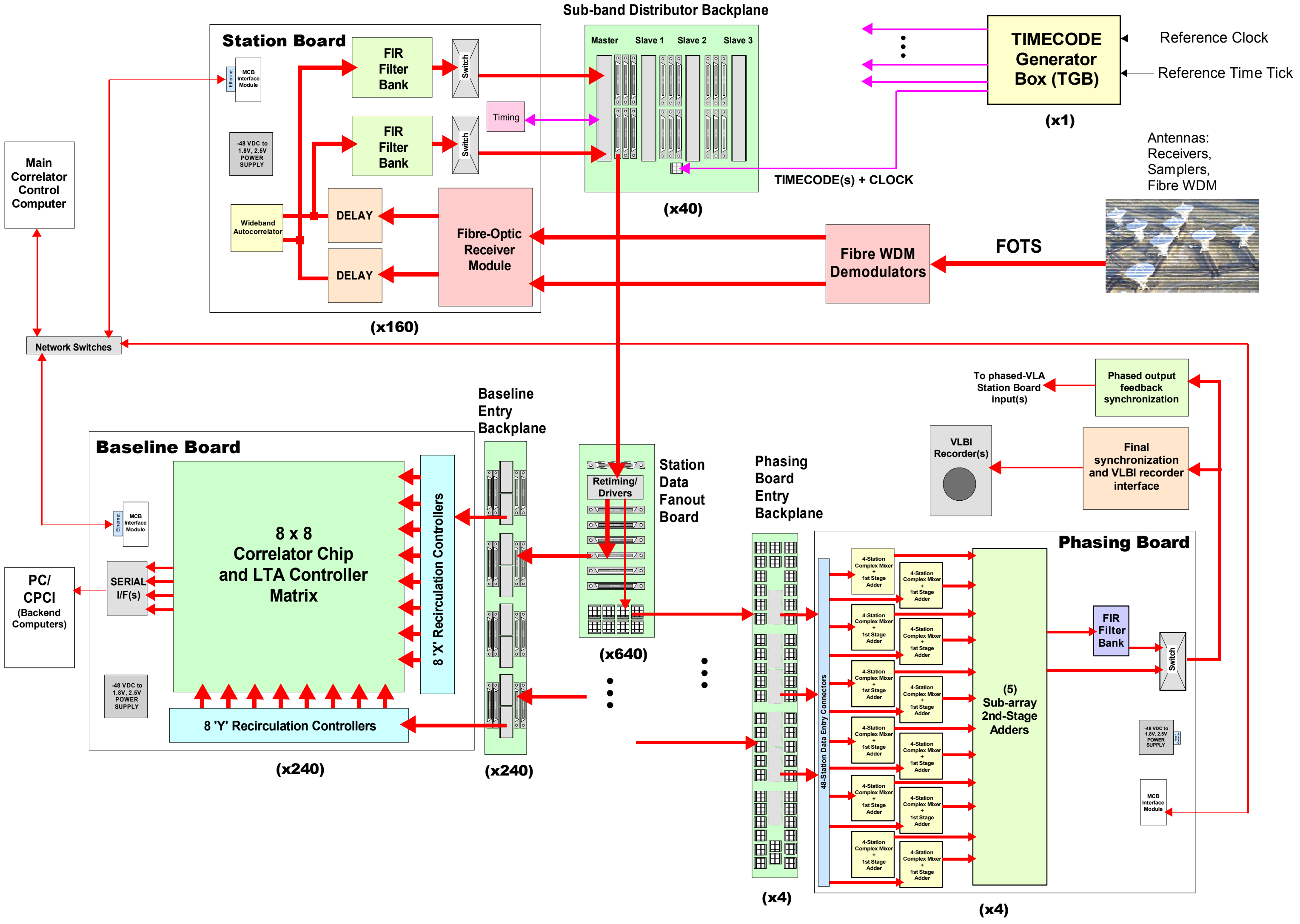

Figure 8-2 Correlator module connectivity diagram.

On the Baseline Board, there are 8 ‘X-station’ and 8 ‘Y-station’ inputs—each input being data from one sub-band cable from one station. The input data are resynchronized and formatted for transmission to a row or column of correlator chips by the 8 ‘X’ and 8 ‘Y’ Recirculation Controllers. The correlator chips correlate data and respond to commands coming from the Recirculation Controllers. After integration, and on command from Recirculation Controllers, the data are read out of the correlator chip by its own dedicated LTA (Long-Term Accumulator)

Controller and saved in 256 Mbit LTA SDRAM. Although having one LTA Controller for each correlator chip seems extreme, it offers significant performance advantages and is cost-effective since a relatively small (and inexpensive) FPGA can be used. When enabled by an on-board scheduler, LTA data are transmitted via Gigabit Ethernet (and a switch—not shown—see Figure 8-3) to a backend computer (PC) for further processing. The data on the Baseline Board are not handled by a microprocessor so there are virtually no bottlenecks to data flow off the board.

On the Phasing Board, data for one sub-band pair from all antennas enters via the Phasing Board Entry Backplane. These are the same data that goes to the Baseline Boards only they are rearranged so that two sampled data streams (one sub-band pair of one baseband pair) and timing/synchronization is contained on one cable. Thus, each Phasing Board sums antennas for one sub-band pair of one baseband pair. Data are summed in two stages to keep on-board data path widths within device capabilities. In the first-stage, data from antennas are summed in groups of 4—hence the "group of 4" restriction mentioned in the specifications section. Each antenna's data are complex mixed before complex addition to remove the Doppler shift and the frequency shift required by the WIDAR technique. There are 5, second-stage adders—each one being the output of one sub-array. After second-stage addition, the complex data are combined using the Hilbert transform FIR, the second part of the digital single-sideband mixer. Details and test results are found in (Carlson, Memo# 008). The final summed output is available in normal sub-band "wide" mode, or it can be filtered with on-board FIRs to generate more, smaller, sub-bands for VLBI recording.

8.3.3 System Network Topology

The correlator system is designed for scaleable performance: there are virtually no bottlenecks to output data flow and the system's real-time data handling performance is largely governed by back-end COTS computing performance. The proposed network configuration for the correlator is shown in Figure 8-3. (All network connections are isolated with either fiber or transformer-coupled/isolated Ethernet. Isolation is required to minimize ground-loop noise between sub-systems operating on different UPSs.) In the figure the MCCC is the Main Correlator Control Computer and the CPCC is the Correlator Power Control Computer. Each Station, Baseline, and Phasing Board has an embedded CMIB. Finally, Baseline Board data are transmitted to backend computers on Gigabit Ethernet through Gigabit Ethernet switches. Switch connections are such that all data required for a particular FFT arrives at one computer and that processing can be dynamically load-shared across computers. This eliminates the need for an additional wideband network fabric that would be required if a distributed FFT is performed. More straw-man details of network topology and backend processing are in (Rowen, 2001) and (Carlson, Memo# 015).

8.3.4 System Installation

The correlator will be a large system. For cost and performance reasons, it is desirable to minimize the correlator installation footprint. A smaller footprint requires shorter and less expensive cables and results in better signal performance—particularly at the clock and data rates under consideration. A preliminary floor-plan for a 48-station correlator installation is shown in Figure 8-4.

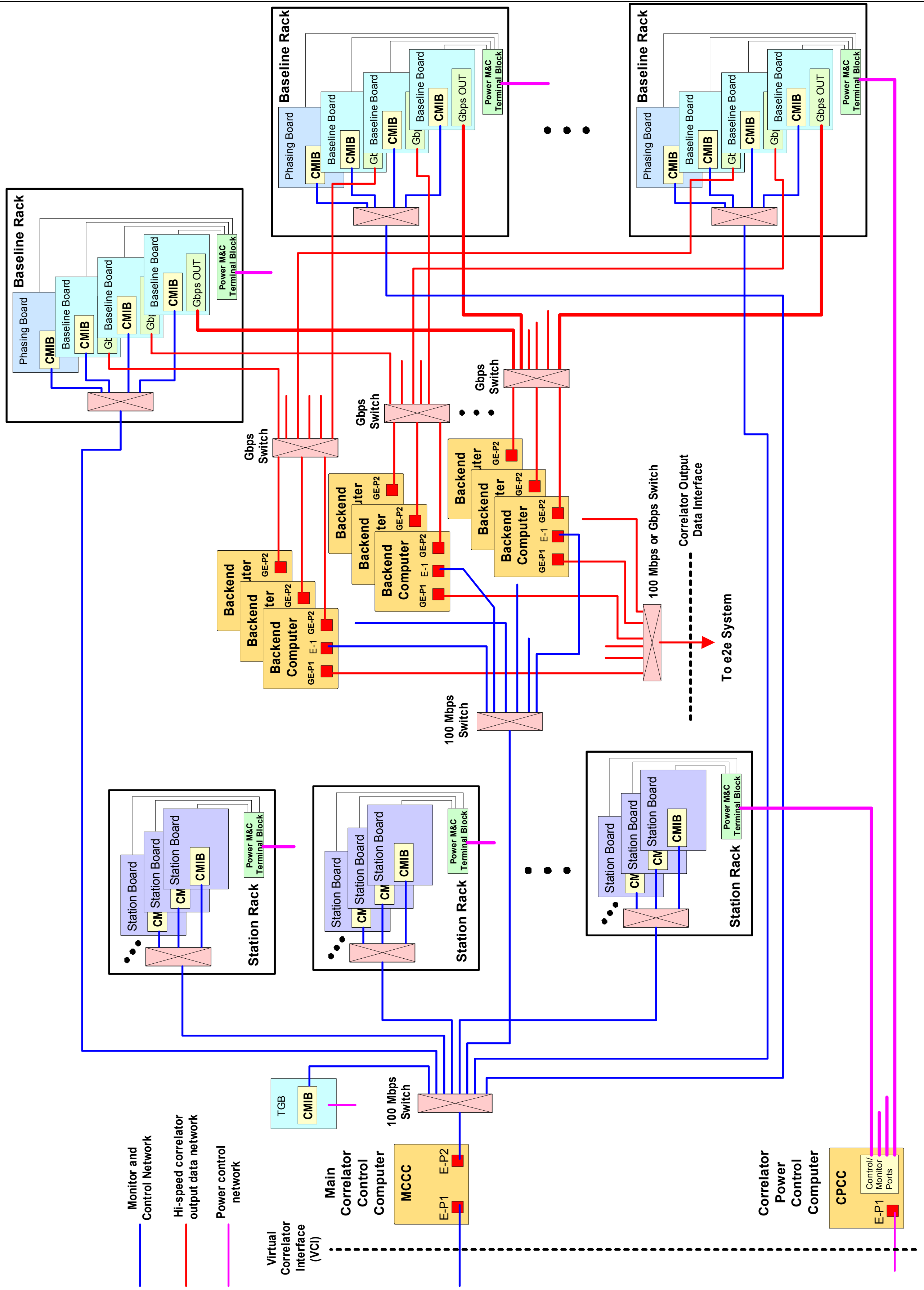

Figure 8-3 Possible correlator computing/network topology.

In this plan, 11 m cables are required for data distribution from the Sub-band Distributor Backplanes (in the Station Racks) to the Station Data Fanout Boards (in the Baseline Racks). In a 48-station correlator, each sub-band correlator uses 21 Baseline Boards, requiring 1 ½ racks (3 crates/sub-racks). Thus, 3 racks contain 2 sub-band correlators. Signal arrival time mismatch at the Baseline Boards will be partially compensated for by similar cable lengths and finally compensated for on the Baseline Boards in the Recirculation Controllers and/or the correlator chip. Station racks need only front and rear access, but because of intra-cabinet cabling density, it is estimated that Baseline Racks need 360° access. Each Station Rack holds 16 boards (4 station inputs) and each Baseline Rack holds 16 Baseline Boards with unused slots available for Phasing Boards. Provided there is floor space, more Phasing Boards and racks can easily be added at a later date without requiring replacement of existing cabling. Each rack is about 7 feet high. The fronts of the racks are shown with bold lines in the figure. All high-speed cabling is within the racks and under the (raised) floor. Any other cabling (e.g. network cables shown in Figure 8-3), will be run in cable trays hanging from the ceiling. The MCCC, CPCC, and backend computers can be located in the room, or located in a completely separate room.

Figure 8-4 Preliminary 48-station correlator system floor-plan.

8.4 Deliverables

Table 8-3 summarizes the modules that will be developed and delivered by the NRC. This table includes items and costs for a 32-station correlator. Costs are estimated and do not include NRE (Non-Recurring Engineering) costs or technician test, burn-in, and handling costs. Some spares (~5%) are included. All figures are in 2001 U.S. dollars.

Table 8-3 Cost estimates for NRC-supplied correlator deliverables

Qty	Item/Description	Cost (ea) USD
135	Station Board	$9,930
34	Sub-band Distributor Backplane	$360
538	Station Data Fanout Board	$522
168	Baseline Entry Backplane	$220
168	Baseline Board	$16,027
5	Phasing Board Entry Backplane	$354
5	Phasing Board	$9506
2	TIMECODE Generator Box	$2117
1	High-speed 80-wire cabling for 32 stations	$577,000
1	Sub-racks and racks for 32-station correlator	$300,000
64	COTS computers (MCCC, CPCC, backend, switches, copper-fiber converters)	$582,120
1	48VDC, 2000A plant including batteries, shipping, installation, cables. Can be field-upgraded to 3000A.	$183,238
1	AC-AC UPS for back-end COTS PCs (est. 30 kVA)	$30,000
n/a	Correlator software	

The total installed system cost is about $6.1 million. The total *estimated cost* of the correlator including NRE, labour, and all of the above deliverables is $12 million dollars, *not* including a contingency of $1.9 million.

Table 8-4 summarizes additional modules and components that NRC does not develop or supply as part of the correlator installation. Not all modules are required, depending on desired configuration (VLBI correlation, phased-VLA correlation etc). Quantities are for a 32-station correlator. Higher-level on-line, interface, data processing, and VLBI control software is not included in this table. Quantities in **boldface** are considered essential for the system to perform its basic functions.

Table 8-4 Additional (NRAO-supplied) correlator deliverables.

Qty	Item/Description
135	Dual-input (2 x 2 GHz bandwidth) fiber-optic receiver mezzanine card to plug into the Station Board. C/w test vector receivers and test vector transmitters (to Station Board receivers). Each baseband output is 4 Gs/s arranged as 16 demultiplexed streams, 4 (or 3) bits/stream, @ 250/256 Mbps each.
1+	Final Phasing Board output synchronization and VLBI recorder interface. This includes a fiber output to feed back into the correlator (i.e. into the fiber receiver mezzanine card).
12+	VLBI playback interface: fiber output to go to the fiber receiver mezzanine card on the Station Board.

8.5 Interfaces and Impacts on Other Systems

Table 8-5 summarizes correlator interfaces and/or associations to the external world, and a description of possible impacts on other parts of the system.

Table 8-5 Table of correlator interfaces and potential impacts on other systems.

Interface/Location	Description	Impacts
Fibre-optic receiver module interface (Station Board). Sec. 8.2.4, 8.2.10	Interface to fibre-optic reciever mezzanine card. Each interface is 16, 256 Ms/s streams at 4 bits per sample per stream. There are 2 interfaces per Station Board.	BERT transmitter in the antenna's fiber-optic transmitter and in the (correlator) receiver module allows transmission system and interface testing. Supports 1, 2, 3, 4, or 8-bit sampling with flexible baseband widths. 8-bit sampling reduces the sampled bandwidth by a factor of 2.
Coarse Delay Module (Station Board). Sec. 8.2.16	This modules inserts wavefront delay in the station data path. The depth of this delay determines the maximum baseline.	Design will be for 25,000 km baselines + 0.5*c* data transmission velocity. <u>Better estimates of transmission velocity should be obtained</u>. Can be increased with new module, or possibly, more or new SDRAM SIMMs.
Correlator clock/timing interface (TIMECODE) Sec. 8.2.24	Reference clock (128 MHz), and reference time tick (1 PPS). Required for correlator TIMECODE generation.	Requires clock and time epoch (1 PPS) from array maser/timing master.
LO system (antenna). Sec. 8.2.6, 8.2.7, 8.2.12, 8.2.13, 8.2.17	LO offsets for anti-aliasing, sub-sample delay tracking, and narrowband harmonic/inter-modulation product reduction.	Requires 100 Hz LO tuning resolution for LO offset capability. An antenna can have the same LO offset in every one of its basebands. Optionally, different LO offsets in the same antenna allow sub-band "cross auto-correlation". System control should ensure that minimum acceptable net phase rotation rate is ensured on all baselines. Time-variant LO offsets could be employed for more aliasing attenuation on long *coherent* integration times. LO offsets could be turned off, and correlator would lose sub-sample delay tracking and anti-aliasing capability.
Noise diode switching (antenna). Sec. 8.2.6	Noise diode switching in the antenna receivers for system noise calibrations. A reference FIR filter will synchronously switch with the noise diode to acquire power data with the diode on and with the diode off.	Switching/binning in the correlator will be synchronized to switching in the antenna using a timer and apriori knowledge of the switching period and phase. It is not defined what this switching rate will be.
VLBI recorder interface (Phasing Board) and output for feedback into the Station Board. Sec. 8.2.19	Interface box to synchronize outputs of multiple Phasing Boards for transmission to VLBI recorder, and feedback into the correlator.	NRAO-developed. Rack space and physical location is currently undefined.
Internal correlator monitor and control bus (Station, Baseline, Phasing Boards). Sec. 8.3.2, 8.3.3	Interface to Station, Baseline, and Phasing boards. Will use 100 Mbps Ethernet. Will use embedded PC/104+ "CMIB".	Station Board data products output from this interface (auto-corr, sub-band power, quantizer statistics, phase-cal) internally, but through the backend computers externally.
Internal data output interface (Baseline Board). Sec. 8.2.25, 8.3.2	Baseline Board data output pipeline on Gigabit Ethernet.	Wideband output with delivered output data rate of ~100 Mbytes/sec from each Baseline Board. Potential for upgrade to 400 Mbytes/sec (4 x Gigabit Ethernet) output capacity from each Baseline Board.
Correlator system monitor and control interface. Sec. 8.3.3	Network interface to higher-level control computers. 100 Mbps Ethernet. Refer to (Carlson, Memo# 015)	Virtual correlator interface to allow high-level configuration, control, and monitoring.
Correlator system data output interface. Sec. 8.3.3	Straw-man concept is Gigabit or 100 Mbps network connections. See Figure 8-3.	In the straw-man concept, correlator backend computers perform FFTs, excise interference, and integrate. Refer to (Carlson, Memo# 015).

8.6 Risk Assessment

Table 8-6 Areas of risk, and planned risk mitigation strategies in descending order of importance.

Risk	Risk Mitigation
Personnel	One engineer has been hired. Currently taking steps to acquire experienced senior engineer and one more design engineer. Local FPGA design consultants will be used if necessary.
Speed (256 MHz clock rates)	Mentor Graphics high-performance development tools will be used. These are budgeted to cost ~$360k. System signaling and synchronization designed to accommodate skewed clocks and data. If necessary, the clock rate can be reduced to 128 MHz, but new cabling, signaling, and sub-rack layout required to minimize cost impact.
Correlator chip	2048 complex lags. The current plan is to prototype with a scaled down (fewer lags) FPGA, and then once the design is solidly tested (including testing on the sky), to use an external supplier for an FPGA to gate-array conversion. Current estimates indicate that use of a 0.18 um CMOS gate array should be within our power budget of ~2 W. This approach minimizes our risk by thoroughly testing the design before committing to final silicon. It also pushes back our technology freeze date so that we can take advantage of technology improvements. If absolutely necessary, de-scope to smaller chip—resulting in fewer spectral channels—and/or use 3-level fringe rotation.
FIR filter	The current plan is prototype a scaled down version in an FPGA and then do a gate array conversion to a 0.18 um CMOS gate array. Power estimates indicate that it may be possible to implement a 2048-tap FIR using this approach.
Personnel turn-over	Define and enforce documentation standards to minimize single person dependencies.
Disruptive ground loop noise	Use differential signaling from rack-to-rack. Use common-mode noise filters on cables, and use large, low-impedance shunts between racks.
Major supplier insolvent	The major device/component suppliers in this project are: Xilinx (FPGAs) and IDT/Motorola (memory). The most severe blow would be if Xilinx became insolvent. Xilinx is a "fab-less" semi-conductor company with multiple foundaries in geologically diverse locations. Cabling is no longer thought to be a risk area, since at least two suppliers have now been identified.

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