EVLA Project Book, Chapter 7

FIBER OPTICS SYTEM

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Summary

7.1 Introduction

The EVLA makes extensive use of fiber optic technologies for the IF Data Transmission, the Local Oscillator and Reference distribution, and all Monitor/Control functions. This allows for the use of commercially developed technologies and components, leveraging on the tremendous investment made in these technologies by the computer and telecommunications industries. Each of these systems will be discussed separately.

7.2 The Fiber System

A set of fibers will be run to each pad location throughout the EVLA. The cables are run in a star configuration with all fibers originating at each antenna pad, and fiber trunks terminating at the termination panel in the control building. This termination panel is a commercial product and is designed to handle 1500 fibers.

The fiber system consists of 1) standard single-mode fiber, 2) 12 channels WDM on a single fiber, 3) an EDFA optical pre-amplifier, and 4) power margin of over 6 dB.

The EVLA uses standard single-mode fiber. The fiber has a typical attenuation of 0.3 dB/km. Maximum chromatic dispersion is 17.4 ps/nm km. Maximum pulse spread to pad A9 is 38.3 ps. Mode Field Diameter is 82 μm. The fiber meets or exceeds ITU-T recommendation G.652, TIA-EIA-492CAAA, IEC Publication 60793-2, and Bellcore GR-20-COR requirements.

Table 7.2.1 illustrates the power budget for the pre-amplified system. This configuration includes the gain from an EDFA and uses the ideal receiver sensitivity of –22.5 dBm to maintain the required bit error rate of 10^{-9}. The power margin for this system, with only 10 dB of gain, is 6 dB. This power margin provides headroom for system aging.

Table 7.2.1 EVLA IF Power Budget (Pre-Amplified System)

Elements	No. Units	Loss/Unit (dB)	Loss/Element(dB)
IF Rack to Vertex Room Bulkhead			
Launch Power			0.00
16ch WDM MUX	1	-6.00	-6.00
Connector	3	-0.30	-0.90
Fiber (km)	0.004	-0.30	0.00
Vertex Room Bulkhead to Antenna Pad		$P_{vtx\ bulkhead}$ = -6.90	
Connector	1	-0.30	-0.30
Fiber (km)	0.02	-0.30	-0.01
Farthest Antenna Pad to CB Termination Panel		$P_{last\ antenna\ pad}$ = -7.21	
MIL Connector	2	-0.50	-1.00
Connector	1	-0.30	-0.30
Fiber (km)	22	-0.30	-6.60
Splice	2	-0.10	-0.20
Bends	18	-0.10	-1.80
CB Termination Panel to Patch Panel		$P_{termination\ panel}$ = -17.11	
Connector	3	-0.30	-0.90
Fiber (km)	0.02	-0.30	-0.01
EDFA Gain	1		10.00
Correlator Patch Panel to Correlator Receiver		$P_{IF\ patch\ panel}$ = -8.01	
Fiber (km)	0.004	-0.30	0.00
Connector	3	-0.30	-0.90
16ch WDM DMUX	1	-6.50	-6.50
Received Power			-15.41
Aggregate Noise (N)			1.00
Receiver Sensitivity			-22.50
Loss Margin			6.09

7.3 Digital IF Data Transmission System

A Digital Transmission System (DTS) is employed within the EVLA to transmit the digitized IF signals from the antennas to the Central Electronics Building. A sustained data rate of 96 Gbits (120 Gbits formatted) is transmitted. Each polarization uses a parallel interface of three synchronized single bit high-speed serial optical fiber transmission channels. The single channel signaling protocol defines the format of the three parallel fibers. The design of the EVLA Digital IF transmission system is largely based on the system developed for the Atacama Large Millimeter Array (ALMA) project.

7.3.1 Specifications and Requirements

Figure 1 shows a conceptual diagram for the signal data paths from the receivers to the fiber output at each antenna. The front-end can provide simultaneous reception of two

orthogonally polarized signals. Each receiver provides an instantaneous bandwidth of up to 8 GHz which is partitioned into four, 2 GHz wide sub-bands by the IF system. Each sub-band is harmonically sampled at 4 GHz and quantized to 3 bits. This produces a data stream of 12 Gbits/s per sub-band. The digitizers incorporate a de-multiplexer which reduces the clocking rate while increasing the number of bits, a 48-bit wide parallel output word clocked at a 250 MHz rate. With two digitizers paired together, the parallel word is 96 bits wide, clocked at 250 MHz. This corresponds to a 24 Gbits/s data rate per polarization. Each antenna can provide four polarizations producing a total data transmission rate of 96 Gbits/s. and 120 Gbits/s formatted.

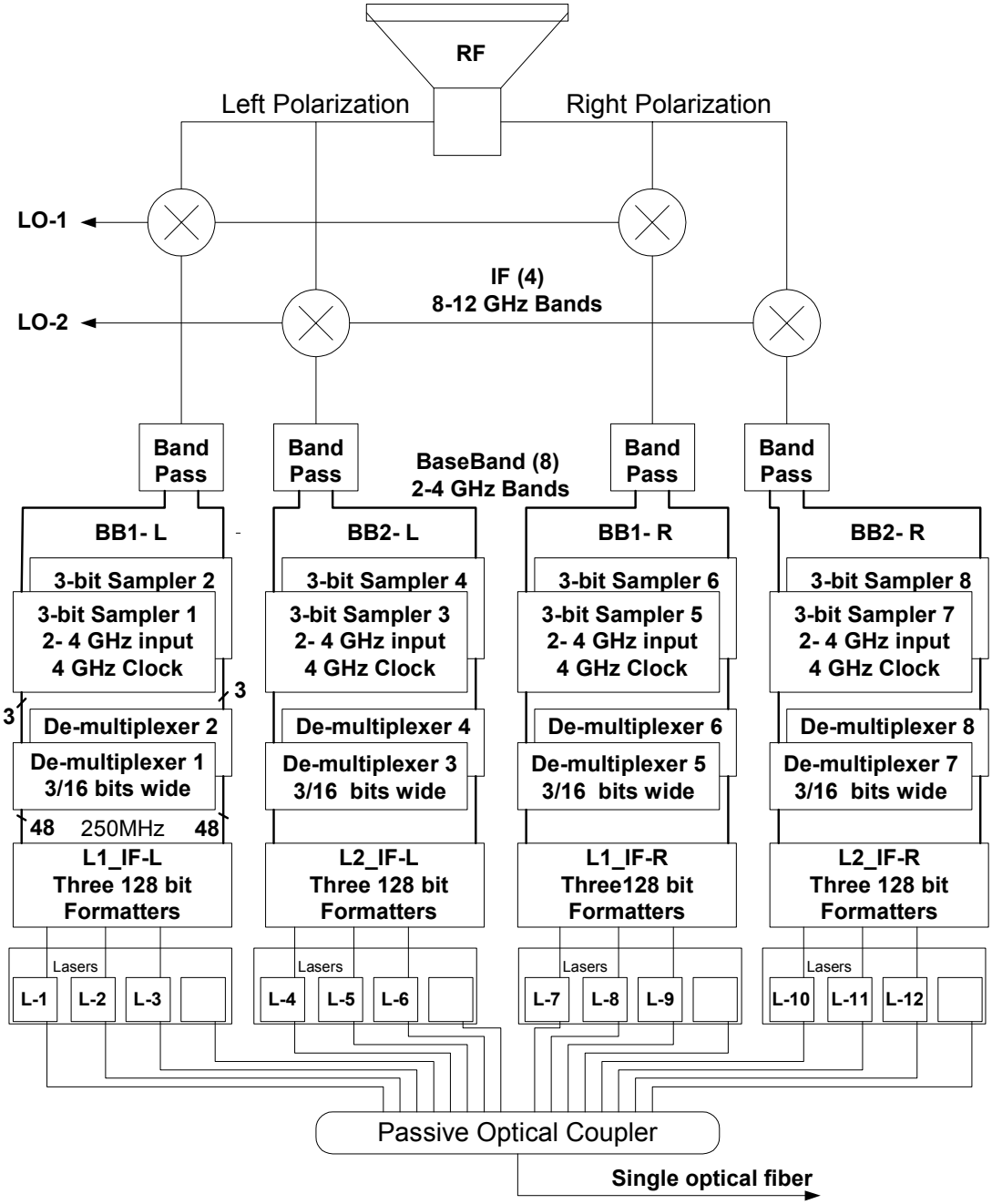

Figure _. Conceptual Diagram of the Signal Data Path

At the central site, the DTS supplies a 96-bit wide word clocked at 250 MHz to the correlator. Each bit position in the received word corresponds exactly to an identical position in the transmitted word.

The serial protocol requirements for the DTS were derived from the end-of-life bit error rate required to support good astronomy. Typically the minimum bit error rate for good astronomy is 10^{-4} divided by the number of bits in the sync word. The EVLA sync word

is 10 bits long, thus the minimum bit error rate for good science is about 10^{-5}. Since there are twelve serial optical channels each channel also provides contains a Metaframe index bit and a sequence count. These bit provide the required multi-channel synchronization to recreate the original data in the correct sequence.

The measurable system parameters are shown in Table 1.

Table 1. Measurable IF Transmission System Parameters

a.	Bit Rate:	10 Gbits/second per channel
b.	Number WDM Channels:	12 or 16 channels
c.	Channel Spacing:	200 GHz spacing
d.	Channel Wavelengths:	C Band, 1560.61 nm to 1536.61 nm
e.	Bit Error Rate:	Beginning of Life, 10^{-9}; End of life, 10^{-6}
f.	Digital SNR (Q):	Beginning of Life, 6; End of life, 4.7
g.	Maximum, fiber length	21.6 km
h.	Minimum fiber Length	0.625 km
i.	Operation Temperature	-12C to 35C

7.3.2 Transmission Protocol

The digital protocol is based upon a 160-bit frame structure and line coding exploiting scrambling techniques. The protocol is described in detail in the EVLA Memorandum #33 - "Digital Transmission System Signaling Protocol" Version 2, November 2001.

The frame is composed of a divided 10-bit sync word, 1 meta-frame index bit, a 5-bit sequence count, a 1PPS bit, a 1 pulse per 10 second bit, a data valid bit, 5 non dedicated bits, a 8-bit checksum**.** The first 4 payload bits are carried in locations 12 through 19 with the remaining 124 contiguous bits beginning with the bit location 20.

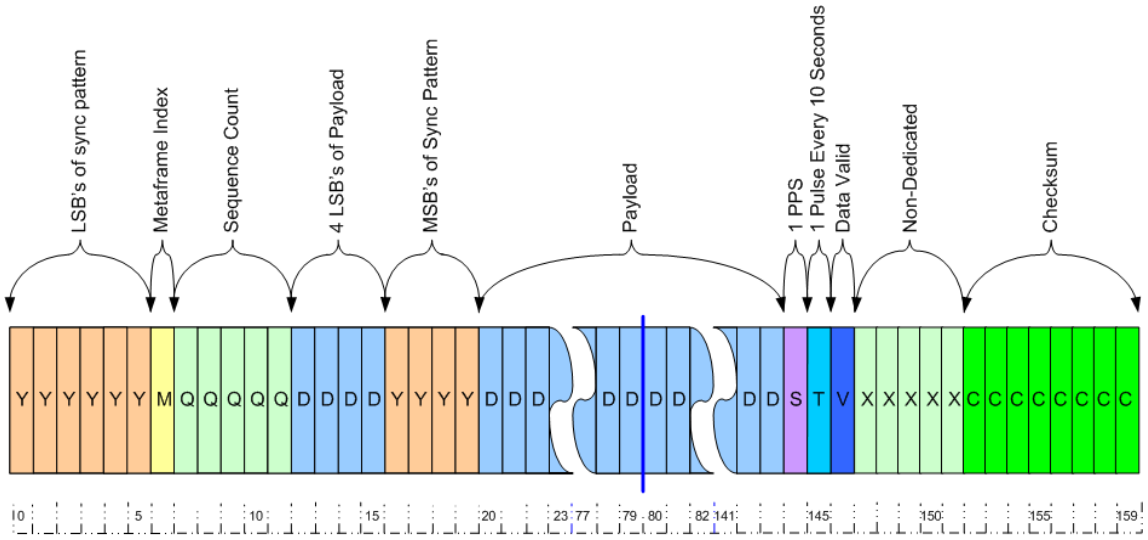

Figure __The Data Frame

Channel coding is used to modify each 10 Gbits/second optical channel to facilitate proper reception. Channel coding provides better timing information and minimizes low frequency content. The EVLA uses a channel coding technique that produces almost an equal number of ones and zeros per frame. This scrambling not only reduces systematic jitter but also minimizes the low frequency content.

7.3.3 Transmitter (Antenna) Hardware Design

The formatter uses the Xilinx Virtex E/2 series Field Programmable Gate Array and a 10-Gbits/s-16:1 multiplexer IC made by several manufacturers for SONET OC192 communications. Integrated Laser/Optical Modulator devices are used to transmit the 10 Gbits/s signal onto the 12 fibers. The twelve fibers from the transmitters in each antenna are combined onto a single fiber using a passive 12:1 fiber multiplexer, Figure __.

Figure _. Multiplexer Configuration

7.3.4 Formatter Configuration

The 250 MHz to 10 GHz rate conversions produces a natural 80 bit wide word. This word consists of 16 format bits and 64 data bits. Two consecutive 80-bit words are combined to produce a 160-bit frame. The 160-bit frame is produced at an effective 62.5

MHz clock rate and time division multiplexed by 160. To maintain the order of the frame, a 16-bit partitioning and re-ordering circuit is used. It is placed between the input selector and the two 5:1 output multiplexers inside the formatter chip. This re-ordering is necessary to correct for the shuffling of the output selector.

A simplified formatter block diagram showing a 64-bit input bus, input selector, partition and re-ordering circuit, the addition 16 overhead bits, the times 5 multiplexers, the output selector and the final times 16 multiplexer is shown in Figure ___. Sixteen format bits are associated with each 64 data bit group. These bits are used for frame and Meta-frame synchronization, timing bits and transmission of the checksum word.

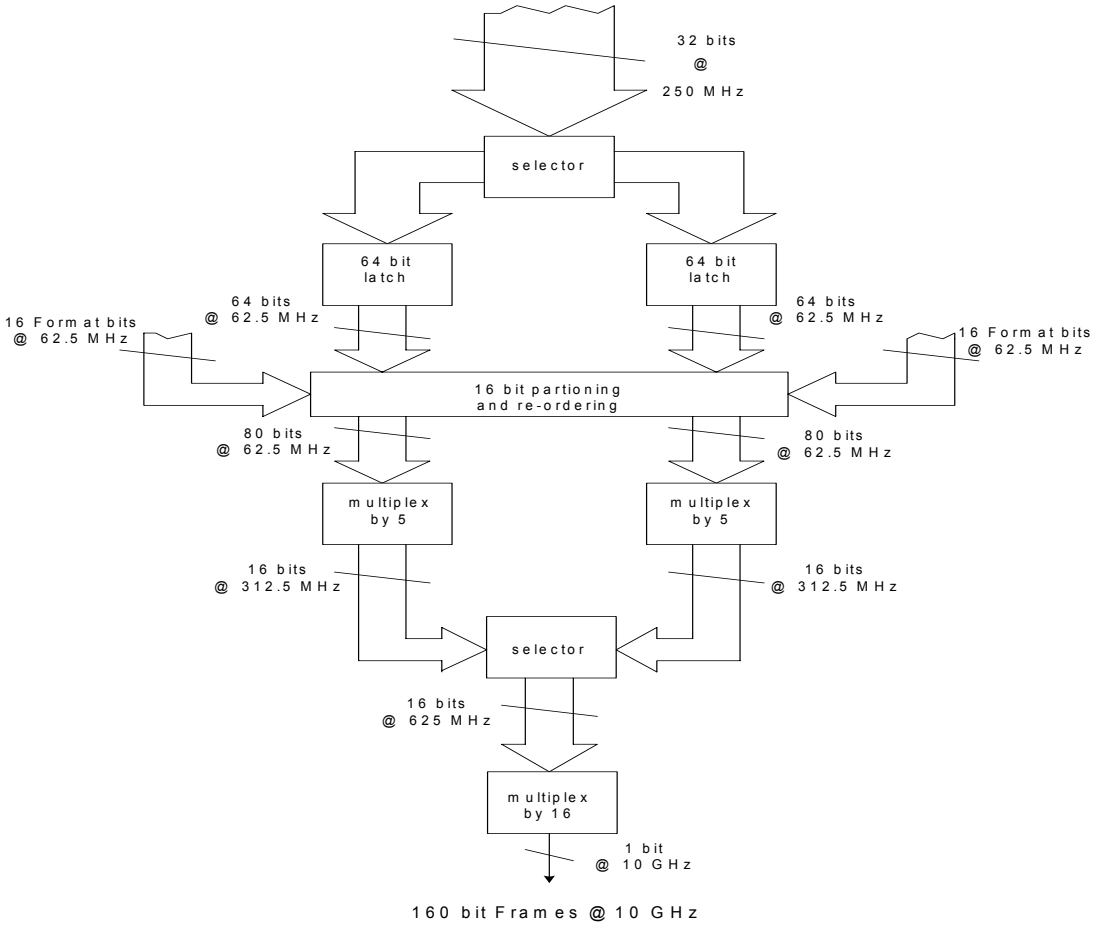

Figure 3 Simplified Formatter Block Diagram

7.3.5 Frame Synchronization

The sync word pattern is located at the same location in each frame although it is divided into two separate locations. The sync word is composed of ten bits of a unique pattern. The selected 10-bit pattern is similar to the seven-bit Barker sequence (binary 0100111). The pattern order is not important.

As with the transmitter, the receiver implementation utilizes a 16-bit wide data selector. This data selector follows the high-speed 1:16 de-multiplexer and shuffles the incoming 16-bit words. Partitioning the sync word makes it is possible to correctly locate the beginning of a frame and determine the data shuffling. The location of the first six bits of the sync word corresponds to the least significant bits of the 160-bit frame.

Frame synchronization moves through three stages: the search stage, the check stage and the monitoring stage. A 160-bit candidate frame is selected from the incoming serial bit stream. The ten sync location bits are checked for the pattern. If unsuccessful, a subsequent frame delayed by one bit time is selected and the comparison repeated. This process of changing the frame selection delay and sync pattern comparison repeats until a candidate frame is located. If no delay produces a match, the alternate shuffled possibility is checked according to the same algorithm. The matching criterion for the pattern comparison requires that all ten bits must match.

Once a candidate frame is located, the synchronization process enters the second or check stage. Since it is possible to correctly detect the sync pattern in a data stream the presence of the check stage is needed to improve the accuracy of detecting the true sync pattern. At least seven out-of-eight frame sync patterns must successfully identify that the true frame has been located. The possibility of a transmission bit error must be permitted. If this procedure fails, the system returns to the search phase and begins a new search.

In the monitoring stage, the system continually monitors the sync pattern for frame slippage. Two sequential mismatched frames or the mismatch of more than one of eight sequential frames will return the system to the search stage. The search begins as soon as an erroneous frame has been detected. In any situation where the search stage is re-entered, the search begins from the current shift value and not from a zero shift.

7.3.6 Meta-frame Implementation

To maintain frame concurrence across the three optical channels used to transmit each IF polarization, the formatter inserts an identical incrementing count into each frame. This count is extracted by the three receivers, compared, and delays applied to the early arriving channels. The result is three simultaneously clocked 160-bit frames with the identical incrementing count. Therefore, the received word will be identical to the transmitted word.

Together with the unique sync pattern, the sequence number creates a large virtual frame or meta-frame. The duration in time of the meta-frame or “size” is larger as the largest expected propagation time differences between channels. These differences arise due to inherent fiber characteristics and variations in dispersion and group delay with environment. Representative dispersion values for the Conventional band (C band: 1530 nm - 1565 nm) of single mode optical fiber optimized for use in Dense Wavelength Division Multiplexing (DWDM) applications are about 16 ps/nm/km to 18 ps/nm/km [3]. With 25 km of fiber and assuming a worst-case situation of two optical carriers separated by the maximum of 24 nm (the reddest red to the bluest blue), this only amounts to 2.4 ns

(24 bit times). The maximum calculated delay is about 10.1 ns (101 bits). These values scale linearly with distance. For the assumed distance and fiber types, a Meta-frame consisting of two 160-bit frames would be satisfactory. This implementation sets the Meta-frame size to two frames.

7.3.7 Data Integrity

The intrinsic bit error rate of the electro-optical components in the fiber transmission system is expected to be extremely low. However, in addition to the laser diode source, high-speed modulator, photo-diode detector, AGC amplifier, and the clock and data recovery electronics associated with each channel, the EVLA system includes a large number of manually re-configurable optical fibers and connectors. With each individual channel comprised of a number of complex high-speed components and multiple fiber segments, the need for continuous performance monitoring is obvious.

Presently 8 bits of each frame are used as a checksum of the previous 152 bits. This method detects all odd numbers of errors introduced in each 19-bit group.

7.3.8 Scrambling

Channel coding is the process of modifying the source data stream to facilitate proper reception. The source is composed of both payload information, whose characteristics are known only in a statistical sense, and overhead information. The sync pattern and sequence count parameters of the overhead are known, but not the other overhead bits. Thus channel coding is essential to provide adequate timing and to minimize low frequency content of each frame. Sufficient timing information is necessary to permit regeneration of the original data and to ensure low systematic jitter [2]. Data recovery and symbol timing is determined by a phase locked loop system operating on the high-speed channel data stream. It requires sufficient transitions per reciprocal loop bandwidth to properly operate. More data transitions produce less jitter and lower recovered bit error rates due to clock extraction timing errors.

To maintain low bit error rates low frequency content should be minimized. Equal numbers of ones and zeros produce a balanced signal with minimal low frequency content. This is important in AC coupled systems.

The Frame Synchronous Scrambling (FSS) will be is used in the EVLA to provide adequate timing and to minimize low frequency content. The entire frame, except for the ten sync bits, will be scrambled by a static random pattern. A selected scrambling pattern is added modulo 2 to the remaining bits of the frame with the first generated scrambling bit added to the eighth frame bit. A Shift Register Generator (SRG) produces the scrambling pattern and the pattern "runs" continuously throughout the 153 bits of the pattern. A seven stage SRG producing a 127-bit length sequence is used. The 153-bit pattern produced with a generator polynomial of $1 + X^6 + X^7$ and a seed or initial value of hexadecimal 46 has the required randomness properties [4]. The scrambling

pattern has 77 ones and 76 zeros achieving almost perfect DC balance. Table 2 shows the run length distribution of ones and zeros.

Table 2, Run length distribution of ones and zeros for 153-bit scramble pattern.

Run Length	Number of Ones	Number of Zeros
1	19	20
2	11	10
3	5	6
4	2	2
5	1	1
6	0	1
7	1	0

Table 2 also indicates the small amount of low frequency content in the pattern. The pattern has a total of only 4 runs of length greater than 4 bits with the longest one being only 7 bits. With a frame static pattern, the scrambling operation is performed in parallel across all frame bits from a single pre-loaded 153-bit long register. This register is implemented as an array of 20 byte-sized words, which are dynamically loaded with the desired pattern.

7.3.9 Self Test

Self-testing mechanisms are essential for the operational success of the EVLA DTS. These capabilities are different from the continuous error monitoring afforded by the inclusion of the checksum. Once a basic system fault has been detected, self-testing mechanisms will be provided to enable maintenance personnel to quickly isolate and repair the fault. The MCB will control the test pattern generator located in each transmitter formatter.

To check the clock recovery circuitry, a simple alternating pattern of ones and zeros is transmitted. In this mode, no frame or meta-frame synchronization, checksum calculation, or scrambling operations occur. Adding the ten-bit sync pattern to the test pattern allows frame detection diagnostics. Enabling the five-bit incrementing sequence number provides multiple channel synchronization testing. Enabling the scrambler with fixed payloads of all zeros or all ones tests scrambling. In the previous two cases, the checksum generation is disabled.

The final diagnostics evaluates the checksum system. Pattern 6 involves the checksum generation and checking of a 128-bit pattern of all zeros. Pattern 7 uses a pattern of all

ones. The remaining test patterns involve forcing an error in the checksum generation using the previous simple payload patterns. Table 3 summarizes these diagnostics patterns.

Table 3. Diagnostic modes.

Pattern 1	10 GHz clock Recovery	160 bits of alternating ones and zeros
Pattern 2	Frame Detection	Sync pattern + 153 bits of alt. ones & zeros
Pattern 3	Multiple channel synch	Sequence word + 148 bits ones and zeros
Pattern 4	Scramble + data pat #1	enable scrambler plus 148 bits of zeros
Pattern 5	Scramble + data pat #2	enable scrambler plus 148 bits of ones
Pattern 6	chksum with pattern #1	checksum of 128 + 3 bits of zeros
Pattern 7	chksum with pattern #2	checksum of 128 + 3 bits of ones
Pattern 8	forced chksum error #1	erroneous checksum of 128 + 3 bits of zeros
Pattern 9	forced chksum error #2	erroneous checksum of 128 + 3 bits of ones

Most of these diagnostic tests patterns use a twenty (20) byte dynamically loadable scrambling register. By combining the ability to disable the two 64-bit input words and changing the scrambling pattern all tests all of the above patterns can be generated, except those involving checksum generation.

7.3.10 IF Optics and WDM Systems

The twelve 10Gbits/s channels in each antenna are transmitted on the fiber by 5mw 1550nm lasers with integrated Electro-Absorption (EA) modulators. The current and temperature in the lasers is closely regulated to ensure wavelength stability and long life. Temperature, current and optical power are continuously monitored to provide information on the health of the laser to ensure reliable operation of the system at the lowest possible bit error rate.

The twelve optical carriers from each antenna are combined onto a single fiber using Wavelength Division Multiplexing (WDM). This requires the use of different wavelength Lasers for each of the twelve optical carriers from each antenna. These wavelengths fit onto the International Telecommunications Union (ITU) grid that defines 1550nm class wavelengths at 200GHz spacing. The exact wavelength of each laser is factory set and is by specified when each device is purchased. This adds some complexity to sparing and configuration control of the IF Data Transmission System. Twelve different wavelength lasers will be spared. Care must also be taken to track where these lasers are in the system and to make sure failed lasers are replaced with units operating in the same wavelength.

Table 4, DWDM Laser Frequencies and Wavelengths

Channel Number	Frequency (THz)	Wavelength (nm)	Signal
21	192.1	1560.61	
23	192.3	1558.98	
25	192.5	1557.36	
27	192.7	1555.75	
29	192.9	1554.13	
31	193.1	1552.52	
33	193.3	1550.92	
35	193.5	1549.32	
37	193.7	1547.72	
39	193.9	1546.12	
41	194.1	1544.53	
43	194.3	1542.94	
45			
47			
49			
51			

A typical semiconductor distributed feedback laser diode used as the transmitter in the optical channel has a mean time before failure, MTBF, of about 200 years. The EVLA array will contain 336 optical channels, thus on average over the 20-year design life, one laser will fail every 7 months. Reliability is very important. Unanticipated failures are very costly in terms of degraded observations. With so many expected failures, it is essential for the VPB design to use operational diagnostic and monitoring information. Since this discussion only deals with signaling protocol, hardware issues related to reliability will not be addressed. The monitoring of data integrity becomes important is part of the protocol.

7.3.11 IF Block Diagrams

Fig 1: Virtual Parallel Bus Transmitter Module
Fig 2: Digital PCB
Fig 3: 16:1 MUX PCB
Fig 4: Optical Electronics PCB
Fig 5: IF Digital Transmission System as implemented using four VPB transmitter modules in the antenna

7.3.12 IF Power Supplies

All IF Digital Transmission System hardware is powered from a single 48 Volt DC power source. The following local voltages required:

+1.5/1.8 VDC
+2.5 VDC

+3.3 VDC
+5.0
-5.2 VDC
+12 VDC

These voltages are derived from the 48 VDC power source by efficient, high reliability DC/DC converter modules located on each Printed Circuit Board.

7.3.13 IF Hardware Description

The hardware used in the IF DWDM is described.

7.3.13.1 Field Programmable Gate Array

The formatter is implement in Xilinx Virtex –E or Virtex-2 Field Programmable Gate Arrays (FPGA's). These devices accept input data from the digitizer system, perform all formatting, generation of error checking codes, and output the data and framing multiplexed into 625MHz 16 Bit words. All designs for the Xilinx FPGA's are done in the VHISI Hardware Description Language (VHDL – IEEE std 1076.3) utilizing Xilinx's Foundation series software.

7.3.13.2 The OC-192 Multiplexer

The 16:1 Multiplexing is accomplished using commercial SONET OC192 multiplexer IC's mounted on mezzanine printed circuit boards. Devices are available from AMCC and Giga/Intel. Future devices are expected from Maxim and several other manufacturers. The IC's are mounted on separate mezzanine boards. This was done to 1) reduce costs by using 10 Gbits/s design techniques and materials only on the smaller mezzanine boards, and 2) protecting us from the volatility of the rapidly changing telecommunications market.

7.3.13.3 Opto-Electronics

The optical portions of the DTS are on to a second mezzanine printed circuit board. These modules contain the circuitry to control current and temperature of the lasers, monitor the health and safety of the laser, and provide the bias current to the modulator and/or modulator driver.

7.3.13.4 Physical Packaging

Each Module is packaged in a standard VLA module housing. One side panel of the module is a large heat sink designed to conduct heat away from the high-speed electronics in the module while still providing RFI integrity. The electrical connectors are four Amp 68 Pin amplimite connectors designed for the high speed SCSI computer interfaces. The optical connectors are Diamond E-2000 blind mate connectors.

7.3.13.5 Manufacture and Assembly

7.3.14 Transmitter Module Cooling Requirements

This module is an RFI tight sealed container. All heat is conducted from inside the module to the heat sink that forms one of the vertically oriented side plates of the module. Chilled air forced upward through the rack passes over this heat sink to remove heat from the module.

7.4 Digital IF Receiver

7.4.1 Receiver (CEB) Hardware Design

The optical receiver is built around the Xilinx Virtex 2 Field Programmable Gate Array and a 10 Gbits/s 1:16 de-multiplexer made for SONET OC192 communications systems. Integrated photo receiver/amplifier devices are used to receive the 10 Gbits/s signal from the fiber. The twelve optical carriers from the transmitters in each antenna are split out from the one single mode fiber using passive de-multiplexer.

7.4.2 Block Diagrams

The following block diagrams show the design of the receiver system.

Fig 1: Receiver Module
Fig 2: Digital PCB
Fig 3: 1:16 DEMUX PCB
Fig 4: Optical Electronics PCB
Fig 5: IF Digital Transmission System receiver section

7.4.3 Power Supplies

All IF Digital Transmission System receiver hardware is powered from the 48 Volt DC battery power system in the WIDAR Correlator. The following local voltages required:

+1.5 VDC
+3.3 VDC
+5.0
-5.2 VDC
+12 VDC

These voltages are derived from the 48 VDC power source by efficient, high reliability DC/DC converter modules located on each printed circuit board.

7.4.4 IF Receiver Hardware Description

The hardware used in the IF receiver is described.

7.4.4.1 Field Programmable Gate Array

The receiver uses a Xilinx Virtex-2 Field Programmable Gate Arrays (FPGA's). This device accepts data from the 1:16 de-multiplexer IC, performs all synchronization, error checking, buffering and multiplexing functions. Data is output as 250 MHz 48 Bit words

to the WIDAR Correlator. All designs for the Xilinx FPGA's are done in the VHISI Hardware Description Language (VHDL – IEEE std 1076.3) utilizing Xilinx's Foundation series software.

7.4.4.2 The OC192 De-multiplexer

The 1:16 de-multiplexing is accomplished using commercial SONET OC192 de-multiplexer IC's mounted on mezzanine printed circuit boards. Devices are available from AMCC and Giga/Intel. Future devices are expected from Maxim and several other manufacturers. The IC's are mounted on separate mezzanine boards to 1) reduce costs by using 10 Gbits/s design techniques and materials only on the smaller mezzanine boards, and 2) reduce the impact of parts becoming obsolete.

7.4.4.3 Optical Electronics

The optical portions of the receiver modules are built on to a second mezzanine printed circuit board. These modules contain the photo receiver and all associated monitor and control circuitry.

7.4.4.4 Physical Packaging

The receiver module is built as an open frame module designed to be used as a mezzanine module on the Widar Correlator Station Card. It is built using a main Printed Circuit Board (PCB) with the fiber optic receiver and 1-16 de-multiplexer cards attached above it as mezzanine cards. It is designed to receive data from fiber optic cable from the WDM de-multiplexer, output data to the Widar Correlator through its mezzanine connector(s), and output data through a secondary port to be used during the transition period to feed data to the existing VLA systems.

7.4.4.5 Manufacture and Assembly

Due to the number of units required and the type of components used, these modules are best suited to fabrication on a commercial assembly line**.**

7.4.5 Optics and WDM Systems

The twelve 10Gbits/s channels in each antenna are transmitted on the fiber by 5mw 1550nm lasers with integrated Electro-absorption (EA) modulators. The twelve optical carriers from each antenna are combined onto a single fiber using Dense Wavelength Division Multiplexing (DWDM). This requires the use of different wavelength Lasers for each of the twelve optical carriers from each antenna.

The twelve different wavelength carriers are separated at the receiving end using a DWDM de-multiplexer. The resulting carriers are now on twelve discrete fibers and are be distributed to the receiver modules as required. The fibers terminate into an integrated photo receiver device. This device contains a biased photodiode that converts the signal back into electrical form. The output of this diode is AC coupled to a trans-impedance

amplifier to drive the 50-ohm impedances of the following stages. This signal is then amplified and leveled and fed to the input of the 1:16 OC-192 de-multiplexer IC.

7.4.6 IF Receiver Signal Interfaces

VPB Transmitter Module:
Inputs: 250/256 MHz, LVDS Digital Data from Digitizers

VPB Receiver Module
Outputs: 250/256 MHz, LVDS Digital Data to WIDAR Station Card and/or Transition Data Converter

7.4.7 Reference Signal Interfaces

VPB Transmitter and Receiver Modules
Inputs: 250 MHz Sine wave or LVDS System Clock and the 19.2 Hz LVDS timing signal

7.4.8 Monitor Control Interface

VPB Transmitter and Receiver Modules
I/O: M&C Ethernet Interface – 10/100BaseT or Fiber Pair
Module ID: 3 or 4 wire SPI interface to ID PROM on the Backplane

7.4.9 Power Supply Interfaces

VPB Transmitter and Receiver Modules

Power: 48 Volts DC

7.4.10 Receiver Module Cooling Requirements

This module is built as a vertically oriented, open-frame type module that is mounted to the station card in the WIDAR Correlator or to a temporary card plugged into a backplane during the transition. This module is directly cooled by chilled air forced upward through the rack passes over this heatsink to remove heat from the module. Heat producing components in this module are either designed for this type of application or have small, finned heat sinks attached to them to dissipate heat.

7.5 LO Reference Distribution System

This section is intended to address the requirements for the distribution of the LO references over the fiber optic link. This includes the measurement of the round trip phase. This part LO reference distribution system consists of four modules, the LO Offset Generator, the Round Trip Phase Receiver, the Central LO Transmit/Receiver, and the Antenna LO Transmit/Receiver. This system sends out a 512MHz signal on the LO-transmit-fiber then this signal is returned on the LO-receive-fiber and compared with a 512MHz that has been offset by 128Hz. The resulting 128Hz is then compared to the central 128Hz to complete the measurement of the residual round trip phase. The 512MHz sent to the antenna is cleaned-up and is used for the primary reference for the antenna LO system. Other references are also sent to the antenna on the LO-transmit-fiber. The requirements for these references are more thoroughly explained in chapter 6, the LO chapter.

7.5.1 Specifications and Requirements

The specifications and requirements for the LO reference distribution system are linked to the stability requirements for the over all LO system as presented in 6.5. Calculations of the predicted fiber stability with temperature are presented in EVLA Memo 10. Fiber temperature stability has improved due to advances in manufacturing and is now around 2ppm/degree C. Based on calculations, I believe that the overall temperature stability of the fiber buried at one meter will be about .5fs/s @ 512MHz. In 6.5 short term stability is .5ps/s @ 100GHz which translates to 2.5fs/s @ 512MHz. The long term stability requirements of 1.6ps per 30min will require round trip phase measurement. The electronics will dominate the LO reference stability and careful design will be required to compensate.

7.5.2 LO Offset Generator

The LO Offset Generator takes the 512MHz reference signal and offsets it by 128Hz. The offset is accomplished by injecting the 128 Hz into a phase lock loop steering a VCXO off frequency. The requirements of the LO Offset Generator are shown in Table 7.3.2

Table 7.3.2 LO Offset Generator Requirements

Frequency	Power Level dBm	Harmonically related spurious signals dBc	Non-Harmonically Related spurious signals dBc	Phase noise degree RMS	Notes
512 MHz					input
128 Hz	TTL	----------	----------	----------	Input square wave
512MHz + 128 Hz					output

7.5.3 Round Trip Phase Receiver

The Round Trip Phase Receiver takes the offset 512MHz and compares it to the non-offset 512MHz received back from the antenna. The non-offset 512MHz after demodulation from the LO-receive-fiber is put through a phase lock loop for filtering and smoothing. The bandwidth of the phase lock loop is to be TBD. The result of comparing the offset 512MHz and the non-offset 512MHz is the 128Hz signal that has been phase shifted by the fiber path. This 128Hz is squared up in a zero-crossing detector and compared to a non-phase shifted 128Hz. This comparison in accomplished by counting the difference between the two 128Hz signals. The resultant count will be the residual round trip phase. This count will be output to the module interface board (MIB). The input signal requirements to the Round Trip Phase Receiver are shown in Table 7.3.3.

Table 7.3.3 Round Trip Phase Receiver Requirements

Frequency	Power Level	Notes
128 Hz	TTL	Square wave
5MHz		
512MHz		
512MHz + 128Hz		

7.5.4 Central LO Transmitter/Receiver

The Central LO Transmitter/Receiver uses an external modulator to modulate the reference LO signals onto the LO-transmit-fiber. This module also receives the 512MHz reference back from the antenna on the LO-receive-fiber for round trip phase measurement. The LO signals to be modulated onto the LO-transmit-fiber are shown in Table 7.3.4 along with their requirements.

Table 7.3.4 Transmitted LO Reference Frequencies

Frequency	Power Level dBm			Notes
512 MHz				
32 MHz				
19.2 Hz				
1 Hz				

7.5.5 Antenna LO Transmitter/Receiver

The Antenna LO Transmitter/Receiver receives LO signals sent from the central control building on the LO-transmit-fiber. These signals are shown in Table 7.3.4. The 512MHz LO when received is put through a clean-up loop using a low noise VCXO. The bandwidth of this loop is to be about 1Hz. This signal is then modulated onto the LO-

receive-fiber to complete the loop for the round trip phase measurement system. The 512MHz signal and remaining LO signals are passed to the LO Reference Generator/Distributor where they are separated, processed, and distributed to various LO modules within the antenna. The VCXO requirements are shown in Table 7.3.5.

Frequency	Power Level	Phase noise	Drift rate	notes
512MHz				

7.6 LO Reference Distribution System

7.6.1 Specifications and Requirements

7.6.2 Round Trip Phase Correction Scheme

7.6.3 Transmitter (CEB) Hardware Design

7.6.3.1 Block Diagrams

7.6.3.2 Power Supplies

7.6.3.3 Electronics Design

7.6.3.4 Optical Design

7.6.3.5 Physical Packaging

7.6.3.6 Manufacture and Assembly

7.6.4 Receiver (Antenna) Hardware Design

7.6.4.1 Block Diagrams

7.6.4.2 Power Supplies

7.6.4.3 Electronics Design

7.6.4.4 Optical Design

7.6.4.5 Physical Packaging

7.6.4.6 Manufacture and Assembly

7.6.5 Signal Interfaces

7.6.6 Monitor Control Interface

7.6.7 Power Supply Interface

7.6.8

7.6.9 Cooling Requirements

7.7 Monitor Control System (Antenna & CEB electronics systems)

The EVLA monitor control system will be based almost entirely on commercially available technologies developed by the computer industry. It will utilize fiber optic based Gigabit Ethernet technology for faster computer to computer and antenna field networks and slower, lower cost, 100mb Ethernet technology for slower computer to computer and antenna electronics networks.

7.8.4.4 Direct Buried Splices

7.8.4.5 Underground Vault Splices

7.8.4.6 Antenna to Pad Connections

7.8.4.7 Antenna Pedestal Room

7.8.4.8 Antenna Azimuth Cable Wrap

7.8.4.9 Antenna Elevation Cable Wrap

7.8.4.10 Antenna Vertex Room

7.8.4.11 Antenna Apex

7.8.5

7.8.6 Fiber Optic and Laser Safety Requirements and Procedures

7.8.6.1 (THIS SECTION BEING WRITTEN BY JON SPARGO)

7.8.6.2 OSHA Safety Requirements

7.8.6.3 Laser Safety Training, Certification and Vision Testing

7.8.6.4

7.8.6.5 Fiber Optic Cable Accessibility (Planned and Accidental)

7.8.6.6

7.8.6.7 Fiber Optic Cable Fire Safety requirements

7.8.7 Fiber Optic Installation Standards and Procedures

7.8.8 Fiber Optic Cable Repair Standards and Procedures

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