EVLA Project Book, Chapter 6

6 LO / IF SYSTEMS

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Deleted 4096 synthesizer
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Updated central and antenna ref gen, updated syns specs
DDS specs, Switch specs, T304 specs, Vswr specs on
Converters.

Summary

This chapter describes the LO/IF system for the Expanded Very Large Array (EVLA) Project. The requirements and specifications are presented for each part of the LO/IF system. ***Transition issues for making antennas with new electronics hardware compatible with antennas that have existing hardware is also discussed.***

6.1 Introduction

The Very Large Array (VLA) was designed and built more than 20 years ago and since that time the need for a more sensitive instrument has arisen. The scientific requirements for a more sensitive instrument coupled with aging electronic equipment has lead to the much needed Expanded Very Large Array (EVLA) project. The EVLA project is designed to increase the overall system bandwidth by a factor of 80 and replace antiquated electronics with a new state of the art electronic system. The waveguide system will be replaced with a fiber optic system. The fiber optic system will transmit LOs to the antennas and receive digitized IFs from the antennas. The EVLA will contain new synthesizers, reference generators, IF converters, and samplers, which are described in this document.

6.2 Specifications and Requirements

The specification and requirements for the LO/IF system are contained in this document. General specifications that apply to every piece of the system are contained in the first few paragraphs while the more specific requirements for each module are shown in paragraphs particular to that module. As a general rule, all specifications will be equal to or better than the specifications for the current VLA system.

6.3 Environmental

The nominal temperature of each bin/rack will be within the range of +18 to +22 °C and will not vary more than ± 1 °C from nominal in any given 24 Hr period; additionally, the average slope of the temperature shall not exceed 0.25 °C/(30 min). All equipment will be designed to meet all specifications over a temperature range of +10 to +30 °C, at an altitude of 12,000 ft., and humidity level ranging from 0 to 95%.

6.4 General Module Interface

Each module in the LO/IF system shall use OSP type connectors for RF ports < 22 GHz on the back panel. For back panel RF ports that may exceed 22 GHz then OSSP type connectors up to 28 GHz may be used or the appropriate screw type connector may be used, provided mechanical safety devices are used to prevent damage. Any RF ports on the front panel shall be either BNC or SMA type depending upon the frequency range.

Each module shall use a D type connector for all DC and low frequency connections. The D connector shall be sized as to not exceed 80% of the pins on the initial design.

6.5 LO Phase Stability

These specifications do not include phase instability induced by the antenna structure or the atmosphere. These specifications do include any instability induced in the front end by the LO system. These specifications have been divided up by systems engineering as follows: one-third to the front end, one-third to the T304 downconverter, and one-third to the 4P, LSC, and UX converter combination.

Short term: Less than 0.5 ps rms for times under 1 second.
(this would be 5% coherence loss at 100 GHz)

Long term: Slope <200 fs/min for time scales longer than 30 minutes.
(roughly 1/4 turn at 40 GHz)

Peak-to-peak phase deviations over 30 minutes less than 1.4 ps
after removal of any linear slope (20 degrees at 40 GHz).

Phase shift with pointing change:

Less than 0.7 ps over the whole sky (10 deg at 40 GHz).
Less than 0.07 ps per degree of slew for short slews at elevations under 60 degrees (1 deg of phase at 40 GHz).

This specification applies after correction using any round trip and/or pulse cal data that might be available.

Phase noise is defined as phase instability outside an offset of 1 Hz from the frequency of concern. Phase drift is defined as phase instability within an offset 1 Hz from the frequency of concern.

6.5.1 LO Phase Noise Allocation

The phase noise allocation is shown in Table 6.5.1. For each of the components shown, the phase noise is obtained by integrating the power spectral density over the appropriate bandwidth. The phase noise specification is determined by the type of component and its location.

Table 6.5.1 Phase Noise Allocation

Component	Specification (fs)	Notes
Reference	200 max	1 to 10 Hz offset
Fiber distribution system	TBD	
12 to 20 GHz LO	100 max	integrated from the loop band width to 10 MHz
10.8 to 14.8 GHz LO	100 max	integrated from the loop band width to 10 MHz
Antenna Reference Generator	TBD	Integrated from 10 Hz to the 1st LO PLL cutoff

6.5.2 Phase Drift Allocation

Table 6.5.2 is a attempt to allocate the phase noise specification to various components of the system. It is likely that some of the components will be better than these allocations and some will be worse.

Table 6.5.2 Phase Drift Allocation

Component	Drift (degrees)/min	Notes
Round trip phase correction loop	TBD° @512MHz	
4.096 GHz LO	0.0013° /min/GHz	For a maximum average temperature slope of 0.25°C/(30 min)
12 to 20 GHz LO	0.0013°/min/GHz	For a maximum average temperature slope of 0.25°C/(30 min)
10.8 to 14.8 GHz LO	0.0013° /min/GHz	For a maximum average temperature slope of 0.25°C/(30 min)
Master LO Generator/distributor	TBD° @4GHz	
LO Transmitter system	TBD matched to ± TBD	Since all LO transmitters see the same temperature variation the phase drift as a function of temperature will be matched.

Antenna Reference Generator	TBD° @4GHz	
IF cables/switches	0.0013° /min/GHz/°C	
IF down/up converters	0.0013° /min/GHz	For a maximum average temperature slope of 0.25°C/(30 min) per converter, does not include drift introduced by the LO

The goal of 180 degrees of phase drift at 86 GHz for the system is interpreted here to represent the standard deviation of the difference between true phase of the electronics and the estimate made by linearly interpolating between two calibrations taken 30 minutes apart. The standard deviation of this difference should be less than 40 degrees at 86 GHz.

6.6 Fringe Tracking, Phase Switching, Sideband Suppression

Fringe rotation is required due a sinusoidal component introduced in the system caused by the rotation of the earth. This frequency is usually called the natural fringe frequency. The fringe frequencies are dependant upon baselines and observe frequencies. The fringe frequency can be canceled by introducing a continuous phase shift or frequency offset into one of the LOs used for down conversion. The fringe rotation will be removed using a direct digital synthesizer and its requirements are shown in Table 6.6. The calculations were based on equations derived by A. R. Thompson in EM #124.

Fringe rotation will take place in the correlator. However for the transition period from the old system to the new system, fringe rotation will be required at the antenna.

The second LO is required to support fringe rotation and 180d phase switching for the transition period. The phase switching is required to suppress spurious signals and d.c. offsets between the baseband downconverter and the samplers. The hardware required to support 180d phase switching will also support 90d phase switching if needed for sideband suppression during the transition period.

Table 6.6 Fringe Generator Requirements

Item	Frequency range (min)	Frequency accuracy	Phase shift increment	update time	notes
Fringe Generator (Internal to the 1st and 2nd LO synthesizer)	±(0 to 5 KHz)	1 part in 10^6	1°	.46sec max	1

Notes: 1. Calculations are based on 86 GHz front ends and a “Los Alamos” baseline.

6.7 RFI

RFI emissions for all LO/IF equipment shall meet the requirements set forth in EVLA Memo 59.

6.8 Mechanical

All LO/IF modules shall be compatible with existing BIN hardware currently in use at the VLA.

6.8.1 General Module Monitor Requirements

All analog monitor points within each module, unless otherwise stated, will be implemented using serial peripheral interface SPI bus technology. Each command word sent, will be echoed back from the module it was sent to, if possible.

6.9 Central Reference System

The central reference system (CRS) will take a signal from one of two reference standards and either divide or multiply this signal to generate various reference signals required by each antenna. The signals will be distributed to each antenna's central fiber optic transmitting system through a central reference generator and distribution system. The primary reference standard will be a hydrogen maser and the secondary or backup reference standard will be a rubidium oscillator. The CRS in addition to generating reference frequencies will also track long term drift of the reference standards via a GPS receiver. System timing will be accomplished using a central timing generator and will be distributed to each antenna's central fiber optic transmitting system. There will be a backup CRS rack to duplicate critical functions. The power for each CRS rack and the reference standards will be backed up with batteries. All critical functions of the CRS and the reference standards will be monitored by the online system.

6.9.1 Frequency Standards

There will be two frequency standards. The primary standard will be a hydrogen maser and the secondary or backup standard will be a rubidium oscillator. The principal performance requirements for the maser are shown in Table 6.9.1a while the rubidium requirements are shown in Table 6.9.1b. These standards will be purchased from external vendors.

Table 6.9.1a Principal performance requirements of the H-maser

Item	Requirement	Notes
LO-Ref max frequency error	1 part in 10^{12} averaged over 10 sec	
Wide-band phase noise at 5 MHz	1.4 psec RMS	see 6.5
Allan Variance	1<t<1000secs 2E-13t $^{-3/5}$ 1000<t<10,000secs 3E-15	

Table 6.9.1b Principal performance requirements of the Rubidium Oscillator

Item	Requirement	Notes
LO-Ref max frequency error	1 part in 10^{12} averaged over 10 sec	
Wide-band phase noise at 5 MHz	1.4 psec RMS	
Allan Variance	1 sec <5E-12 10 sec <1.6E-12 100 sec <5E-13 1000 sec <5E-13	

6.9.2 Timing Generator (deleted)

6.9.3 GPS Receiver

The GPS receiver will be purchased from an external vendor. The receiver will serve as the UTC time reference for the array. All clocks can be synchronized to the GPS, so that on a long term basis, the time at the array can be known within 10 nsec.

The GPS receiver will have a built-in or external time interval counter with a computer interface that will provide time offset and slope for the data analysts.

6.9.4 LO Reference Generator L350

The LO reference generator takes the reference standard frequency and multiplies it to the frequencies shown in Table 6.9.4. The specific requirements for each frequency is also shown in this table.

The L350 generates a Time Code Output that is sent via optical fiber to the WIDAR Correlator. The Time Code is a 128 Mbps LVPECL signal that is encoded with a 1PPS and a 1 pulse per minute.

The L350 generates a 1PPS that is used by the L353 . This pulse is the divider reset pulse and is modulated onto the 512 MHz LO sent to the antenna. The pulse is only activated when needed. The pulse has a width of 100 ns and a rise time of less than 4 ns.

Table 6.9.4 Reference Generator Frequencies

Frequency MHz	Power Level dBm ±1 dB	Harmonically Related spurious signals dBc	Non-Harmonically Related spurious signals dBc	Phase noise ps integrated from 1 Hz to 10 MHz unless otherwise noted	location	Notes
19.2 Hz	TTL	N/A	N/A	N/A	reference output	switchable after transition
1PPS	LVPECL	N/A	N/A	N/A	reference output	
128 Hz	TTL	N/A	N/A	N/A	reference output	To L351
128 Hz	LVTTL	N/A	N/A	N/A	reference output	To 128Hz Dist
5	+13	35	50	3.3	reference output	phase noise integrated from 1 Hz to 2 MHz
5	-6	35	50	3.9	reference dist output	phase noise integrated from 1 Hz to 2MHz
128	+10	35	45	0.4	LO ref gen output	
512	+12	50	50	0.6	LO ref gen output	
512	+12	40	40	0.7	LO ref dist output	

6.9.5 LO Ref Distributor L354

The LO reference distributor shall take the reference signals of the LO reference generator and amplify them. These signals will then be divided either internally or externally and sent to the central fiber optic transmitter system of each antenna. The specific requirements for output frequencies are shown in Table 6.9.4.

6.9.6 LO Transmitter L353

The LO Transmitter L353 is part of the fiber optic system and is described in chapter 7 paragraph 7.5 of the project book.

6.9.7 Master Offset Generator L351

The Master Offset Generator L351 is part of the round trip phase system and is described in chapter 7 paragraph 7.5 of the project book.

6.9.8 Round Trip Phase Receiver L352

The Round Trip Phase Receiver L352 is part of the round trip phase system and is described in chapter 7 paragraph 7.5 of the project book.

6.10 12-20 GHz LO System

6.10.1 12-20 GHz Synthesizer L301

The 12-20 GHz synthesizer provides the LO signals for the first down conversion. There will be two 12-20 GHz synthesizers in each antenna . One synthesizer is switched to one of the high frequency front ends for block down conversion or it is switched to an up converter for the low frequency front ends. The second 12-20 GHz synthesizer is switched to the UX downconverter or it is switched to the same up converter for the low frequency front ends as the first 12-20 GHz synthesizer. In the high frequency front ends, where necessary, the synthesizer frequency is either doubled or tripled. While in the UX downconverter, the LO is always doubled. The exception is that both synthesizers are used in the UX downconverter for Ku band. The synthesizer is YIG based and designed for low noise, phase coherent operation**.** See 6.14.3.2 for an explanation of the UX down converter.

The synthesizer has the following performance specifications:

Output Frequency tuning	11776-20224 MHz in 256MHz steps	
Output Power	+13 dBm Nominal and Adjustable	
Output Spurious signal level	<-70 dBc except for harmonics of ref	
Output harmonics of Ref	<-80 dBc	
Phase Noise	-107 dBc/Hz @100KHz offset and -90 dBc/Hz @ 10KHz offset @20GHz output frequency Which corresponds to a phase noise of <100fs	
Harmonics	<-40 dBc	
Output VSWR	<2:1	
RF port impedances	50 ohm	
Lock time	1 sec max between any two frequencies	
Supply voltages	Voltage	Current
	+16.5	2.5 amps max
	-16.5	0.5 amps max
	+6.5	2 amps max
Power Dissipation	75 watts max	
Monitor Points	Synthesizer freq 1MHz Resolution Synthesizer output power Lock condition FM tuning voltage Main coil voltage Power supply voltages 2 Module Temperatures	
Synthesizer out to ref in isolation	<-40 dBc	
Rear Panel connections	MIB interface 512 MHz Ref in: noise of ref:	

	<100 fs
	Synthesizer out
	Power supply voltages
Front panel requirements	Frequency display to 1 MHz Res
	SMA output of 512 MHz ref
	BNC output of FM tune voltage
	Lock condition indicator

6.11 10.8-14.8 LO System

6.11.1 10.8-14.8 Synthesizer L302

The 10.8-14.8 synthesizer provides the last tunable LO for down conversion of the astronomical data before digitization occurs. This is a dual YIG based synthesizer designed for low noise, phase coherent operation**.** This synthesizer will have two integral direct digital synthesizers (DDS) to provide fine tuning for fringe rotation and phase switching. There will be four 10.8-14.8 synthesizers in each antenna.

The synthesizer has the following performance specifications:

Output Frequency	10.8 to 14.8 GHz nominal	
Output Frequency Steps	Sub milliHertz	
Output Power	+13 dBm Nominal Adjustable	
Output Spurious signal level	<-70 dBc except for harmonics of ref	
Output harmonics of Ref	<-80 dBc	
Phase Noise	-108dBc @100KHz offset and -87dBc@10KHz offset @15 GHz output frequency	
	Which corresponds to a phase noise of <100fs	
Harmonics	<-40 dBc	
Output VSWR	<2:1	
RF port impedances	50 ohm	
Lock time	1 sec max between any two frequencies	
Supply voltages	Voltage	Current
	+16.5	2.5 amps max
	-16.5	0.5 amps max
	+6.5	3 amps max
Power Dissipation	75 watts max	
Monitor Points	Synthesizer freq 1MHz Resolution	
	Synthesizer output power	
	Direct Digital synthesizer power	
	Lock condition	
	FM tuning voltage	
	Main coil voltage	
	Power supply voltages	
	2 Module temperatures	
Synthesizer out to ref in isolation	<-40 dBc	
Rear Panel connections	19.2 Hz in: with <TBD ns of Jitter on rising	

	Edge MIB interface 128 MHz Ref in: noise of ref: <100fs Synthesizer out Power supply voltages
Front panel requirements	Frequency display to 1 MHz Res BNC output of fine tune syn SMA output of 128 MHz ref BNC output of FM tune voltage Lock condition indicator
DDS outputs	1 to 22 MHz and 22 to 42 MHz Noise: >-140dBc @100KHz

6.11.2 Fringe Generator

The fringe generator uses direct digital synthesis techniques to achieve its high frequency and phase resolution. The device is based on the Analog Devices AD9852 DDS integrated circuit. The AD9852 provides the infrastructure to obtain very sophisticated control over its output. Below is a short discussion of the features of the device that apply to the fringe generator.

The DDS contains a 48 bit digital phase accumulator which is truncated to 17 bits. This 17 bit phase word is then converted to a 12 bit sine function which drives a high speed Digital to Analog Converter (DAC). There is a programmable 48 bit frequency accumulator. At each system clock cycle, 256MHz in this application, the frequency accumulator contents are added to the phase accumulator. The result is that any frequency between DC and half the clock frequency can be generated to a resolution of sub micro hertz. In the fringe generator the lower frequency limit is established at about 8 MHz by the output coupling transformer.

There is a programmable 48 bit delta frequency word register. At each system clock cycle, the contents of this register are added to the frequency accumulator. This results in an FM chirp signal.

The DDS contains a programmable 14 bit phase offset register. The contents of this register are added to the contents of the 48 bit phase accumulator before conversion to the sign function. This register is used to produce the ± pi/2 and ±pi/4 phase switching needed in the LO system.

This phase accumulator can be reset to zero on command. This, along with the two programmable frequency control registers, allow the approximation of any desired phase profile function modeled by a polynomial with up to two coefficients in the hardware. Along with the 14 bit phase offset word, an arbitrary initial condition can be obtained with up to fourteen bit resolution. Movement to a new function with different coefficients can be accomplished in a single system clock cycle. The primary limitations are the time required for the micro controller to load the required parameters into the DDS registers and the settling time of other components in the LO synthesizer.

The DDS uses a serial interface protocol to load it's internal registers under control of an FPGA. When all I/O registers are loaded, an I/O update pulse is issued to the DDS to cause all data in the I/O registers to be loaded to the

DDS active core on a single system clock edge. There is a system pipeline delay of 17 clock cycles, from the first clock edge after the I/O update, until the time these parameters take effect. They all take effect immediately on that clock edge.

Except for the case of a reset to the DDS, the output is always phase continuous, i.e., the phase of the start of a new phase function begins where the previous one was at the time the new parameters take effect. This defines the phase offset register contents as part of the desired phase function.

The output of the DDS is a zero order hold sampled sine wave at the programmed frequency and phase.

All system timing events within the VLA are synchronized to a 52 millisecond fiducial which is distributed throughout the array. The DDS uses this signal to synchronize its activities with the rest of the array. There is a large Field Programmable Gate Array (FPGA) in the fringe generator which derives the necessary timing signals from the 52ms tick and the system clock. This FPGA contains a set of counters and state decoding logic to derive the I/O update signal for the DDS to keep all parts of the fringe generator synchronized. This FPGA is a Xilinx Spartan series XC2S30.

The board uses the SPI protocol to interface to the MIB. The SPI signals are routed through the FPGA to the DDS chip and additional synchronizer logic is implemented in the FPGA.

External Connections

1. 5VDC power, .5amp nominal
2. Power return. Connected to case
3. 128 MHz clock input, sine wave, terminated with 50 ohms.
4. 52 ms reference LVDS, terminated with 100 ohms.
5. Output, 50 ohm impedance, +0 dBm
6. Interface bus

6.11.3 LO Switches

There will be a set of three 12 to 20 GHz synthesizer select switches. These switches are used to select which front end and/or the UX Converter receives the 12 to 20 GHz LO. These switches are specified in Table 6.11.3. The switches will be controlled through a DCS interface module.

Table 6.11.3 12 to 20 GHz LO Switch Specifications

Item	Specification	Notes
Frequency Range	12 to 20GHz	
VSWR	2.0 to 1 Max	
Insertion Loss	4 dB Max	
Isolation	50 dB min	
Input impedance	50 Ohm nominal	
Actuating Voltage	TBD	
Actuating Current	TBD	
Switching Time	15 ms max	
# poles	1	Per switch
#throws	4	Per switch
RF connection	SMA	
Power Connector	TBD	

6.12 Antenna Reference System

6.12.1 LO Reference Generator/Dist. L305

The LO reference generator/dist. takes the reference frequencies which were transmitted on the fiber link and cleans them up where necessary. The Reference Generator/Dist also multiplies or divides the reference frequencies from the fiber link to frequencies required by the antenna LO system. These frequencies are shown in Table 6.12.1. The specific requirements for each frequency are also shown in this table.

The L305 generates a Time Code Output that is sent over optical fiber to the DTS/Sampler modules. The Time Code is a 128 Mbs LVPECL signal that is encoded with a 52 millisec signal.

The L305 is equipped to detect a divider reset pulse that is transmitted from the L353 module and is modulated onto the 512MHz LO sent optically to the antenna. The pulse is used to reset all of the dividers in the L305.

Table 6.12.1 Antenna Reference Generator Frequencies

Frequency MHz	Power Level dBm ±1 dB	Harmonically Related spurious signals dBc	Non-Harmonically Related spurious signals dBc	Phase noise degree rms to 10 MHz offset	location	Notes
9.6 Hz	TTL	N/A	N/A	N/A	Ant LO ref gen output	optically transmitted
19.2 Hz	LVDS	N/A	N/A	N/A	Ant LO ref gen output	To L302 switchable after transition
19.2 Hz	RS422	N/A	N/A	N/A	Ant LO ref gen output	MIB Distr switchable after transition
128	+13	25	40	0.025	Ant LO ref gen output	
512	+0	35	50	0.058	Ant LO ref gen output	
1024	+3	40	50	0.130	Ant LO ref gen output	
4096	+0	40	40	0.650	Ant LO ref gen output	

6.12.2 LO Reference Receiver L304

The LO Reference Receiver L304 is part of the fiber optic system and is described in chapter 7 paragraph 7.5 of the project book.

6.14 Intermediate Frequency System

The intermediate frequency system selects four IFs from either the 4, P, L, S, or C Band front end or it selects two IFs from either the A, K, or Q Band front end. The selection occurs through band switches. A, K, and Q band front ends are designed with block down converters. The block down conversion scheme will converts IFs to the 8 to 18 GHz range for the UX converter. The UX converter then divides the IFs and eventually delivers 4 IFs in the 8 to 12 GHz range. See 6.14.3.2 for a better description of the UX converter. The 4, P, L, S, and C band front ends need to be up converted externally to the 8 to 12 GHz range. The lower frequency front ends are converted using two 12 to 20 GHz synthesizers. The U band front end is converted to 8 to 12 GHz in the UX converter using both 12 to 20 GHz synthesizers. The 8 to 12 GHz IFs are then switched into the baseband downconverters. The baseband downconverter takes the 8 to 12 GHz IFs, performs total power detection and either a single or double down conversion. Single conversion is used with the low resolution sampler while, double conversion is needed for the high resolution sampler. The IFs out of the baseband downconverter are either 2 to 4 GHz (for low resolution sampling) or the range of 1 to 2 GHz (for high resolution sampling). The lower frequency path is provided for narrow band lower frequency front ends or observations that require high resolution sampling. The LO for the lower frequency path is provided by a 4096 MHz reference. The output of the baseband downconverter is switched into the samplers. There are two samplers provided, one is a 2 to 4 GHz 4GS/s 3 bit sampler and the second is a 1 to 2 GHz 8 bit sampler. The sampled IFs are then modulated onto the fiber optic system.

6.14.1 Band Switches

There will be two sets of four band select switches (one switch per IF). These switches are used to select the IFs from the different front ends. One set of switches is used to select the 8 to 12 GHz IFs and are specified in Table 6.14.1a. The other set is used to select IFs in the 1 to 8 GHz range and is specified in Table 6.14.1b. There is a third set of two IF switches. This third set is used to select the block down converted 8 to 18 GHz IFs from the high frequency front end and is specified in Table 6.14.1c. The switches will be controlled through a DCS interface module.

There will be a set of two intermediate band select switches (one per polarization). These intermediate band switches are used to select the IFs from either the L, S, or C front ends to a second set of two switches. The second set of switches are used to select either the signal from the 4P Converter or the signal selected from the intermediate band switches to go to the LSC Converter. This combination of switches was chosen because both the 4P Converter and the LSC Converter are contained within the LO-Rack thus reducing the number of signals leaving and entering the rack.

There will be a set of two high band select switches (one per polarization). These high band switches are used to select the IFs from either the Q, A, U, or X band front ends to the UX Converter.

There will be a set of four pre Down Converter switches (one per IF). These pre Down Converter switches are used to select a signal from either the UX Converter or the LSC Converter to go to the IF Transfer Switches and into the Down Converter.

All of these switches are specified in Table 6.14.1 The switches will be controlled through a DCS interface module.

Table 6.14.1 Band Switch Specifications

Item	Specification	Notes
Frequency Range	1 to 18 GHz	
VSWR	1.4 to 1 Max	
Insertion Loss	.4 dB Max	
Isolation	60 dB min	
Input impedance	50 Ohm nominal	
Actuating Voltage	TBD	
Actuating Current	TBD	
Switching Time	15 ms max	
# poles	1	Per switch
#throws	4	Per switch
RF connection	2.9mm	
# of switches per antenna	10	
Power Connector	TBD	

6.14.2 Transfer Switches

After the IFs are selected with the Band Select switches, then the IFs go through a set of 2 IF transfer switches. These transfer switches allow the IFs to be transferred to a different IF downconverter**.** These switches are used to reverse the IF polarization. These switches are specified in Table 6.14.2.

Table 6.14.2 IF Transfer Switch

Item	Specification	Notes
Frequency Range	DC to 12 GHz	
VSWR	1.4 to 1 Max	
Insertion Loss	.5 dB Max	
Isolation	70 dB min	80 dB goal
Input impedance	50 Ohm nominal	
Actuating Voltage	+28 v	
Actuating Current	215ma	
Switching Time	20 ms max	
# poles	2	Per switch
#throws	2	Per switch
RF connection	SMA	
Power Connector	DC Feedthrus	

6.14.3 Converter Modules

6.14.3.1 4P Converter T301

The 4P converter module is used to convert both the 74 MHz front end and the P-Band front end to L-Band. Power dividers are used at the input to allow dichroic observations. The corresponding IFs for 4-Band and P-Band are diplexed together. Each IF is up converted with the same fixed LO. The specifications for this converter are shown in Table 6.14.3.1.

Table 6.14.3.1 4P Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	4	
Input frequency range	70 to 426 MHz	
Input power level per IF per GHz	-35 dBm/2 MHz 4 band -45 dBm/50 MHz P band	
Headroom	60 dB	with -35 dBm in, Headroom measured from 1 dB compression point
# of LOs per module	1	1 fixed
Frequency range of LO	1.024 GHz fixed	
Power Level of LO	+3 dBm	Nominal
Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	1.094 to 2 GHz	
Power Level of output	-45 dBm/GHz	
1 dB compression point	+18 dBm	nominal
Headroom	63 dB	Headroom measured from 1 dB compression point
LO 2nd harmonic spur and leakage	-40 dBc	
IF input VSWR	1.2 to 1 Max	
IF input noise figure	9 dB Max	@25°C
Image rejection	-30 dBc	
Passband ripple	.2 dB	for ripple with a period less than 2 MHz
Overall flatness	1.5 dB	from 1090 to 1400 MHz
Phase/delay stability	TBD	
Isolation between channels	70 dB Min	80 dB goal
Interface	MIB	External with SPI bus

Control requirements	solar attenuator	
Monitor requirements	IF total power, regulated voltages, temperature, solar attenuator status	

6.14.3.2 UX Converter T303

The UX converter is used to down convert IFs in the 8 to 18 GHz range to X-Band. The IFs are either from the Ku-band, K-band, Ka-band, or Q-band front end. One of the first LO synthesizers is used to block down convert either the K-band, Ka-band, or Q-band front end to the 8 to 18 GHz range. This block down converted IF is then fed to the converter where it is processed. The processing proceeds as follows: If the frequency range of the "wanted" input IF is within 8 to 12 GHz, then the IF is simply passed through the converter. If the frequency range of the "wanted" input IF is not within the 8 to 12 GHz range, then the IF is down converted using the other first LO synthesizer. For the Ku-band front end, both of the first LO synthesizers are used to down convert the IFs to X-band. Note: any converted IF will be spectrally inverted from the non-converted IF. The specifications for this converter are shown in Table 6.14.3.2.

Table 6.14.3.2 UX Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	2	
Input frequency range	8 to 18 GHz	
Input power level per IF per GHz	-53 dBm ±3 dB	Depends upon front end selection
Variation of power spectral density	3 dB Max	per 4 GHz sub band
Headroom: X-band thru path Ku-band converted path	38 dB nominal 25 dB nominal	Headroom measured from 1 % compression point
# of LO per module	1 or 2	internally doubled (see description)
Frequency range of LO	12 to 14 GHz	Doubled to 24- 28 GHz
Power Level of LO	+10 dBm	Nominal
Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	7.5 to 12.5 GHz	
Power Level of output	-48 dBm ± 1.5 dB	per 4 GHz sub band
LO 2nd harmonic spur and leakage	-60 dBm	12 to 14 GHz

IF input VSWR	1.4:1 max	1.35:1 goal
IF input noise figure	5.2 dB max	
Image rejection	-30 dBm Min	
Passband ripple	.2 dB	for ripple with a period less than 2 MHz
Overall flatness	2 dB/2 GHz	
Phase/delay stability	.0013°/min/GHz	For a maximum average temperature slope of 0.25°C/(30 min)
Isolation between channels	70 dB Min	80 dB goal
Isolation between each path of the same IF	70 dB Min	80 dB goal
Interface	MIB via M301	Fiber ethernet
M&C requirements	See A23275A003	

6.14.3.3 LSC Converter T302

The LSC Converter module is used to convert the lower frequency front ends to X-Band. This converter uses the 12 to 20 GHz synthesizer for the conversion process. The specifications for this converter are shown in Table 6.14.3.3.

Table 6.14.3.3 LSC Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	4	
Input frequency range	1 to 8 GHz	
Input power level per IF per GHz	-50 dBm/GHz	Nominal
Variation of power spectral density	±1.5 dBm/500 MHz	
Headroom	60 dB Min	Headroom measured from 1 dB compression point
# of LO per module	2	
Frequency range of LO	12 to 20 GHz	
Power Level of LO	+3 dBm	

Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	8 to 12 GHz	
Power Level of output	-50 dBm/GHz	
1 dB compression point	+10 dBm	nominal
Headroom	60 dB Min	Headroom measured from 1 dB compression point
LO 2nd harmonic spur and leakage	-40 dBc	
IF input VSWR	1.35 to 1 max	1.3:1 goal
Image rejection	-30 dBc min	
Passband ripple	.2 dB	for ripple with a period less than 2 MHz
Overall flatness	1.5 dB/2 GHz	
Phase/delay stability	TBD	
Isolation between channels	70 dB Min	80 dB goal
Interface	MIB via M301	External with SPI bus
M&C requirements	see A23270A002	

6.14.4 Downconverter T304

In each antenna there will be four Downconverter modules, one per IF. The IFs are in the to 8 to 12 GHz range and total power detection and leveling are performed on the full range IF. These IFs are then split in two inside each module. These two IFs are down converted with the 10.6 to 14.6 GHz Synthesizer and the resultant IFs are in the passband from 2 to 4 GHz. Another conversion is provided for low band signals that may require higher resolution samplers due to higher levels of RFI.. This conversion uses the 4.096 GHz reference generator output and is used only on one of the split 8 to 12 GHz IFs. This lower passband is from 1 to 2 GHz. The eight 2 to 4 GHz IFs from the four downconverters will be harmonic sampled by 3-bit 4 GS/s samplers. The four lower frequency IFs will be harmonic sampled by 8-bit 2 GHz samplers. The input and output noise power spectral distribution will be nominally flat over the passband. The downconverter module provides for total power measurement of each split IF as well as the total IF. Internal filters and external filter connections will be provided to either narrow the desired passband or notch out undesired areas within the passband. The specifications for the downconverter are shown in Table 6.14.4.

Table 6.14.4 IF Downconverter Specifications

Item	Specification	Notes
Number of modules	124	4 per antenna + 12 spares
# of IF inputs per module	1	
Input frequency range	7.5 to 12.5 GHz	
Input power level per IF per GHz	-47.5 dBm	
Variation of power spectral density	±1.5 dBm	
Headroom at input	>20 dB	Headroom measured from 1% compression
# of LO per module	3	independently tunable
Frequency range of LO	10.6 to 14.6 GHz and 4.096 GHz	
Power Level of LOs	+12 dBm for 10.6 to 14.6 GHz +0 dBm for 4.096 GHz	
Spurious levels of LO	<-70 dBc for spurious, <-80 dBc for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	3	
Frequency range of output	2 at 2 to 4 GHz, or 1 at 1 to 2 GHz	
Power Level of output	-29 dBm	
Headroom after conversion	>20 dB	Headroom measured from 1% compression
LO 2nd harmonic spur and leakage	<-40dBc	
IF input VSWR	1.25:1 Max	
IF input noise figure	<12 dB	
Image rejection	>30 dB	
Passband ripple	.2 dB	for ripple with a period less than 2 MHz
Overall flatness	2 dB/2 GHz	smooth variations only
Phase/delay stability	0.0056°/min/GHz	For a maximum average temperature slope of 0.25°C/(30 min)
Isolation between channels	>70 dB	80 dB goal
Total power detector response time	2 ms	

Phase linearity	<1.6nsec/2 MHz	
Interface	MIB	internal
SNR degradation	<1%	
M&C requirements	SPI Bus interface to MIB	

6.15 Samplers

6.15.1 2-4 GHz Sampler

The samplers installed in the antennas provide the flexibility required for the fiber optic transmission of the IF. Digital conversion is of course indispensable to the correlator in order to derive the correlation function as a function of lags for spectroscopy. The samplers are thus crucial and single-point-failure elements in the system. The EVLA will incorporate 3-bit samplers thus improving the overall sensitivity compared to the 2-bit correlator. The specifications for the samplers are given in Table 6.15.1.

Table 6.15.1 2-4 GHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	2-4 GHz	
Clock Rate	4096 MHz	
Resolution	3 bits	
Quantization	8 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/16	
Output Word Rate	256 MHz	
Power Consumption	TBD	

The sampler includes several fundamental elements briefly described below. The input adapter amplifier, the comparators and the associated latches and encoding are implemented in a single ASIC. The fast demultiplexing unit is separate from the ASIC to diminish any coupling of the digital output with the analog signal input. The ASIC and the demultiplexing unit form the sampler proper. A PLL box produces and distributes the sinusoidal 4096 MHz sampling clock and the TBD signal required by the demultiplexing unit. This is another separate unit which will be common to at least one sampler pair.

Input Adapter Amplifier

The analog signal is delivered from one of the four output of the IF downconverter modules in the 2 to 4 GHz range. It is random with Gaussian statistics. The response of this amplifier is flat within ± .5 dB over 2 GHz bandwidth and linear up to about +15 dB above R.M.S. input signal range. The voltage supply required for the adopted ASIC technology is ± 1.25 V.

The sampler input level is controlled in the IF downconverter with ±.25 dB attenuators placed in the 2-4 GHz output paths of each IF downconverter. This allow minimization of platforming effects and keeps the quantization thresholds constant and at their optimum level for maximum quantizing efficiency.

Comparators and Quantization Thresholds
The sampling function is preformed in the comparators which include two latches operated in a master-slave configuration and clocked at 4096 MHz. The 4096 MHz clock signal is equally distributed to 7 comparators. It's shaped internally in a dedicated amplifier driven by the external 4096 MHz sinusoidal signal. The seven thresholds comprise a zero reference voltage and are set around ±0.5 'sig', 1 'sig' and 1.5 'sig', where 'sig' is the R.M.S. voltage at the common input of the 7 comparators; these levels are kept constant and their exact value is tuned with an accurate division voltage chain so as to minimize the quantization losses. First simulations of SiGe samplers indicate that the sampler indecision region is small and at the level of 1% of the smallest comparison threshold.

Encoding
The sampler encoding is not yet finally adopted.

6.15.2 1-2 GHz Sampler

In addition to the 2-4 GHz sampler, a lower frequency higher resolution sampler is required. Due to higher RFI in L-Band, an 8-bit sampler will be needed. A higher number of bits allows more dynamic range and allows the correlator to better filter unwanted RFI. This sampler will be used for either harmonic or bandpass sampling, where the IF to be sampled is in the region from 1000 to 2000 MHz. The specifications for this sampler are shown in Table 6.15.2.

Table 6.15.2 1000 to 2000 MHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	2000 MHz	
Clock Rate	1024 MHz	
Resolution	8 bits	
Quantization	256 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/8	
Output Word Rate	256 MHz	

Power Consumption	TBD	

6.15.3 Digital Transmission System Module D301

The Digital Transmission System Module D301 will house both samplers as well as the data formatters and fiber optic transmitters. This module is described in chapter 7 of the project book.

6.16 Transition Hardware

There will be special hardware necessary to keep the new electronics compatible with the old correlator. This hardware is necessary since the new correlator in not expected to be in place until most antennas are modified with the new electronics**.** This new hardware consists of the 8 bit sampler, a digital decimator for frequency conversion, a digital to analog converter for conversion back to an analog IF, and the current baseband filter and driver modules, T4 and T5. The 8 bit sampler data will be digitally filtered and converted back to analog and then input to the current baseband signal hardware.

6.16.2 Transition Converter

The transition converter consists of a 8 to1 digital decimator followed by an FIR filter then another 2 to 1 digital decimator followed by another FIR filter. Finally, in the transition converter there is a spectral inverter followed by a digital to analog converter. The decimators down converts the signal that was in the 1152 to 1216 MHz range to a signal that will end up in the 0 to 64 MHz range. The 1152 to 1216 MHz was chosen because of clock frequencies. The decimator clock will be 256 MHz allowing both sidebands of the IF to appear at multiples of the 128 MHz. The digital filters will be implemented in the FPGAs located in the deformatter module. The DAC will also be in this module. The final digital signal will then be fed to a digital to analog converter. The digital to analog converter needed for the transition is specified in Table 6.16.2. This D to A converter is necessary to reconstitute the digital data to analog form for the old correlator.

Table 6.16.2 Transition Digital to Analog Converter

Item	Specification	Notes
Update rate	128 MHz	256 if necessary
Resolution	10 bits	

6.16.4 Other Transition Hardware

Other hardware which will be required during the transition are the current backend filter module T4 and the Baseband Driver Module T5. The T4 provides filtering of the final IF and the T5 provides amplification and automatic gain control of the IF.

6.17 Power Supplies

The power supply modules required are described in the Systems Chapter of the project book.