EVLA Project Book, Chapter 6

6 LO / IF SYSTEMS

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Last changed 2001-Jan-11

Revision History:
2001 -July-20: Initial Release

Summary

This chapter describes the LO/IF system for the Expanded Very Large Array (EVLA) Project. The requirements and specifications are presented for each part of the LO/IF system. Transition issues for making antennas with new electronics hardware compatible with antennas that have existing hardware is also discussed.

6.1 Introduction

The Very Large Array (VLA) was designed and built more than 20 years ago and since that time the need for a more sensitive instrument has arisen. The scientific requirements for a more sensitive instrument coupled with aging electronic equipment has lead to the much needed Expanded Very Large Array (EVLA) project. The EVLA project is designed to increase the overall system bandwidth by a factor of 80 and replace antiquated electronics with a new state of the art electronic system. The waveguide system will be replaced with a fiber optic system. The fiber optic system will transmit LOs to the antennas and receive digitized IFs from the antennas. The EVLA will contain new synthesizers, reference generators, IF converters, and digitizers, which are described in this document.

6.2 Specifications and Requirements

The specification and requirements for the LO/IF system are contained in this document. General specifications that apply to every piece of the system are contained in the first few paragraphs while the more specific requirements for each module are shown in paragraphs particular to that module. As a general rule, all specifications will be equal to or better than the specifications for the current VLA system.

6.3 Environmental

The nominal temperature of each bin/rack will be within the range of +18 to +22 °C and will not vary more than ± 1 °C from nominal in any given 24 Hr period. All equipment will be designed to meet all specifications over a temperature range of +10 to +30 °C, at an altitude of 12,000 ft., and humidity level ranging from 0 to 95%.

6.4 General Module Interface

Each module in the LO/IF system shall use OSP type connectors for RF ports < 22 GHz on the back panel. For back panel RF ports that may exceed 22 GHz then OSSP type connectors up to 28 GHz may be used or the appropriate screw type connector may be used, provided mechanical safety devices are used to prevent damage. Any RF ports on the front panel shall be either BNC or SMA type depending upon the frequency range.

Each module shall use a D type connector for all DC and low frequency connections. The D connector shall be sized as to not exceed 80% of the pins on the initial design.

6.5 LO Phase Stability

These specifications do not include phase instability induced by the antenna structure or the atmosphere. These specifications do include any instability induced in the front end by the LO system.

Short term: Less than 0.5 ps rms for times under 1 second.
(this would be 5% coherence loss at 100 GHz)

Long term: Linear slope over 30 minutes less than 6 ps.
(roughly 1/4 turn at 40 GHz)

Peak-to-peak phase deviations over 30 minutes less than 1.4 ps
after removal of any linear slope (20 degrees at 40 GHz).

Phase shift with pointing change:

Less than 0.7 ps over the whole sky (10 deg at 40 GHz).
Less than 0.07 ps per degree of slew for short slews at elevations
under 60 degrees (1 deg of phase at 40 GHz).

This specification applies after correction using any round trip and/or pulse cal data that might be available.

6.5.1 LO Phase Noise Allocation

The phase noise allocation is shown in Table 6.5.1. For each of the components shown, the phase noise is obtained by integrating the power spectral density over the appropriate bandwidth. The phase noise specification is determined by the type of component and its location.

Table 6.5.1 Phase Noise Allocation

Component	Specification (fs)	Notes
Reference	TBD	
Fiber distribution system	TBD	
1st LO	TBD	integrated over all frequencies
2nd LO	TBD	integrated over all frequencies
Master Reference Generator/distributor	TBD	for any reference frequency integrated from the PLL cutoff (if any) to infinity; Multipliers are integrated over all frequencies
Antenna Reference Generator	TBD	for any reference frequency integrated from the PLL cutoff (if any) to infinity; Multipliers are integrated over all frequencies

6.5.2 Phase Drift Allocation

Table 6.5.2 is a attempt to allocate the phase noise specification to various components of the system. It is likely that some of the components will be better than these allocations and some will be worse.

Table 6.5.2 Phase Drift Allocation

Component	Drift (degrees)/s	Notes
Round trip phase correction loop	TBD° @512MHz	
1st LO	TBD° @20GHz	
2nd LO	TBD° @12GHz	
Master LO Generator/distributor	TBD° @4GHz	
Antenna Reference Generator	TBD° @4GHz	
IF down/up converters	TBD° @max LO freq	per converter, does not include drift introduced by the LO

6.6 Fringe Tracking, Phase Switching, Sideband Suppression

Fringe rotation is required due a sinusoidal component introduced in the system caused by the rotation of the earth. This frequency is usually called the natural fringe frequency. The fringe frequencies are dependant upon baselines and observe frequencies. The fringe frequency can be canceled by introducing a continuous phase shift or frequency offset into one of the LOs used for down conversion. The fringe rotation will be removed using a direct digital synthesizer and its requirements are shown in Table 6.6. The calculations were based on equations derived by A. R. Thompson in EM #124.

Fringe rotation will take place in the correlator. However for the transition peroid from the old system to the new system, fringe rotation will be required at the antenna. Fringe rotation in the correlator is preferred due to lower RFI generation in the antennas.

Both the first and second LOs are required to support fringe rotation and 180d phase switching for the transition period. The phase switching is required to suppress spurious signals and d.c. offsets between the baseband down converter and the samplers. The hardware required to support 180d phase switching will also support 90d phase switching if needed for sideband suppression during the transition period.

Table 6.6 Fringe Generator Requirements

Item	Frequency range (min)	Frequency accuracy	Phase shift increment	update time	notes
Fringe Generator (Internal to the 1st and 2nd LO synthesizer)	±(0 to 5 KHz)	1 part in 10^6	1°	.46sec max	1

Notes: 1. Calculations are based on 86 GHz front ends and a “Los Alamos” baseline.

6.7 RFI

RFI emissions for all LO/IF equipment shall meet the requirements set forth in TBD.

6.8 Mechanical

All LO/IF modules shall be compatible with existing BIN hardware currently in use at the VLA.

6.8.1 General Module Monitor Requirements

All analog monitor points within each module, unless otherwise stated, will be implemented using SPIE bus technology.

6.9 Central Reference System

The central reference system (CRS) will take a signal from one of two reference standards and either divide or multiply this signal to generate various reference signals required by each antenna. The signals will be distributed to

each central fiber optic transmitting system through a central reference generator and distribution system. The primary reference standard will be a hydrogen maser and the secondary or backup reference standard will be a rubidium oscillator. The CRS in addition to generating reference frequencies will also track long term drift of the reference standards via a GPS receiver. System timing will be accomplished using a central timing generator and will be distributed to the fiber optic transmitting system. There will be a backup CRS rack to duplicate critical functions. The power for each CRS rack and the reference standards will be backed up with batteries. All critical functions of the CRS and the reference standards will be monitored by the online system.

6.9.1 Frequency Standards

There will be two frequency standards. The primary standard will be a hydrogen maser and the secondary or backup standard will be a rubidium oscillator. The principle performance requirements for the maser are shown in Table 6.9.1a while the rubidium requirements are shown in Table 6.9.1b. These standards will be purchased from external vendors.

Table 6.9.1a Principle performance requirements of the H-maser

Item	Requirement	Notes
LO-Ref max frequency error	1 part in 10^{12} averaged over 10 sec	
Wide-band phase noise at 5 MHz	1.4 psec RMS	see 6.5
Allen Variance	1<t<1000secs 2E-13t $^{-3/5}$ 1000<t<10,000secs 3E-15	

Table 6.9.1b Principle performance requirements of the Rubidium Oscillator

Item	Requirement	Notes
LO-Ref max frequency error	1 part in 10^{12} averaged over 10 sec	
Wide-band phase noise at 5 MHz	1.4 psec RMS	
Allen Variance	1 sec <5E-12 10 sec <1.6E-12 100 sec <5E-13 1000 sec <5E-13	

6.9.2 Timing Generator

The timing generator will take the 5 MHz from the reference standard and divide it down to 19.2 Hz and distribute it to the antenna backend and fiber optic transmitter system. The 19.2 Hz will be a TTL compatible signal and have a rise time of TBD ns with a duty cycle of TBD %. The jitter on the 19.2 Hz will be <TBD ns. The timing signal of 19.2 Hz will be changed after the transition period.

6.9.3 GPS Receiver

The GPS receiver will be purchased from an external vendor. The receiver will serve as the UTC time reference for the array. All clocks can be synchronized to the GPS, so that on a long term basis, the time at the array can be known within 100 nsec.

The GPS receiver will have a built-in or external time interval counter with a computer interface that will provide time offset and slope for the data analysts.

6.9.4 LO Ref Generator

The LO reference generator takes the reference standard frequency and multiplies it to the frequencies shown in Table 6.9.4. The specific requirements for each frequency is also shown in this table.

Table 6.9.4 Reference Generator Frequencies

Frequency MHz	Power Level dBm	Harmonically Related spurious signals dBc	Non-Harmonically Related spurious signals dBc	Phase noise degree rms to 10 MHz offset	location	Notes
5	+13	35	50	1.29x10E-3	reference output	phase noise to 2MHz offset
5	-6	35	50	1.29x10E-3	reference dist output	phase noise to 2MHz offset
100	+13	25	40	0.022	reference output	
128	+7				LO ref gen output	
256	+7	25	40	0.051	LO ref gen output	
512	+30				LO ref gen output	
512	+12				LO ref dist output	

6.9.5 LO Ref Distributor

The LO reference distributor shall take the reference signals of the LO reference generator and amplify them. These signals will then be divided either internally or externally and sent to the backend and fiber optic transmitter system of each antenna. The specific requirements for output frequencies are shown in Table 6.9.4.

6.10 First LO System

6.10.1 First LO Synthesizer

The First LO synthesizer provides the LO signals for the first down conversion. These signals are switched to the high frequency front ends or they are switched to an up converter for the low frequency front ends. The exception being the current Ku-band system which requires an external down converter. In the high frequency front ends, where necessary, the synthesizer frequency is either doubled or tripled. The synthesizer is YIG based and designed for low noise, phase continuous operation**.** This synthesizer will have an integral direct digital synthesizer (DDS) to provide fine tuning for fringe rotation and phase switching. There will be two First LO synthesizers in each antenna.

The synthesizer has the following performance specifications:

Output Frequency	12 to 20 GHz
Output Frequency Steps	N*512MHz ± DDS
Output Power	+13 dBm ±.5 dB Nominal and Adjustable
Output Spurious signal level	<-70 dBc except for harmonics of ref
Output harmonics of Ref	<-80 dBc
Phase Noise	-107 dBc/Hz @100KHz, -90 dBc/Hz @ 10KHz
Harmonics	<-40 dBc
Output VSWR	<2:1
RF port impedances	50 ohm
Lock time	1 sec max between any two frequencies
Supply voltages	Voltage Current +24 50ma max with 1A surge at turn on ±18 1.5 amps each max +5 2 amps max
Power Dissipation	50 watts max
Monitor Points	Synthesizer freq 1MHz Resolution Synthesizer output power Direct Digital synthesizer power Lock condition FM tuning voltage/current Main coil voltage Power supply voltages Yig Heater Current Module Temperature
Synthesizer out to ref in isolation	<-40 dBc
Rear Panel connections	19.2 Hz in: with <TBD ns of Jitter on rising Edge 512MHz comb in with following noise: TBD TBD interface bus Ref in: noise of ref: TBD Synthesizer out

	Power supply voltages
Front panel requirements	Frequency display to 1 MHz Res
	BNC output of fine tune syn
	SMA output of 256 MHz ref
	BNC output of FM tune voltage
	Lock condition indicator
DDS output	128MHz @+10 dBm
	Noise: >-140dBc @100KHz

6.11 Second LO System

6.11.1 Second LO Synthesizer

The second LO synthesizer provides the last LO for down conversion of the astronomical data before digitization occurs. This is a YIG based synthesizer designed for low noise, phase continuous operation**.** This synthesizer will have an integral direct digital synthesizer (DDS) to provide fine tuning for fringe rotation and phase switching. There will be four second LO synthesizers in each antenna.

The synthesizer has the following performance specifications:

Output Frequency	11 to 15 GHz nominal
Output Frequency Steps	N*128MHz ± DDS
Output Power	+13 dBm ± 0.5dB Nominal Adjustable
Output Spurious signal level	<-70 dBc except for harmonics of ref
Output harmonics of Ref	<-80 dBc
Phase Noise	-108dBc @100KHz, -87dBc@10KHz
Harmonics	<-40 dBc
Output VSWR	<2:1
RF port impedances	50 ohm
Lock time	1 sec max between any two frequencies
Supply voltages	Voltage Current
	+24 50ma max with 1A surge at turn on
	±18 1.5 amps each max
	+5 2 amps max
Power Dissipation	50 watts max
Monitor Points	Synthesizer freq 1MHz Resolution
	Synthesizer output power
	Direct Digital synthesizer power
	Lock condition
	FM tuning voltage/current
	Main coil voltage
	Power supply voltages
	YIG Heater current
	Module temperature
Synthesizer out to ref in isolation	<-40 dBc
Rear Panel connections	19.2 Hz in: with <TBD ns of Jitter on rising

	Edge
	128 MHz comb in with following noise:
	TBD
	TBD interface bus
	Ref in: noise of ref:
	TBD
	Synthesizer out
	Power supply voltages
Front panel requirements	Frequency display to 1 MHz Res
	BNC output of fine tune syn
	SMA output of 100 MHz ref
	BNC output of FM tune voltage
	Lock condition indicator
DDS output	128MHz @+10 dBm
	Noise: >-140dBc @100KHz

6.11.2 Fringe Generator

The fringe generator uses direct digital synthesis techniques to achieve its high frequency and phase resolution. The device is based on the Analog Devices AD9852 DDS integrated circuit. The AD9852 provides the infrastructure to obtain very sophisticated control over its output. Below is a short discussion of the features of the device that apply to the fringe generator.

The DDS contains a 48 bit digital phase accumulator which is truncated to 17 bits. This 17 bit phase word is then converted to a 12 bit sine function which drives a high speed Digital to Analog Converter (DAC). There is a programmable 48 bit frequency accumulator. At each system clock cycle, 256MHz in this application, the frequency accumulator contents are added to the phase accumulator. The result is that any frequency between DC and half the clock frequency can be generated to a resolution of sub micro hertz. In the fringe generator the lower frequency limit is established at about 8 MHz by the output coupling transformer.

There is a programmable 48 bit delta frequency word register. At each system clock cycle, the contents of this register are added to the frequency accumulator. This results in an FM chirp signal.

The DDS contains a programmable 14 bit phase offset register. The contents of this register are added to the contents of the 48 bit phase accumulator before conversion to the sign function. This register is used to produce the ± pi/2 and ±pi/4 phase switching needed in the LO system.

This phase accumulator can be reset to zero on command. This, along with the two programmable frequency control registers, allow the approximation of any desired phase profile function modeled by a polynomial with up to two coefficients in the hardware. Along with the 14 bit phase offset word, an arbitrary initial condition can be obtained with up to fourteen bit resolution. Movement to a new function with different coefficients can be accomplished in a single system clock cycle. The primary limitations are the time required for the micro controller to load the required parameters into the DDS registers and the settling time of other components in the LO synthesizer.

The DDS has an 8 bit data bus. I/O registers are loaded through this bus a byte at a time. This is a 6 bit address bus which identifies which register is to be loaded. When all I/O registers are loaded, an I/O update pulse is issued to the

DDS to cause all data in the I/O registers to be loaded to the DDS active core on a single system clock edge. There is a system pipeline delay of 17 clock cycles, from the first clock edge after the I/O update, until the time these parameters take effect. They all take effect immediately on that clock edge.

Except for the case of a reset to the DDS, the output is always phase continuous, i.e., the phase of the start of a new phase function begins where the previous one was at the time the new parameters take effect. This defines the phase offset register contents as part of the desired phase function.

The output of the DDS is a zero order hold sampled sine wave at the programmed frequency and phase.

All system timing events within the VLA are synchronized to a 52 millisecond fiducial which is distributed throughout the array. The DDS uses this signal to synchronize its activities with the rest of the array. There is a large Field Programmable Gate Array (FPGA) in the fringe generator which derives the necessary timing signals from the 52ms tick and the system clock. This FPGA contains a set of counters and state decoding logic to derive the I/O update signal for the DDS and interrupts to the micro controller to keep all parts of the fringe generator synchronized. This FPGA is a Xilinx Vertex series XCV50.

Supervision of the over all module is performed by a Motorola MC68HC16 series micro controller. The micro controller receives data through a communication link to an AMB interface board. Commands received are interpreted and the data prepared for loading into the DDS. The DDS registers are mapped into the micro controller memory space.

The board interface is yet to be defined.

One of the Analog to Digital (A/D) channels of the micro controller is connected to the 5 volt power supply through a voltage divider to monitor module input power. Three more of the A/D channels are connected to external monitor points provided as inputs to the module.

External Connections
1. 5VDC power, .5amp nominal
2. Power return. Connected to case
3. 128 MHz clock input, sine wave, terminated with 50 ohms.
4. 52 ms reference LVDS, terminated with 100 ohms.
5. Output, 50 ohm impedance, +9 dBm
6. 3 external monitor inputs
7. Interface bus

6.12 Antenna Reference System

6.12.1 Antenna LO Reference Generator

The Antenna LO reference generator takes the reference frequencies which were transmitted on the fiber link and cleans them up where necessary. The Antenna Reference Generator also multiplies or divides the reference frequencies from the fiber link to frequencies required by the antenna LO system. These frequencies are shown in Table 6.12.1. The specific requirements for each frequency are also shown in this table.

Table 6.12.1 Antenna Reference Generator Frequencies

Frequency MHz	Power Level dBm	Harmonically Related spurious signals dBc	Non-Harmonically Related spurious signals dBc	Phase noise degree rms	location	Notes
9.6Hz					Ant LO ref gen output	
19.2Hz					Ant LO ref gen output	
128					fiber receiver	
128					Ant LO ref gen output	
256					Ant LO ref gen output	
512					fiber receiver	
512					Ant LO ref gen output	
1024					Ant LO ref gen output	
2048					Ant LO ref gen output	
4096					Ant LO ref gen output	
5120					Ant LO ref gen output	

6.12.2 Antenna LO Reference Distributor

The Antenna LO reference distributor shall take the reference signals of the Antenna LO reference generator and amplify them. These signals will then be divided either internally or externally and sent to various LO/IF modules within the antenna. The specific requirements for output frequencies are shown in Table 6.12.1.

6.13 PCAL Generator

The PCAL generator is a module that produces a wideband comb signal with selectable 1 MHz or 5MHz spacing for low frequency front ends and TBD spacings for high frequency front ends that can be used to calibrate an antenna RF/IF signal path in amplitude and phase. The critical specifications for the PCAL generator are shown in Table 6.13.

Table 6.13 PCAL Specifications

Item	Requirement	Notes
Warm-up Drift	20 psec	
Voltage sensitivity	5 psec/volt at 15V	
Input level sensitivity	<5 psec/dB	
Temperature sensitivity	~ 1 psec/^{o}C	

6.14 Intermediate Frequency System

The intermediate frequency system selects the four IFs from one of ten different front ends. The selection occurs through mechanical band switches. Some front ends are designed with built in converters and they will deliver IFs in the 8 to 12 GHz range. Other front ends need to be either up converted or down converted externally to the 8 to 12 GHz range. The IFs that need to be externally converted use the same 1st LO synthesizer as the front ends that are internally converted. The 8 to 12 GHz IFs are then switched into the baseband down converters. The baseband down converter takes the 8 to 12 GHz IFs, performs total power detection and either a single or double down conversion. The IFs out of the baseband down converter are either 2 to 4 GHz or the range of 1 to 2 GHz. The lower frequency path is provided for narrow band lower frequency front ends. The output of the baseband down converter is switched into the digitizers. There are two digitizers provided. One is a 2 to 4 GHz 4GS/s 3 bit digitizer. This digitizer is used for high frequency front ends. The second is a 1 to 2 GHz 8 bit digitizer that is used for the low frequency front ends. The sampler clock will be 2048 GHz. The digitized IFs are then modulated onto the fiber optic system.

6.14.1 Band Switches

There will be two sets of four band select switches (one switch per IF). These switches are used to select the IFs from the different front ends. One set of switches is used to select the 8 to 12 GHz IFs and are specified in Table 6.14.1a. The other set is used to select the 1 to 8 GHz IFs and is specified in Table 6.14.1b. The switches will be controlled through a DCS interface module.

Table 6.14.1a 8-12 GHz Band Switch Specifications

Item	Specification	Notes
Frequency Range	8 to 12 GHz	
VSWR	1.4 to 1 Max	
Insertion Loss	.4 dB Max	
Isolation	60 dB min	
Input impedance	50 Ohm nominal	
Actuating Voltage	+28 V	
Actuating Current	177 mA	
Switching Time	15 ms max	
# poles	1	Per switch
#throws	9 min	Per switch
RF connection	SMA	
Power Connector	TBD	

Table 6.14.1b 1 to 8 GHz Band Switch Specifications

Item	Specification	Notes
Frequency Range	1 to 8 GHz	
VSWR	1.3 to 1 Max	
Insertion Loss	.3 dB Max	
Isolation	70 dB min	
Input impedance	50 Ohm nominal	
Actuating Voltage	+28 V	
Actuating Current	177 mA	
Switching Time	15 ms max	
# poles	1	Per switch
#throws	6 min	Per switch

RF connection	SMA	
Power Connector	TBD	

6.14.2 Transfer Switches

After the IFs are selected with the Band Select switches, then the IFs go through a set of 2 IF transfer switches. These transfer switches allow the IFs to be transferred to a different IF down converter**.** These switches are used to reverse the IF polarization. These switches are specified in Table 6.14.2.

Table 6.14.2 IF Transfer Switch

Item	Specification	Notes
Frequency Range	DC to 12 GHz	
VSWR	1.4 to 1 Max	
Insertion Loss	.4 dB Max	
Isolation	60 dB min	
Input impedance	50 Ohm nominal	
Actuating Voltage	TBD	
Actuating Current	TBD	
Switching Time	20 ms max	
# poles	2	Per switch
#throws	2	Per switch
RF connection	SMA	
Power Connector	TBD	

6.14.3 Converter Modules

6.14.3.1 4/P-Band to L-Band Converter

The 4/P-Band to L-Band converter module is used to convert either the 74 MHz front end and the P-Band front end to L-Band. Power dividers are used at the input to allow dichroic observations. The corresponding IFs for 4-Band and P-Band are diplexed together. Each IF is up converted with the same fixed LO. The specifications for this converter are shown in Table 6.14.3.1.

Table 6.14.3.1 4/P-Band Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	4	
Input frequency range	70 to 976 MHz	
Input power level per IF per GHz	TBD	
Variation of power spectral density	TBD	
Headroom	TBD	
# of LOs per module	1	1 fixed
Frequency range of LO	1.024 GHz fixed	
Power Level of LO	TBD	
Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	1.094 to 2 GHz	
Power Level of output	TBD	
Headroom	TBD	
LO 2nd harmonic spur and leakage	TBD	
IF input VSWR	TBD	
IF input noise figure	TBD	
Image rejection	TBD	
Overall flatness	TBD	
Phase/delay stability	TBD	
Isolation between channels	TBD	
Total power detector response time	TBD	
TBD linearity		

Interface	TBD	
M&C requirements	TBD	

6.14.3.2 U-Band to X-Band Converter

The U-Band to X-Band converter is used to down convert Ku-Band to X-Band. This converter takes the 1ST LO and internally doubles for the conversion process. This converter will no longer be needed once the new Ku-Band receivers are installed so hardware should be chosen so it can be reused in the new receivers. The specifications for this converter are shown in Table 6.14.3.2.

Table 6.14.3.2 U-Band to X-Band Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	4	
Input frequency range	12 to 18 GHz	
Input power level per IF per GHz	TBD	
Variation of power spectral density	TBD	
Headroom	TBD	
# of LO per module	2	internally doubled
Frequency range of LO	12 to 20 GHz	
Power Level of LO	TBD	
Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	8 to 12 GHz	
Power Level of output	TBD	
Headroom	TBD	
LO 2nd harmonic spur and leakage	TBD	
IF input VSWR	TBD	
IF input noise figure	TBD	
Image rejection	TBD	

Overall flatness	TBD	
Phase/delay stability	TBD	
Isolation between channels	TBD	
Total power detector response time	TBD	
TBD linearity		
Interface	TBD	
M&C requirements	TBD	

6.14.3.3 L/S/C-Band to X-Band Converter

The L/S/C-Band to X-Band Converter module is used to convert the lower frequency front ends to X-Band. This converter uses the 1ST LO for the conversion process. The specifications for this converter are shown in Table 6.14.3.3.

Table 6.14.3.3 L/S/C-Band to X-Band Converter Specifications

Item	Specification	Notes
Number of modules	32	1 per antenna + 4 spares
# of IF inputs per module	4	
Input frequency range	1 to 8 GHz	
Input power level per IF per GHz	TBD	
Variation of power spectral density	TBD	
Headroom	TBD	
# of LO per module	2	
Frequency range of LO	12 to 20 GHz	
Power Level of LO	TBD	
Spurious levels of LO	<-70 dBm for spurious, <-80 dBm for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	4	
Frequency range of output	8 to 12 GHz	
Power Level of output	TBD	
Headroom	TBD	

LO 2nd harmonic spur and leakage	TBD	
IF input VSWR	TBD	
IF input noise figure	TBD	
Image rejection	TBD	
Overall flatness	TBD	
Phase/delay stability	TBD	
Isolation between channels	TBD	
Total power detector response time	TBD	
TBD linearity		
Interface	TBD	
M&C requirements	TBD	

6.14.4 IF Down Converter

In each antenna there will be four IF down converter modules, one per IF. The IFs are in the to 8 to 12 GHz range and total power detection and leveling are performed on the full range IF. These IFs are then split in two inside each module. These two IFs are down converted with the 2ND LO and the resultant IFs are in the passband from 2 to 4 GHz. Another conversion is provided for low band signals that may require higher resolution digitizers due to higher levels of RFI.. This conversion uses a fixed 4.096 GHz LO and is used only on one of the split 8 to 12 GHz IFs. This lower passband is from 1 to 2 GHz. The eight 2 to 4 GHz IFs from the four down converters will be harmonic sampled by 3-bit 4 GS/s digitizers. The four lower frequency IFs will be harmonic sampled by 8-bit 2 GHz digitizers. The input and output noise power spectral distribution will be nominally flat over the passband. The down converter module provides for total power measurement of each split IF as well as the total IF. Internal filters and external filter connections will be provided to either narrow the desired passband or notch out undesired areas within the passband. The specifications for the down converter are shown in Table 6.14.4.

Table 6.14.4 IF Down Converter Specifications

Item	Specification	Notes
Number of modules	124	4 per antenna + 12 spares
# of IF inputs per module	1	
Input frequency range	8.5 to 12.5 GHz	
Input power level per IF per GHz	-45 dBm	
Variation of power spectral density	±1.5 dB	
Headroom	>20 dB	

# of LO per module	3	2 independently tunable, 1 fixed
Frequency range of LO	10.6 to 14.6 GHz and 4.096 GHz fixed	
Power Level of LO	+10 dBm	
Spurious levels of LO	<-70 dBc for spurious, <-80 dBc for harmonics related to any ref frequency, <-40 dBc for harmonics	
# of IF outputs per module	2	
Frequency range of output	2- 2 to 4 GHz, or 1- 0 to 2 GHz	
Power Level of output	TBD	
Headroom	>20 dB	
LO 2nd harmonic spur and leakage	<-40dBc	
IF input VSWR	1.25:1 Max	
IF input noise figure	<12 dB	
Image rejection	>25 dB	
Overall flatness	2 dB/200 MHz	smooth variations only
Phase/delay stability	TBD	
Isolation between channels	>70 dB	
Total power detector response time	TBD	
Phase linearity	<2.8nsec/2 MHz	
Interface	TBD	
M&C requirements	TBD	

6.15 Samplers

6.15.1 2-4 GHz Sampler

The analog-to-digital converters, or digitizer, or samplers, installed in the antennas provide the flexibility required for the fiber optic transmission of the IF. Digital conversion is of course indispensable to the correlator in order to derive the correlation function as a function of lags for spectroscopy. The digitizers are thus crucial and single-point-failure elements in the system. The EVLA will incorporate 3-bit digitizers thus improving the overall sensitivity compared to the 2-bit correlator. The specifications for the samplers are given in Table 6.15.1.

Table 6.15.1 2-4 GHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	2-4 GHz	
Clock Rate	4096 MHz	
Resolution	3 bits	
Quantization	8 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/16	
Distribution clock	TBD	
Power Consumption	TBD	

The sampler includes several fundamental elements briefly described below. The input adapter amplifier, the comparators and the associated latches and encoding are implemented in a single ASIC. The fast demultiplexing unit is separate from the ASIC to diminish any coupling of the digital output with the analog signal input. The ASIC and the demultiplexing unit form the digitizer proper. A PLL box produces and distributes the sinusoidal 4096 MHz sampling clock and the TBD signal required by the demultiplexing unit. This is another separate unit which will be common to at least one sampler pair.

Input Adapter Amplifier
The analog signal is delivered from one of the four output of the IF down converter modules in the 2 to 4 GHz range. It is random with Gaussian statistics. The response of this amplifier is flat within ± .5 dB over 2 GHz bandwidth and linear up to about +15 dB above R.M.S. input signal range. The voltage supply required for the adopted ASIC technology is ± 1.25 V.

The digitizer input level is controlled in the IF down converter with ±.25 dB attenuators placed in the 2-4 GHz output paths of each IF down converter. This allow minimization of platforming effects and keeps the quantization thresholds constant and at their optimum level for maximum quantizing efficiency.

Comparators and Quantization Thresholds
The sampling function is preformed in the comparators which include two latches operated in a master-slave configuration and clocked at 4096 MHz. The 4096 MHz clock signal is equally distributed to 7 comparators. It's

shaped internally in a dedicated amplifier driven by the external 4096 MHz sinusoidal signal. The seven thresholds comprise a zero reference voltage and are set around ±0.5 'sig', 1 'sig' and 1.5 'sig', where 'sig' is the R.M.S. voltage at the common input of the 7 comparators; these levels are kept constant and their exact value is tuned with an accurate division voltage chain so as to minimize the quantization losses. First simulations of SiGe digitizers indicate that the sampler indecision region is small and at the level of 1% of the smallest comparison threshold.

Encoding
The digitizer encoding is not yet finally adopted.

6.15.2 1-2 GHz Sampler

In addition to the 2-4 GHz sampler, a lower frequency higher resolution sampler is required. Due to higher RFI in L-Band, an 8-bit sampler will be needed. A higher number of bits allows more dynamic range and allows the correlator to better filter unwanted RFI. This sampler will be used for either harmonic or bandpass sampling, where the IF to be sampled is in the region from 1000 to 2000 MHz. The specifications for this sampler are shown in Table 6.15.2.

Table 6.15.2 750-1500 MHz Sampler Specifications

Item	Specification	Notes
Input Bandwidth	2000 MHz	
Clock Rate	2048 MHz Max	
Resolution	8 bits	
Quantization	256 levels	
Aperture time	50 ps	
Jitter	TBD ps	
Rise time	TBD ps	
Output demultiplexing factor	1/8	
Distribution clock	256 MHz	
Power Consumption	TBD	

6.16 Transition Hardware

There will be special hardware necessary to keep the new electronics compatible with the old correlator. This hardware is necessary since the new correlator in not expected to be in place until most antennas are modified with the new electronics**.** This new hardware consists of a lower frequency sampler, a digital decimator for frequency conversion, a digital to analog converter for conversion back to an analog IF, and the current baseband filter and driver modules, T4 and T5. At this point, digital decimation is the baseline plan, however; decimation may cause unwanted signal to be aliased into the bandpass. Tests are planned to check on this problem.

6.16.1 Transition Sampler

The sampler used to keep the new electronics compatible with the old correlator is to be the same sampler in 6.15.2. The only difference is that the sampled digital data will be decimated. This decimation will digitally down convert the IF to be compatible with the IF scheme of the current VLA.

6.16.2 Transition Converter

The transition converter consists of a digital decimator and a digital to analog converter. The decimator down converts the signal that was in the 1152 to 1216 MHz range to a signal that will end up in the 0 to 64 MHz range. The 1152 to 1216 MHz was chosen because of clock frequencies. The decimator clock will be 256 MHz allowing both sidebands of the IF to appear at multiples of the 128 MHz. A field programmable gate array FPGA integrated circuit will be used to implement the digital decimator and to select the sideband of the signal depending upon whether or not spectral inversion is required. The final digital signal will then be fed to a digital to analog converter. The digital to analog converter needed for the transition is specified in Table 6.16.2. This D to A converter is necessary to reconstitute the digital data to analog form for the old correlator. The FPGA circuit configuration required for the digital down conversion cannot not be specified at this time.

Table 6.16.2 Transition Digital to Analog Converter

Item	Specification	Notes
Update rate	256 MHz	
Resolution	8 bits min	

6.16.4 Other Transition Hardware

Other hardware which will be required during the transition are the current backend filter module T4 and the Baseband Driver Module T5. The T4 provides filtering of the final IF and the T5 provides amplification and automatic gain control of the IF.