

EVLA Correlator

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National Research Council
Canada

Conseil national de recherches
Canada

NRC · CNRC



Outline

1. Funding
2. Review of Key Correlator Capabilities
3. Technical Progress
4. Project Progress
5. Review of Cost, Schedule and Risks

Funding in Canada - Approved

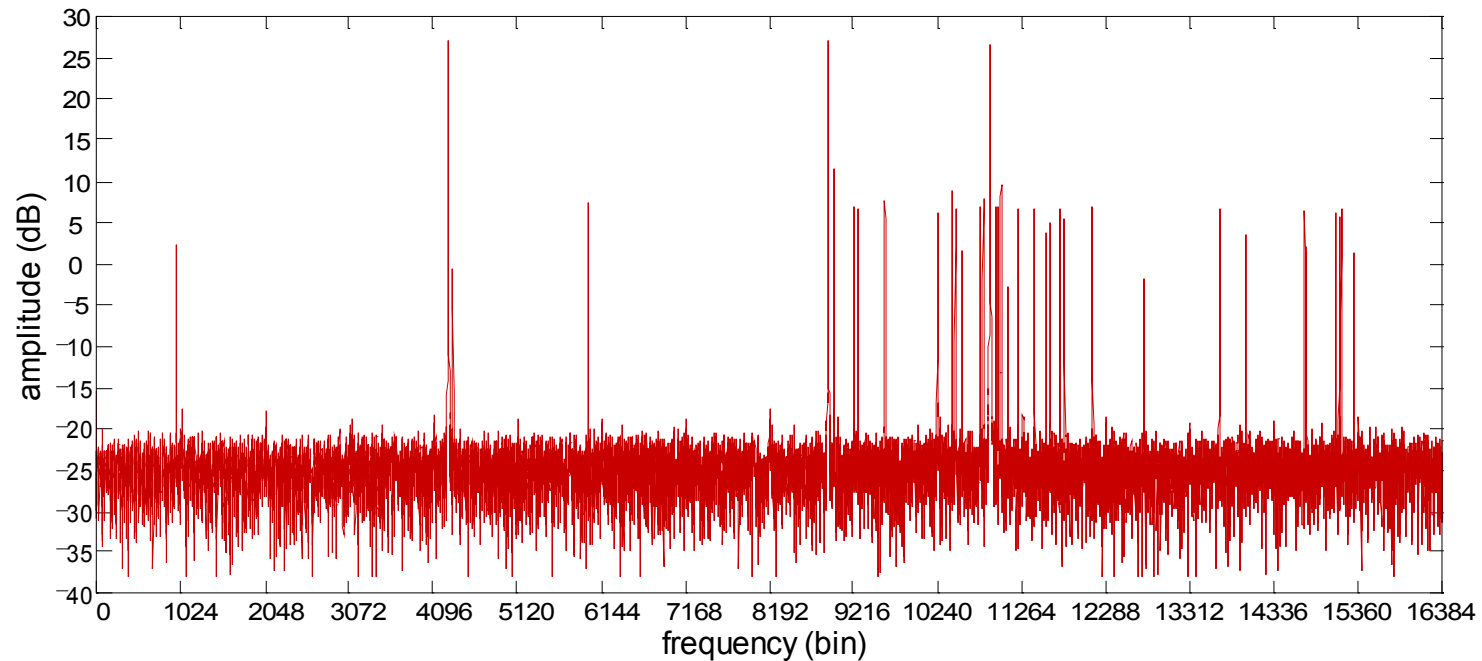
- Original funding request through Canada Foundation for Innovation (CFI) turned down.
- Direct gov't funding to National Research Council (NRC) announced in Canadian Federal Budget in March/03 for 2 years.
- April/03 Treasury Board submission drafted.
- July/03 – funding officially extended to 5 years.
- Aug/03 – Treasury Board approval of submitted budget (\$C 20M over 5 years).

Key Correlator Capabilities

Raw Bandwidth, Large No's of Channels

- **16 GHz** bandwidth per antenna in 2 GHz analog basebands. (8 x 2 GHz)
- **16384 spectral channels** at widest bandwidth over the 16 GHz.
- Targetable sub-band feature:
 - provides flexibility. Can trade off:
 - bandwidth for spectral resolution.
 - polarization modes for spectral resolution.
 - bandwidth for more antennas
 - bandwidth for delay centers (“beams”) (phased VLA)

Example 16000 ch. Spectrum



Key Capabilities

Flexible Configuration Trade-offs

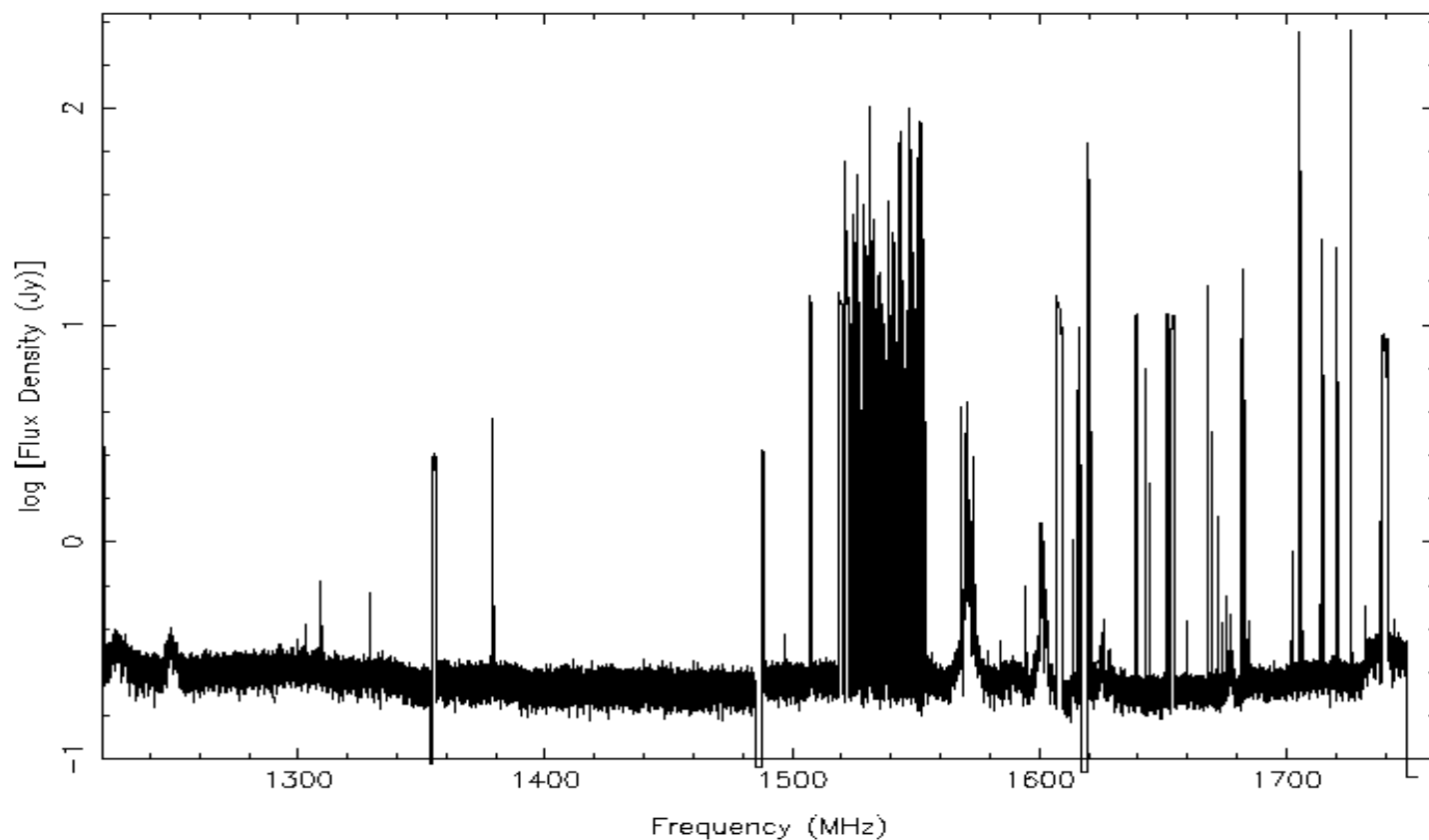
- Reconfigurable, expandable architecture.
 - Can trade antennas for bandwidth.
 - 32 stations input, expandable to 40.
 - EVLA Phase II will add ~8 antennas.
 - Local VLBA antennas will bring sum to 40.
 - physical infrastructure for expansion to 48.
 - VLBA/VLBI capable.
 - Growth path to include tape-based or real-time VLBA antennas (“two correlators for the price of one”).
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Key Capabilities

High Spectral Dynamic Range

- 4-bit/8-bit correlation
 - 4 bits are used internally, antennas deliver 3-bit data.
 - 8-bit mode can be used at lower frequencies where the trade for bandwidth is cost-free.
 - High spectral dynamic range for very bright lines & **interference robustness**.
- The ability to avoid narrow spectral regions which are not of interest, or have the potential to be especially damaging.

Interference Spectrum (single ant.)



Key Capabilities

Pulsar “Phase” Bins, Rapid Dumping

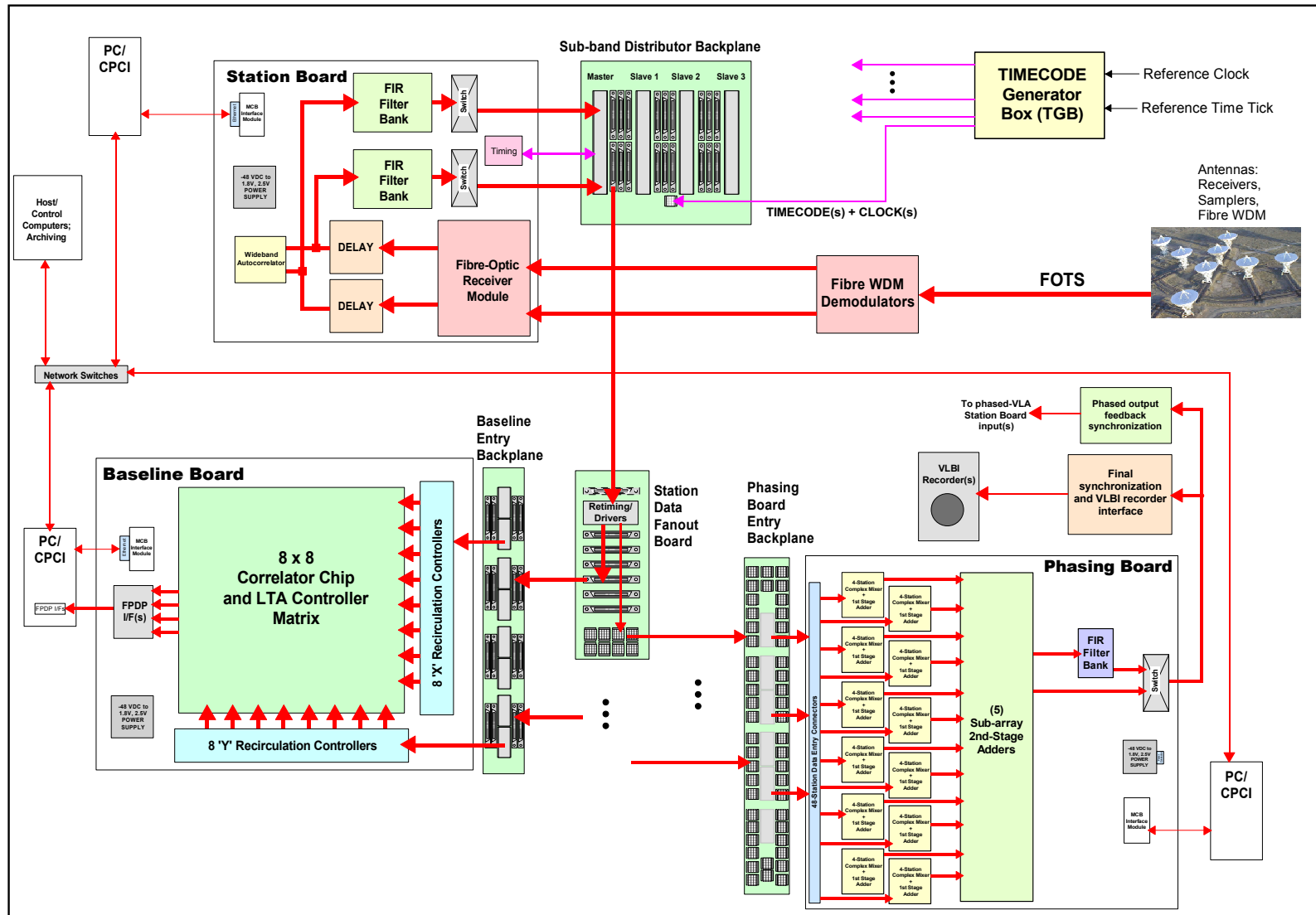
- Two banks of 1000 narrow phase bins per cross-correlation result for pulsar observations.
- Dump time resolution down to ~ 20 us.
- good frequency resolution.

Key Capabilities

“Single-dish” Capability, Sub-Arrays

- All digital **phased-VLA** sum (quasi-single dish mode) for VLBI and pulsar observing.
- Multiple sub-arrays.
 - E.g. Split array into two parts
 - use one part in phased-sum mode for real-time VLBI with VLBA and New Mexico antennas.
 - Use the other part in interferometry mode for another program.

EVLA Correlator System Diagram



Station, Correlator & Phasing Boards

- Most of the design work is in a few key areas.
 - Station board
 - FIR chips & Delay module chips are the major items.
 - About 8 other designs which are much smaller.
 - Board, itself, not expected to be especially challenging.
 - Correlator board
 - Correlator chip & recirculation memory chip are the major items (75%).
 - Long-term Accumulator (LTA) much smaller design.
 - Board, itself, is expected to be very challenging.
 - Phasing board
 - Lower priority at present – no work as yet.

New Station Board Features

1. Radar Mode: Software output available with some buffering (see project book).
2. Individual sub-band delays available (32 μ s at the highest data rate).
3. Standard VSI interfaces for VLBI
 - Saves optical switch in front of station boards for VLBI recorders.
 - Provides 2 input and 2 output interfaces, each 32 bits x 256 MHz clock rate (e.g. 4 Gsamples/s @ 2 bits per input).
4. Staged FIR filter with SSB digital mixer after 1st stage.
 - Permits arbitrary placement of narrower bands within a sub-band at the expense of reduced stitching performance.
 - Yet more choices for the observer . . .

Station Board Progress

1. FIR chip

- FPGA design is complete
- Tests of individual components has been carried out all along.
- Feasibility testing for implementation as FPGA is close but not quite complete.
- Feasibility as gate array is more or less assured.

2. Delay Module

- FPGA “heart” of module is complete and tested.
- Circuit board at the point of prototype fabrication.
- This board is the guinea pig for Mentor Graphics S/W package => learning curve issues.

3. Overall Board Design

- Basic form factor and layout has been worked out.

Correlator Board Progress

1. Correlator chip

- ‘C’ Simulator – reference for functional performance of digital hardware.
- Lots of testing done – graphical tool developed for test case generation and verification.
- Bit-level comparison of multiplier-accumulator (MAC) with behavioural simulator.
- Digital design complete.
- Manufacturers feasibility testing
 - Using our “testbench” test vectors.
 - 4 million gates with 2048 lags.
 - 0.18 μm technology \Rightarrow 2.75 watt.
- Planning to let contract in about 6 months for prototype chip production.

Correlator Board Progress (cont'd)

2. Recirculation Controller

- Design complete.
- Feasibility as FPGA secure (“place & route” at speed is done).
- Can do 4 independent streams.
- Test bench complete – debugging functionality is in progress.

3. Correlator circuit board

- Very crowded with signals (e.g. 90 wires from each recirculation controller to a row or column of corr. chips).
- Synchronization plan put forward by Dave Fort will alleviate earlier concerns with clock distribution.
- Preliminary sketches and ideas for layout are extant.

Correlator Software Progress

- People
 - Hired software specialist, Sonja Vrcic in April/03.
 - Two other Correlator Group S/W people at NRAO (Bruce Rowan – part time & Tom Morgan).
- Group working on S/W requirements, overall design, and scope of work (S/W WBS).
- Draft interface spec. document on Virtual Correlator Interface (VCI)
 - VCI defines boundaries of Correlator Group S/W deliverables.
- Catch-up work needed in software, especially documentation.

Project Management Work

- Define Work Breakdown Structure (WBS)
 - What has to be done?
 - What has to be first, next, etc. (linkages)
- Estimate amount level of effort for each task.
- Obtain parts list and cost estimates.
- Develop schedule and tracking schemes.
- Develop integrated project tracking system (integrated WBS/Schedule/Cash flow).

Project Management Progress

- Preliminary WBS, schedule, and cost estimate has existed since 2001.
- Hired full-time person (Amy Fink) as of Sept 1/03.
- WBS – mostly defined, except for some software tasks.
- Level of effort estimation – near term tasks are done.
- Parts list and costs are still preliminary, but a few key components are being actively tracked (e.g. correlator chip).
- Integrated tracking system is still not done – targeting mid Oct/03.

Figure 1



EVLA Project WBS

HARDWARE (1)

Hardware Design (1.1)

Station Design (1.1.1)

Station Board (1.1.1.1)

Station Board Fibre
Optic Receiver
Module
(1.1.1.1.1) ☒

Station Board PCB
Design [BDP]
(1.1.1.1.2) ☒

Delay Module PCB
Design [BDP]
(1.1.1.1.3) ☒

Input FPGA [FDP]
(1.1.1.1.4) ☒

Delay FPGA [FDP]
(1.1.1.1.5) ☒

Autocorr FPGA
[FDP]
(1.1.1.1.6) ☒

Filter FPGA [FDP]
(1.1.1.1.7) ☒

Output FPGA [FDP]
(1.1.1.1.8) ☒

Decode FPGA [FDP]
(1.1.1.1.9) ☒

Timing FPGA [FDP]
(1.1.1.1.10) ☒

Record FPGA [FDP]
(1.1.1.1.11) ☒

Playback FPGA
[FDP]
(1.1.1.1.12) ☒

Station Board Power
Supply Design
(1.1.1.1.13) ☒

Station Board
Mechanical Design
(1.1.1.1.14) ☒

Final Station Board
Design Review
(1.1.1.1.15) ☒

Produce Bill of
Materials for Station
Board
(1.1.1.1.16) ☒

Station Board
Assembly Notes
(1.1.1.1.17) ☒



Check mark indicates WBS Dictionary form has been created and at least partially filled out.



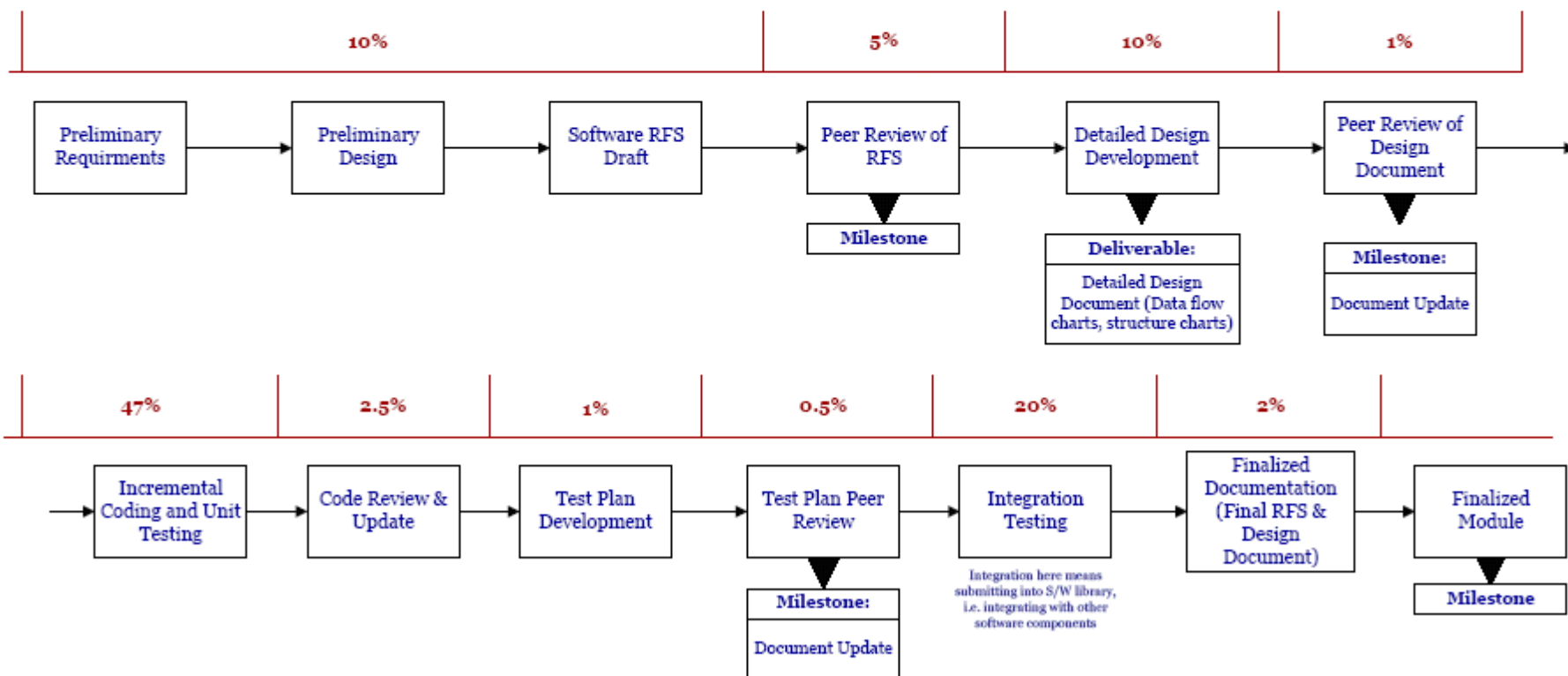
Shaded box indicates task is complete.
(Note: shade colours will differ)

Example of WBS
Hierarchy Detail – Station
Board Hardware Design

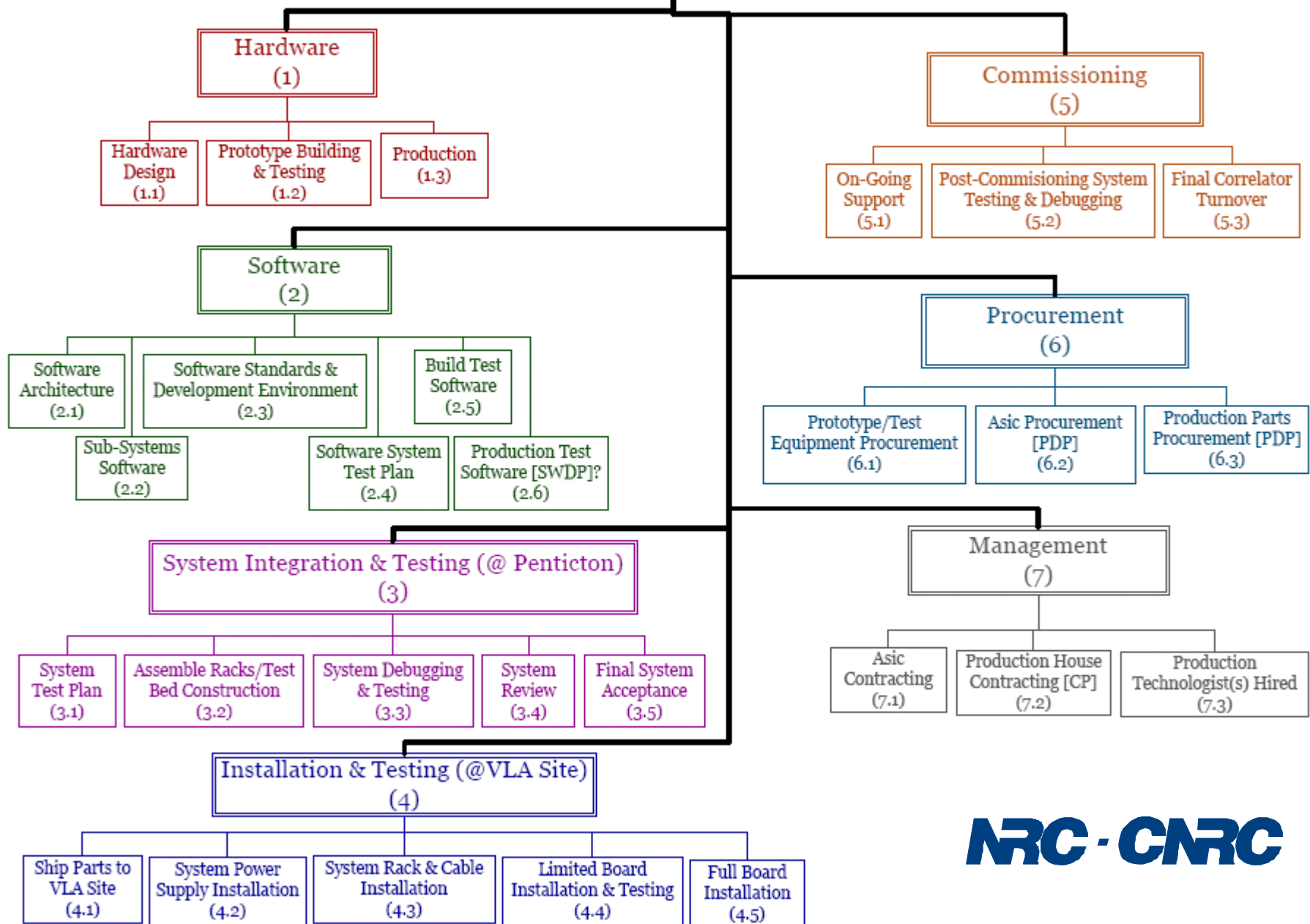
SOFTWARE MODULE DEVELOPMENT PROCESS - CYCLE OF WORK

Things to be completed before you can begin cycle of work:

- * Software Project plan to level of detail equivalent to hardware plan.
- * Preliminary software system architecture (Memo 15)
- * Hardware architecture (Memo 14)
- * OS, Software tools, compiler.
- * Setting revision control system and coding standards



EVLA Project WBS



EVLA Project

Work Breakdown Structure Dictionary

ID:	44	WBS Code:	1.1.2.1.2	Name:	Baseline Board PCB Design [BDP]
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Description:

- Schematic capture, PCB PAR, signal integrity analysis and timing analysis of the baseline board

Assumptions:

- It is possible to do this as currently envisioned
- Everything will fit onto a 12Ux400mm PCB, with maximum thickness of 0.125", number of layers <= 24
- 0.005" trace and clearance thickness, ok.
- There is some way to deal with the large insertion force from all of the connectors
- Double-sided BGA is ok

Deliverables:

- Finished schematic, timing analysis, signal integrity analysis
- RFS document
- PCB Gerber file
- User Manual
- Bill of Materials
- Assembly/production notes
- Test plan
- Design manual

Risk Identification:

- We have never designed and built a PCB of this complexity and speed before
- May take too many layers to route
- Double-sided BGA mount may not work as planned (the full-back position is to have one LTA controller for every 4 correlator chips, instead of one per correlator chip)

Linkages:

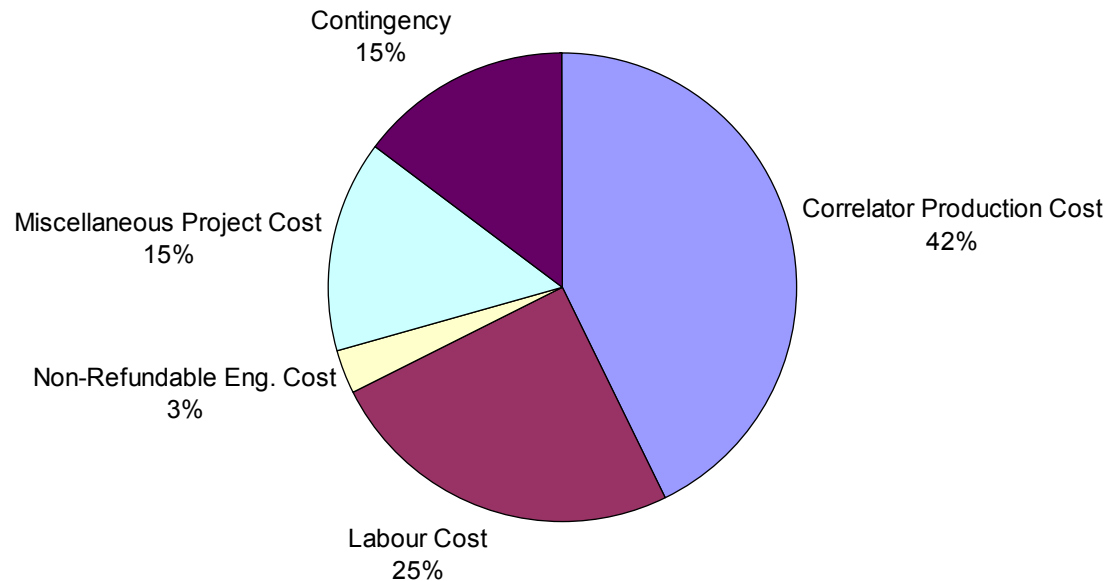
- All FPGA pinouts/designs for the baseline board must be complete (at least pinout definitions)

Staff Resource Identification	Estimate to Complete (in Hours)		
	Best Case	Worst Case	Most Likely
Brent Carlson	400	800	600
High Density Design (from contract estimate)	400	600	480

Sample Page from WBS “Dictionary”

Cost Breakdown

EVLA Correlator Total Cost Breakdown



“Risk-based” Contingency Allocations

Contingency Table	%
Correlator Production Cost	17
Labour Cost	20
Non-Refundable Engineering Cost	30
Miscellaneous Project Cost	10

Design Reviews - Milestones for Technical Progress

- Three Design Reviews planned:
 - Conceptual (CoDR - complete) - review architecture and overall design.
 - Preliminary (PDR) - review detailed designs before prototypes.
 - Critical (CDR) - review system before major production.

Correlator Schedule (unchanged)

<i>Date</i>	<i>Milestone</i>
Nov. 2/2001	Conceptual Design Review (CoDR). Design frozen. (Now complete)
Q1, 2002	New personnel in place. Design tools in place. Training and design work begins.
Q1, 2004	Critical User Manuals in place. Device driver code can be written.
Q2, 2004	Preliminary Design Review (PDR). Designs ready for prototype fabrication.
Q1, 2005	Single baseline prototype test at the VLA starts.
Q2, 2005	Single baseline prototype test at the VLA complete.
Q3, 2005	Critical design review (CDR). Prototype testing complete. Ready for procurement of production components and full production.
Q2, 2006	Production model test and burn-in, system integration and test in Penticton, and rack and cable installation begins at the VLA.
Q4, 2006	Begin full installation at the VLA. Earliest possible start of installed correlator testing.
Q2, 2007	Earliest possible “beta” science data. (Middle of full installation schedule.)
Q1, 2008	Correlator commissioning. Correlator fully on-line for observing. Continuing debug support available.
Q1, 2009	End of project. End of NRC debug support. Full handover to NRAO complete.

Non-Technical Program Risks

- Risks in order of seriousness (impact x probability):
 - CFI funding does not materialize.
 - Remedy - Look to NRC to provide leadership and resources by going to Industry Canada directly (or other such measures). If not possible, quit the project.
 - Inadequate CFI funding.
 - Remedy - Must find another payer. Candidates are NRC, NRAO. We must identify the funding up front.

Non-Technical Program Risks

- Schedule slippage due to a slow start (already happening).
 - Remedy - If the slippage is small, catch up by spending more money on staff.
 - Modern tools and methodology may help make up time.
- Continuing slide in the C\$ and not being recognized in funding profile.
 - Remedy - Either obtain more funding or obtain \$US up front.

\$C currently rising wrt \$US.

Non-Technical Program Risks

- Inadequate contingency.
 - Remedy - The contingency ratios are smaller than most projects, thus the risk is high.
- Inflation not being recognized in funding profile.
 - Remedy - Most likely if project is delayed. Another budgetary issue.
- *As of Sept/03, these issues are still potentially troublesome, but we are not far enough along yet to know.*

Descoping

- Have not reconsidered descoping options since the last Advisory Board meeting.
- As design matures, real costs will become evident.
- We are finding a rough balance between cost savings and cost increases at the moment.
- More complete project management system needed to obtain sufficient detail for more accurate predictions.

Project Summary

- Are we meeting the required schedule?
 - We are somewhat behind in software because of hiring delays. We are possibly catching up in hardware design. Re-evaluation of detailed schedule to 2005 is needed.
 - Are we over budget at this stage?
 - Budget is slimly allocated, but we are not over budget.
 - Are we planning to deliver on what we said we would do?
 - Yes, with minor improvements.
 - What are the major risks at this stage?
 - Major near-term risks have been mitigated.
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