The WIDAR Correlator

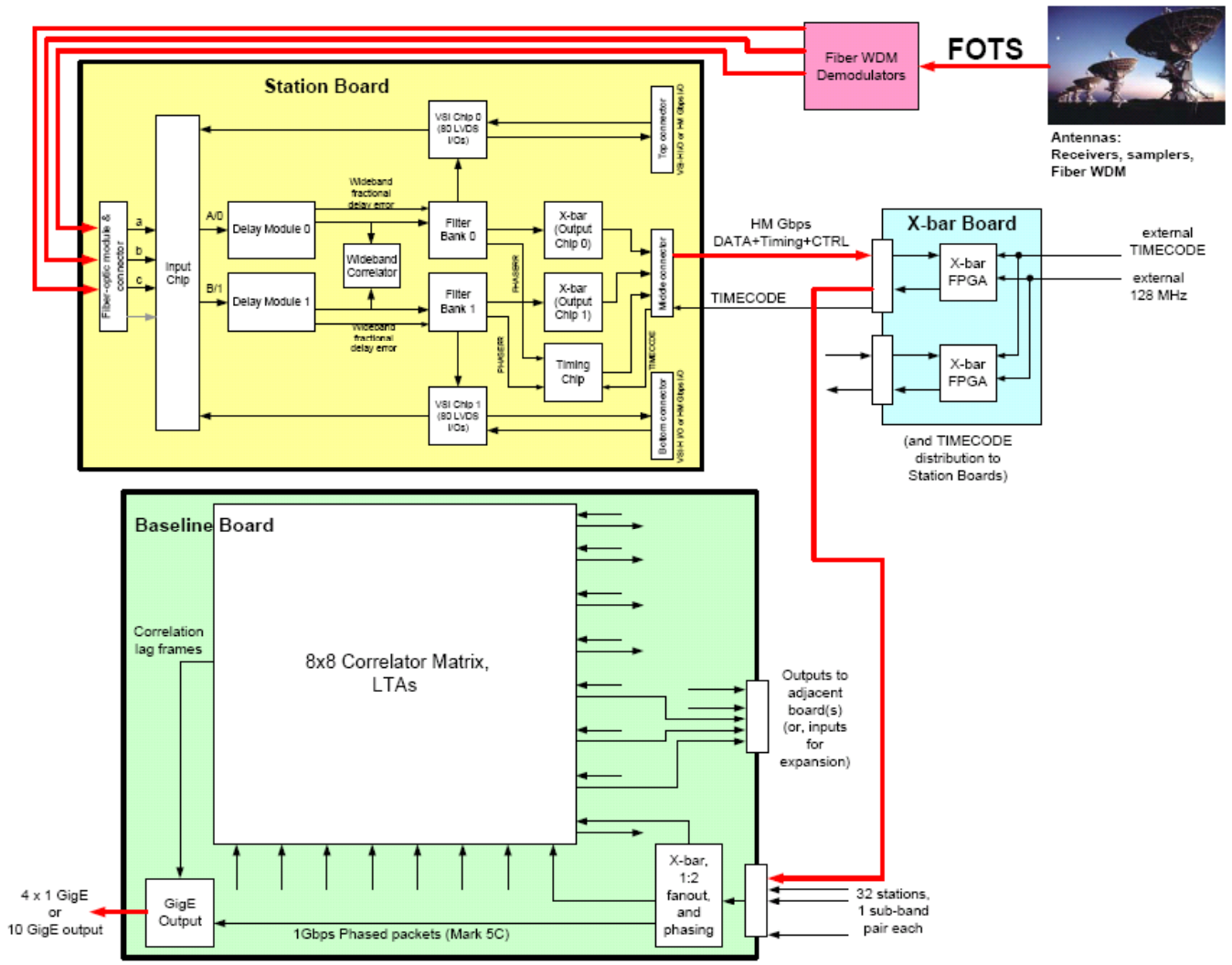
Sean M. Dougherty

Dominion Radio Astrophysical Observatory
Herzberg Institute of Astrophysics
National Research Council Canada

Objectives

- Highlights
- Critical Design Review
- Hardware status
- Software status
- Schedule
  - Project
  - Production
  - Software
- Budget
- Risks

WIDAR System Overview



Staged Hardware Prototyping

- Stage 1 - 1st prototypes
  - Station and Baseline boards tested in 2007
  - X-bar board tested Jan/Feb 2009.
- Stage 2 - 2nd prototypes
  - Two of each board (Station and Baseline) built and tested.
  - Used in PTC on-the-sky testing
- Stage 3 - 3rd prototypes
  - 14 Station boards assembled
  - 14 Baseline boards (6 tested + 8 revised – being assembled)
- Stage 4
  - Full production and production testing of boards.

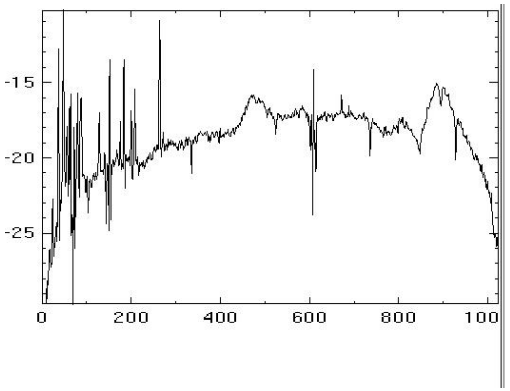
Highlights

- ASIC Correlator chip delivery (12,000) – April 2008
- Installation of the Proto-type correlator (PTC) – July 2008
  - up to 4 station boards and 1 baseline board
- ASIC reliability testing completed – Aug, 2008
- First Fringes – Aug 7th, 2008
- Installation of WIDAR Racks @ VLA site – Aug 2008
- Successful Critical Design Review – Dec 2-3, 2008
- Release of Station Board for full production – Jan 23, 2009

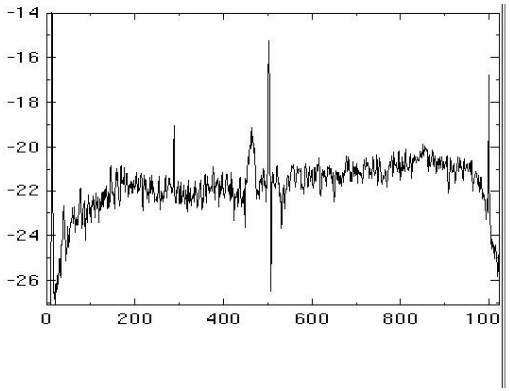
- Management review – Feb 2008
- SMD replaced PED as Project Lead – Mar 2008

First Fringes – Aug 7th, 2008

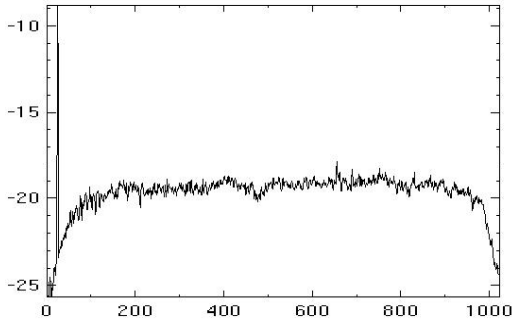
- WIDAR PTC produces first phase and delay-tracked fringes
- Eight sub-bands, 128 MHz each, 1024 channels each



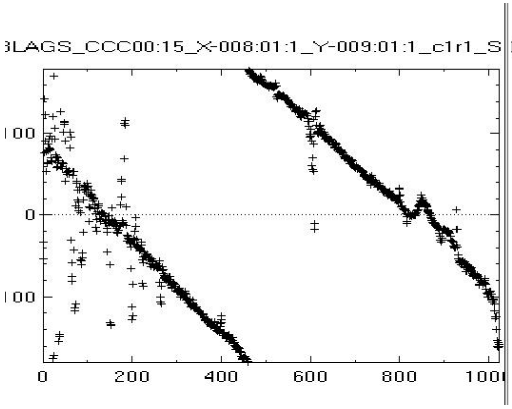
1116 – 1244 MHz

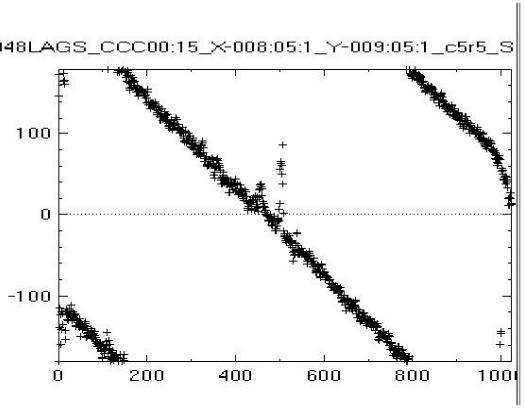


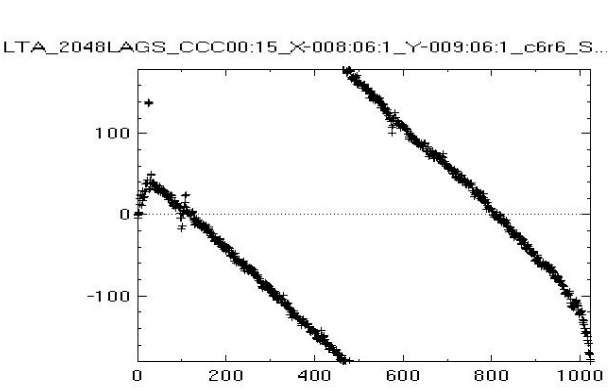
1628 -- 1726 MHz



1726 -- 1884 MHz







Correlator Rack Installation, Aug 2008

Correlator Room Infrastructure

Hardware CDR Dec 2-3, 2008

- Purpose:
  - Examination of complex hardware design and testing prior to committing to production.

- Roger Cappallo (MIT, chair)
- Dave Hawkins (Caltech)
- Barry Clark & Mike Revnell (NRAO)
- Provided two reports:
  - Formal summary of the review
  - Detailed in-formal supplementary comments

"…impressed by the design, the magnitude of the engineering effort encompassing that design, and the high level of technical competence shown by the design team. Also significant was the thought given to issues of manufacturability, reliability, and long-term maintainability."

CDR Charge

1. Does the correlator implementation meet the requirements (as defined in EVLA project book)?
2. Have sufficient tests of the Stage-3 prototypes been performed, to a high certainty, that full production units can be successfully manufactured?
3. Does the design and implementation of the correlator meet acceptable reliability, redundancy, and maintenance requirements?
4. Are production plans, testing plans, personnel and infrastructure at DRAO adequate to handle full production, and deliver high-quality, reliable units on the current schedule?
5. Is NRAO infrastructure sufficient to properly handle (i.e. receive, install, test, maintain, re-work, operate) boards of this size, complexity and quantity?
6. Have reasonable estimates of risk been established?

CDR Outcomes (I)

- Baseline Board
  - Only managed tests on 1 Stage-3 board prior to CDR.
  - *"…prudent to delay production until testing can be performed on a larger suite of prototype boards, and we recommend this be done."*
  - 6 Stage-3 boards now fabricated.
    - Identified preliminary production risk issues and reliability issues addressed via functionality testing and burn-in tests
    - Identified issues best addressed with new PCB layout
    - Initiated manufacture of 8 Stage-3.2 boards for testing prior to release for full production (late April)

CDR Outcomes (II)

- Station Board
  - Testing proceeded on 2 Stage-3 boards.
  - Power supply failure issue identified two days prior to CDR
  - *"…full production of boards commence only after power supply module failures and power-related FPGA deconfiguration are completely understood."*
  - Power supply failures due to faulty manufacturing batch
    - Replacement parts being delivered
  - Thorough examination of power-supply performance
    - Now soldering previously press-fit sockets
    - Double gauge copper now used on all power planes
  - FPGAs now powered up/down sequentially – firmware fix

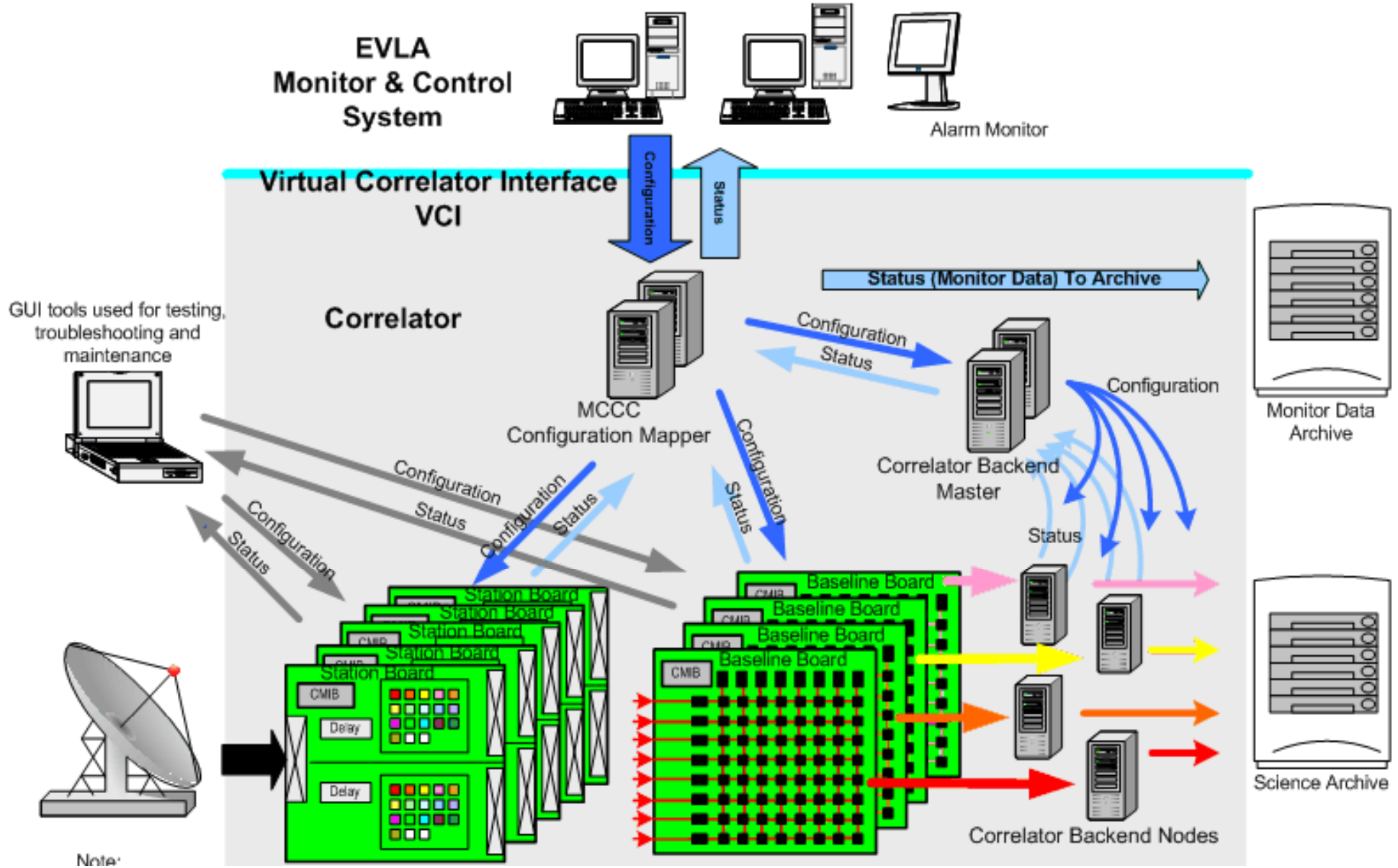
Hardware Progress Summary

- Reliable PCB manufacturer identified – mid-2008
- Station board
  - 14 Stage-3 boards completed
  - Production issues identified and resolved e.g. Delay Module connector
  - No manufacturing defects
  - Component problems identified e.g. power supplies
  - Full production commenced Jan 23, 2009
  - 9 Stage 3 + 1 Stage-2 boards available
    - for 10-station subset of production correlator (WIDAR-0)

- Baseline Board
  - 6 Stage 3 boards completed
  - No manufacturing defects
  - Component yield issues noted
    - E.g. regulator chip (3 of 384 failed) - new revision to be used in next iteration.
  - Some board performance issues identified e.g. Clock jitter
  - Resolved via lab fixes e.g. 60 additional capacitors added.
  - Re-spin to resolve identified problems in production boards.
    - 8 Stage 3.2 boards for final testing
  - Targeting release of full production manufacture ~ late Apr, 2009.
  - 2 Stage-boards available for WIDAR-0

- X-bar boards
  - X-bar board prototype built and tested successfully within 3 months.
  - 3 boards in Socorro for WIDAR-0

Software system



Correlator Software Team

- Sonja Vrcic
  - Software Coordinator (liaison w/ Bryan Butler)
  - overall design and specification.
  - Virtual Correlator Interface (VCI) definition
  - Configuration Mapper
  - Master Correlator Control Computer (MCCC)
- Dave Del Rizzo
  - X-bar board GUI + manager
- David Sharpe
  - GUI upgrades & maintenance

DRAO

- Bruce Rowen & Hichem Ben Frej
  - Correlator hardware control (CMIB).
- Kevin Ryan
  - GUI development
  - Correlator Power Control Computer (CPCC).
  - Test Executor
- Martin Pokorny
  - Correlator Backend (CBE)

NRAO

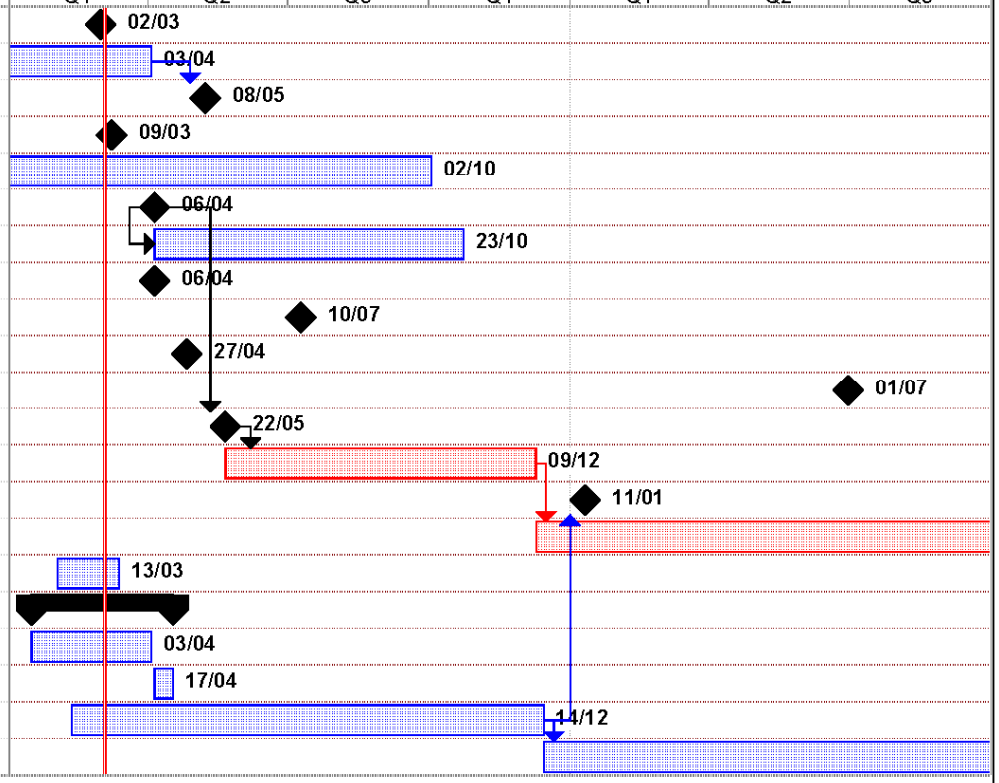
Software Status

- CMIB (Correlator Monitor Interface Board)
  - Handles delay models, generates controls for BB, coordinates FPGAs, monitors board status
  - Continuous development to provide more functionality
  - Current version WIDAR-0 capable.
- GUI's and test tools
  - GUI's provide "experts view" of correlator system.
  - GUI's control of SB and BB configuration, rack monitoring (power, temp etc).
  - X-bar GUI under development
    - Monitor/control of SB to BB connections.
    - Permanent maintenance tool
  - Real-Time Data Display for SB output developed
- CPCC (Correlator Power Control Computer)
  - Basic version implemented for Prototype correlator
  - WIDAR-0 version being tested.
- CBE (Correlator Back-End Software)
  - Generated date files for post-procesing.
  - Current version meets requirements for WIDAR-0.
- VCI (Virtual Correlator Interface)
  - Protocol defined, reviewed and accepted.
  - Configuration mapper to convert VCI parameters into SB and BB configuration info is under development
    - Parsing of common VCI parameters is complete – used in Prototype Correlator
    - X-bar switch capability under development for WIDAR-0
    - Delay model handling from Executor (part of M&C) – implemented.
    - Focus of current development is WIDAR-0 and OSRO support.

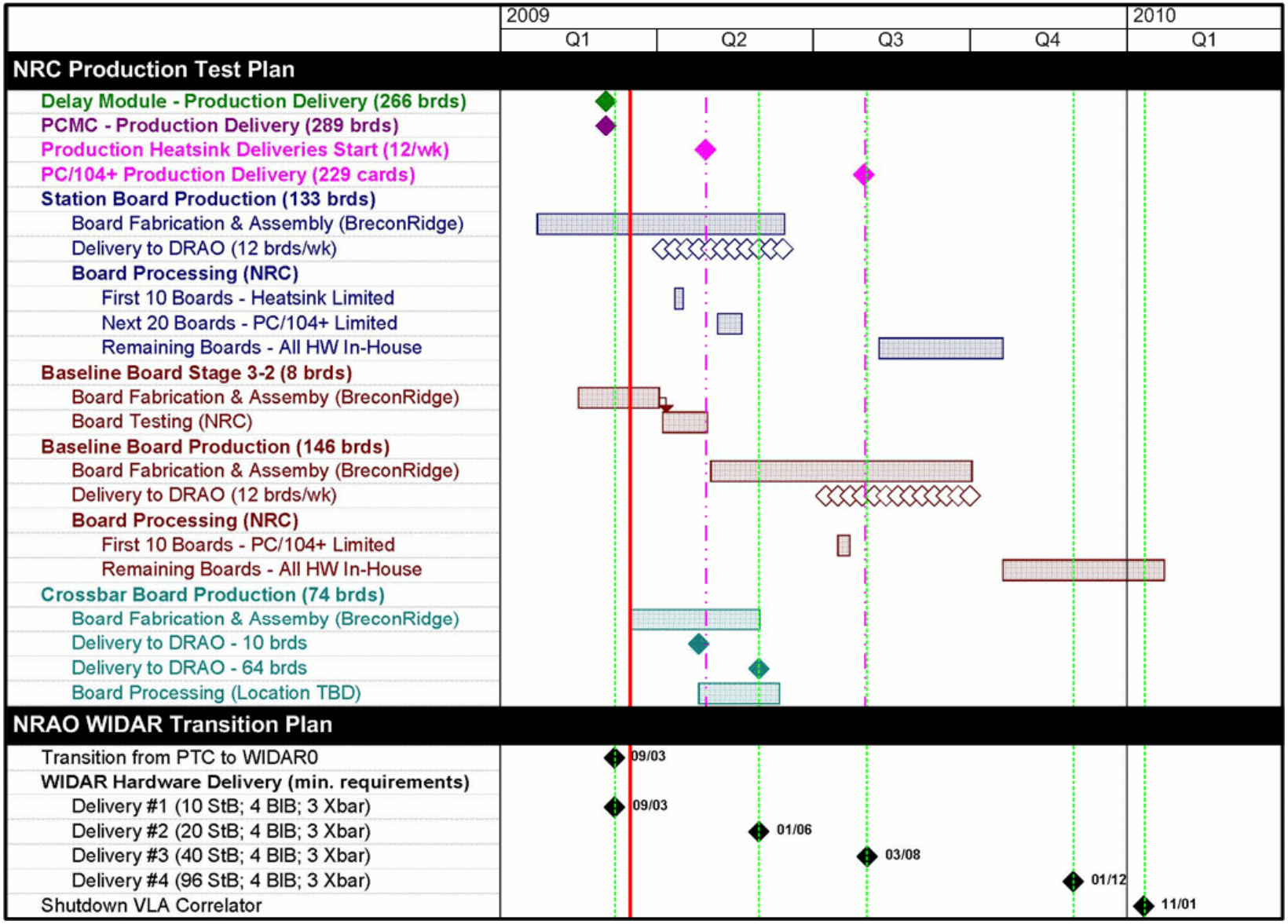
WIDAR schedule

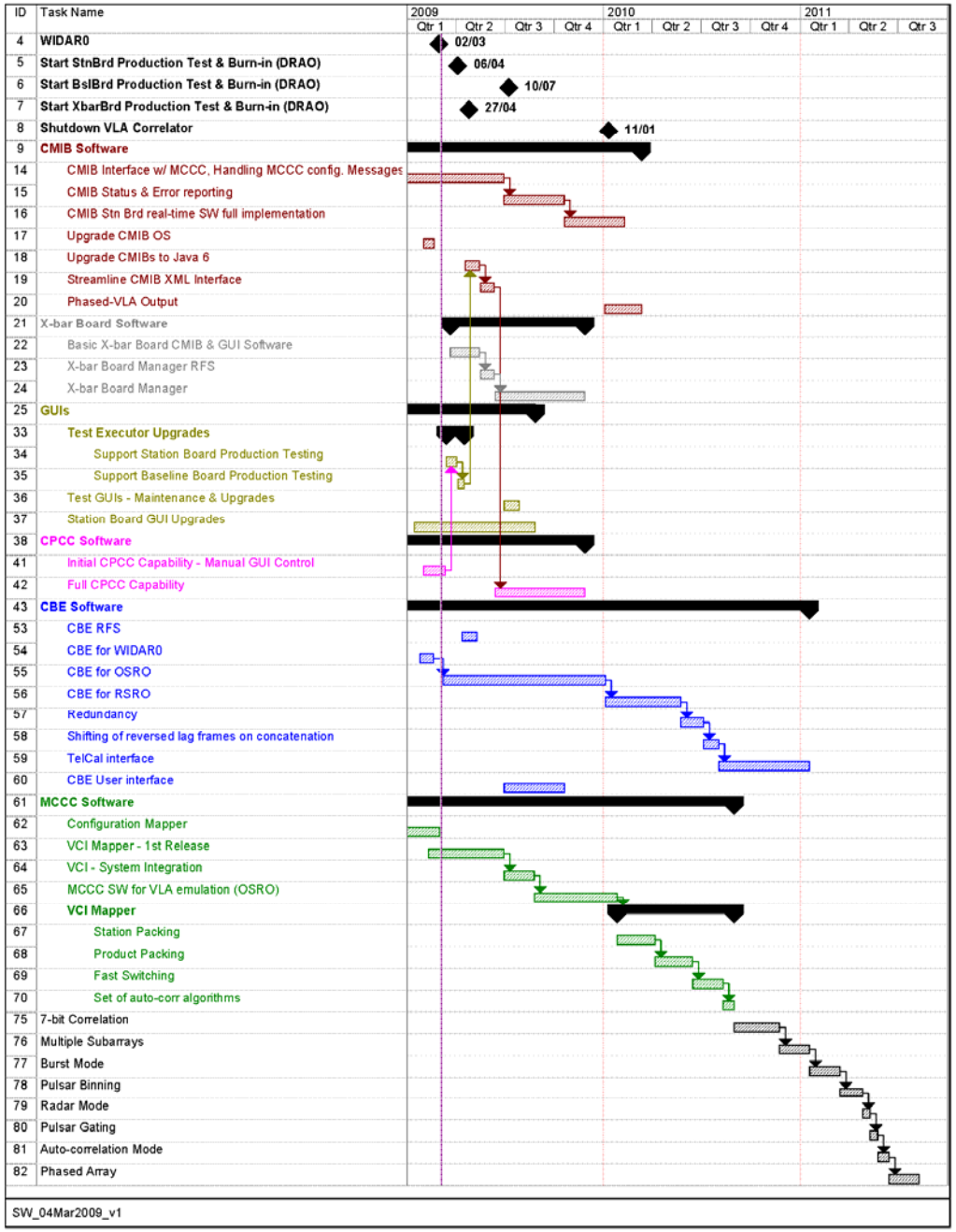
WIDAR Correlator Schedule

ID	Task Name	Start
14	*Crossbar Boards for 10-Station Correlator Arrive at VLA*	02/03/2009
15	Stage 3 Baseline Board PCB Fabrication & Assembly	26/08/2008
17	*Remaining 6 Stage 3 Baseline Boards Arrive at VLA*	08/05/2009
21	***WIDAR 0 Observing Begins***	09/03/2009
24	Full Production (Stage 4) PCB Fabrication & Assembly	09/12/2008
25	***First Production Board Delivery to Penticton***	06/04/2009
26	Full Production Test & Burn-in in Penticton	06/04/2009
27	*Start StnBrd Production Test & Burn-in*	06/04/2009
28	*Start BslBrd Production Test & Burn-in*	10/07/2009
29	*Start XbarBrd Production Test & Burn-in*	27/04/2009
31	*Full Up CBE HW Delivered to VLA Site*	01/07/2010
32	***First Production Board Arrive @ VLA***	22/05/2009
33	Production Board Installation & Testing @ VLA	22/05/2009
34	**Turn Off Old Correlator**	11/01/2010
35	Commissioning/Operational Support	10/12/2009
39	Software for WIDAR 0	02/02/2009
40	**Software for Production Board Testing**	**16/01/2009**
41	Station Board Production Test Software	16/01/2009
42	Baseline Board Production Test Software	06/04/2009
43	OSRO Software	11/02/2009
44	Full System Software	15/12/2009



Board Production Schedule





WIDAR Software Schedule

- Software is in place for WIDAR-0
- Near-term goal: software for OSRO
- Longer term: schedule driven by RSRO demands

WIDAR Budget

- Aug 2003 – Canadian Treasury Board approval of submitted budget ($C 20M over 5 years).
  - Five-year period close - Mar 31, 2008.
  - Budget reprofiling established to Mar 31, 2011
- Additional monies from:
  - eMERLIN - $C 1.4M
  - NRC - $C 0.6M
- Budget outlook
  - Technical risks are diminishing
  - Production delay into FY09/10
    - exposed to currency fluctuation
      - e.g. August 2008 – 0.96c/$ vs March 2009 – 0.77c/$
    - NRC assumes that risk

Program Risks

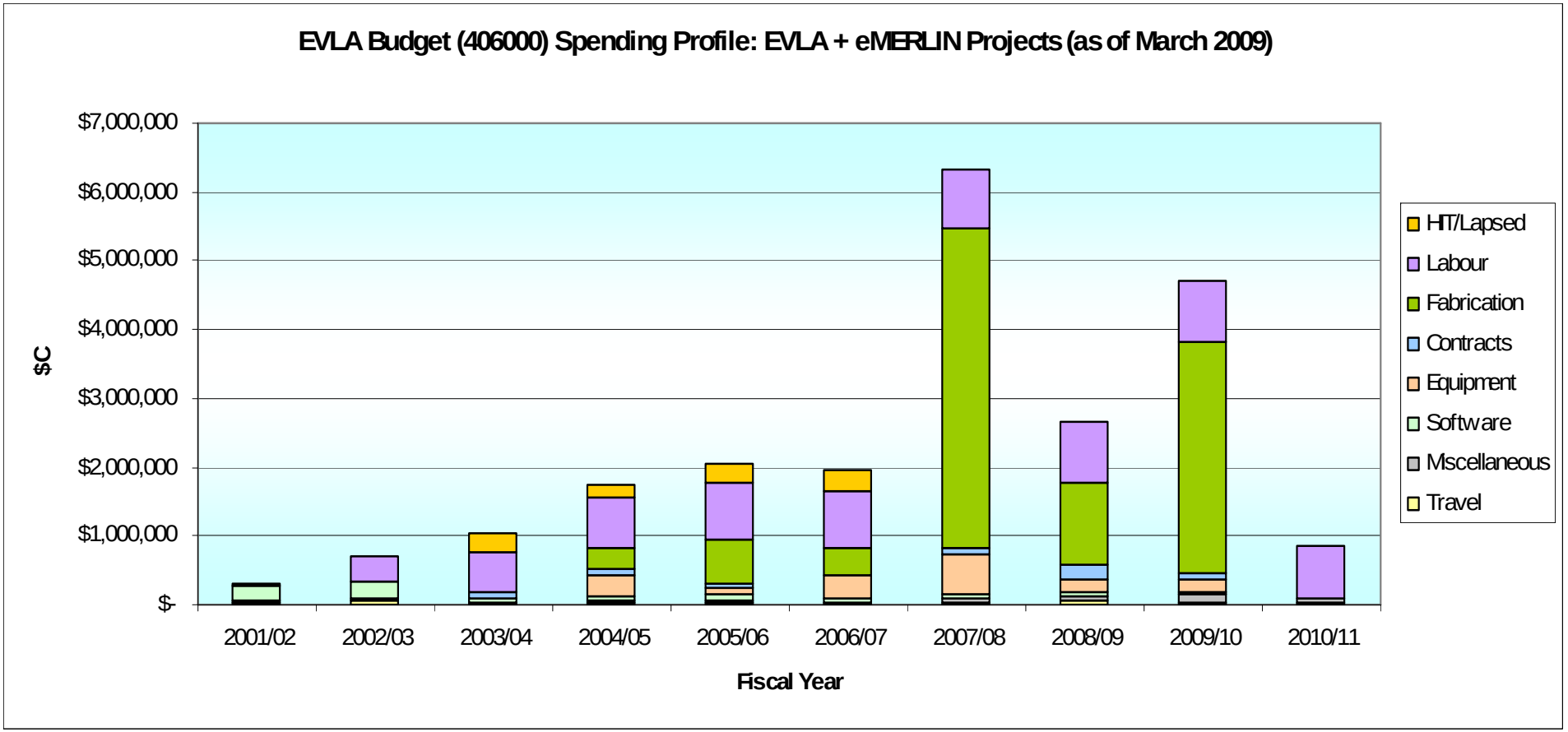
- Technical risk
  - VASTLY reduced with successful, thorough hardware tests
  - Unidentified yield issues e.g. regulator chip
  - Assembly into a final system
- Manufacturing risk -> schedule risk
  - Reliant on a sole board manufacturer
  - Board processing at DRAO
    - Plan in place
    - Minimum rate required to meet Transition milestones 2 boards / 3 days
  - Delivery of assembly hardware
    - PWGSC (Government) contracting procedures
    - Some long lead times pushed out parts delivery e.g. PC104, heatsinks
- Software completion slip -> schedule risk.
  - Software will become critical path in near future
  - Near-term focus on software for Open Shared Risk Observing and Early EVLA Science
- Budget risks
  - Cost risk reduced with completed prototype/pre-production stage
  - Exchange-rate exposure – NRC has assumed that risk.

Summary

- Major progress made in past year => technical risk diminishing rapidly
  - Prototype correlator
  - First Fringes
  - Rack and correlator room infrastructure installation
  - Critical Design Review
  - Release of Station board for production
  - Installation and successful testing of production hardware in racks => WIDAR-0
- Are we meeting the current transition schedule?
  - Yes, though Stage-3 baseline board prototyping is not yet complete
- Are we over budget at this stage?
  - Exposed to currency rate fluctuation – NRC will cash manage.
- Are we planning to deliver on what we said we would do?
  - Yes (with improvements!)
- What are the major remaining risks?
  - Production capability
  - Software capability

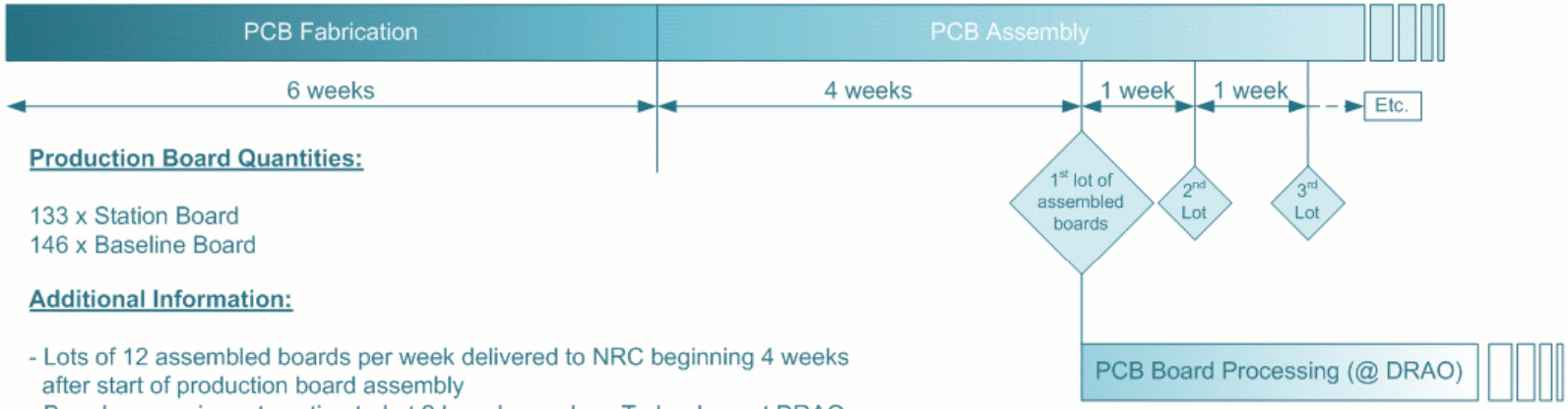
Supplemental Slides

Spend profile (I)



PCB Production timescales

Station Board/Baseline Board Production Timeline



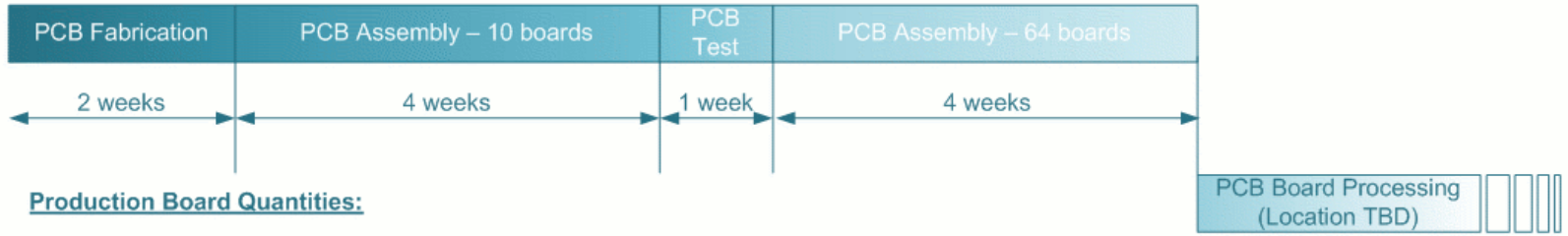
Production Board Quantities:

133 x Station Board
146 x Baseline Board

Additional Information:

- Lots of 12 assembled boards per week delivered to NRC beginning 4 weeks after start of production board assembly
- Board processing rate estimated at 2 boards per day. To be done at DRAO.

Crossbar Board Production Timeline



Production Board Quantities:

74 x Crossbar Board

Additional Information:

- Two assembly stages: 10 boards assembled; acceptance testing; remaining 64 boards assembled.
- Board processing rate currently not estimated. To be decided whether final assembly and functional testing will be done at BreconRidge or at DRAO.