High Speed Digitizers

EVLA Advisory Committee Meeting

March 19-20, 2009

Steven Durand & Mike Revnell

Atacama Large Millimeter/submillimeter Array
Expanded Very Large Array
Robert C. Byrd Green Bank Telescope
Very Long Baseline Array

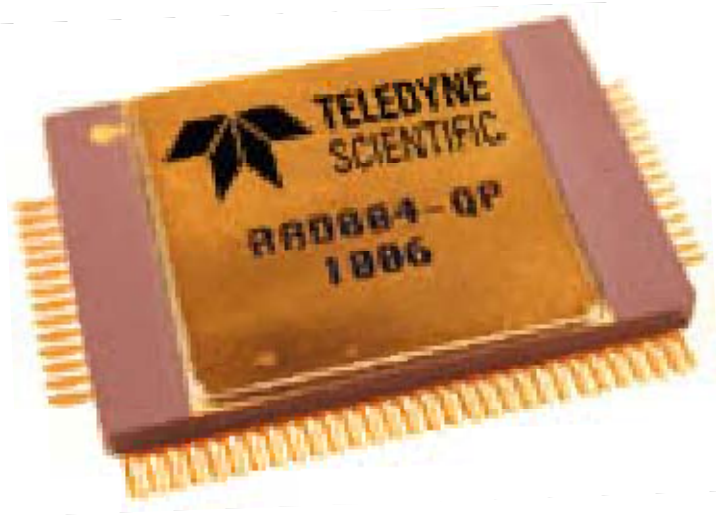
NRAO

High Speed Digitizer Description

- 8 GHz Bandwidth per polarization
  - Consists of eight digitizers, each with a bandwidth of 2 GHz
  - Operates in second Nyquist Zone (2-4 GHz)
  - Sample clock rate of 4,096 MHz
  - 3-bit output each
- 2 GHz Bandwidth per polarization
  - Consists of four digitizers each with a bandwidth of 1 GHz
  - Operates in second Nyquist zone (1-2 GHz)
  - Sample clock rate 2,048 MHz
  - 8-bit output each

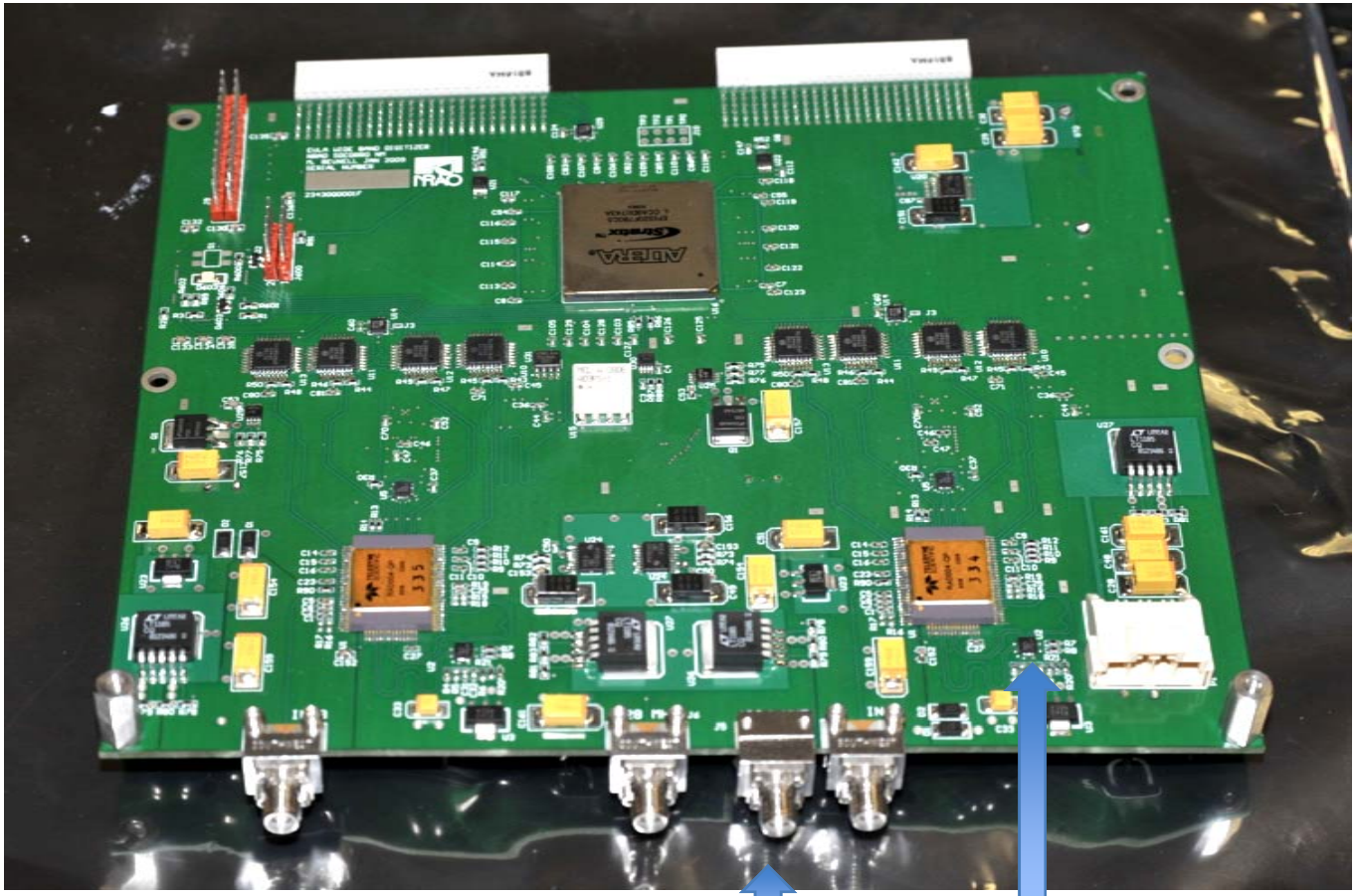
Teledyne RAD004

- Teledyne purchased Rockwell Scientific including digitizer division

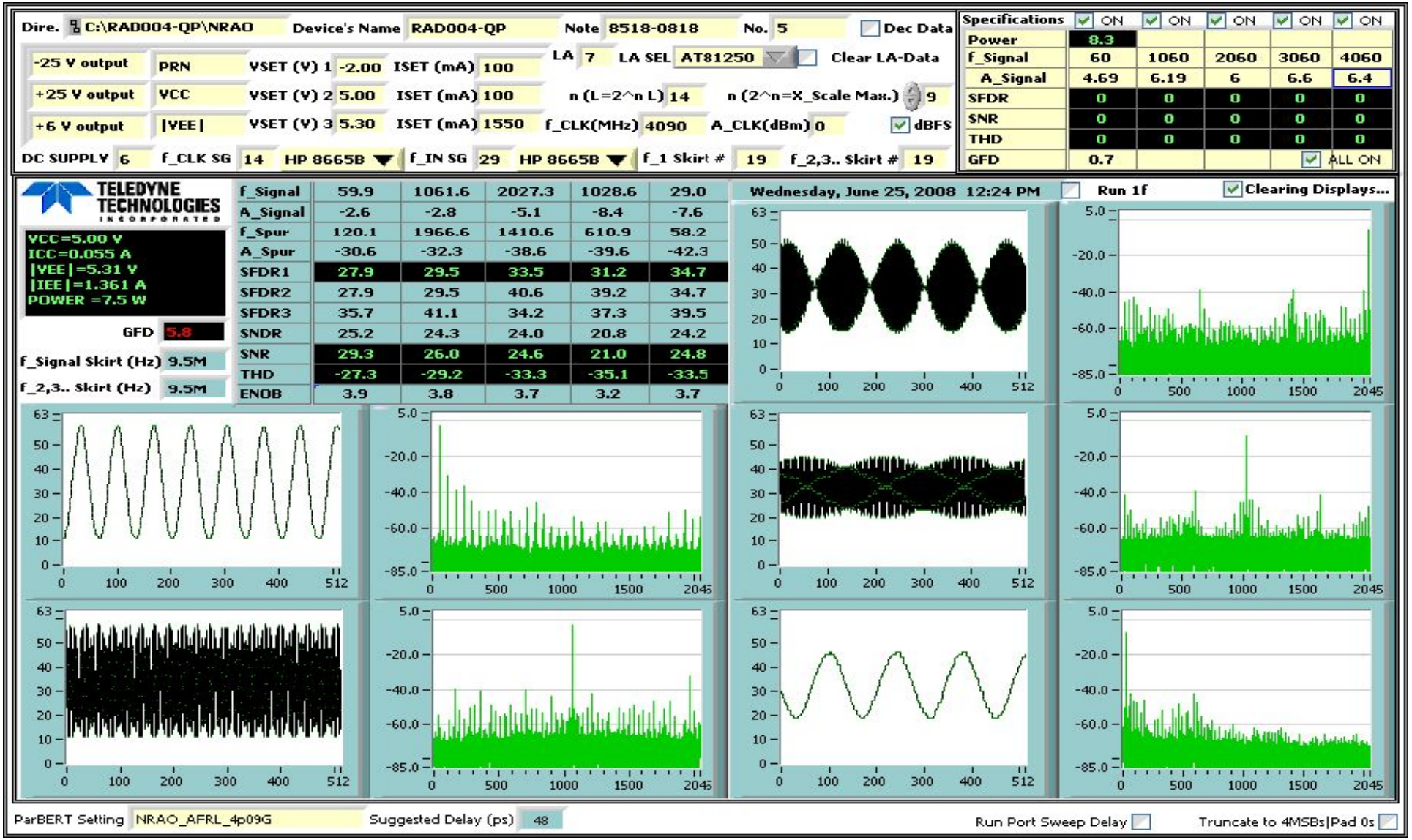


- Teledyne RAD004
  - 6-bit Digitizer
    - Bits 0 1 2 3 4 5
  - Analog input bandwidth 12 GHz
  - 0.5 Vpp full scale

3-Bit Digitizer Board

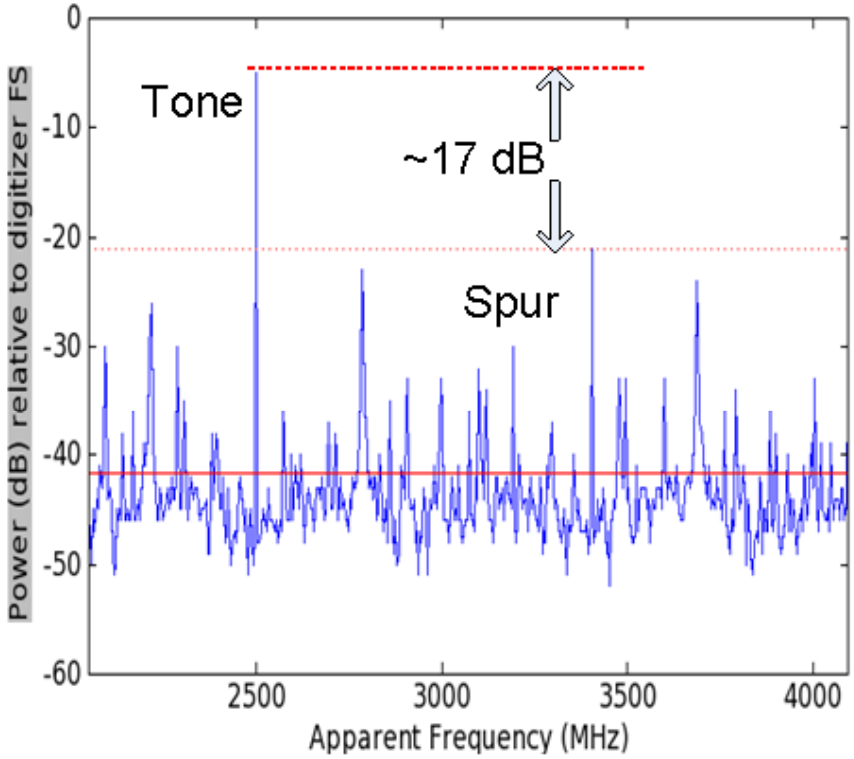


100% Performance testing by Teledyne at Wright Patterson Air Force Base



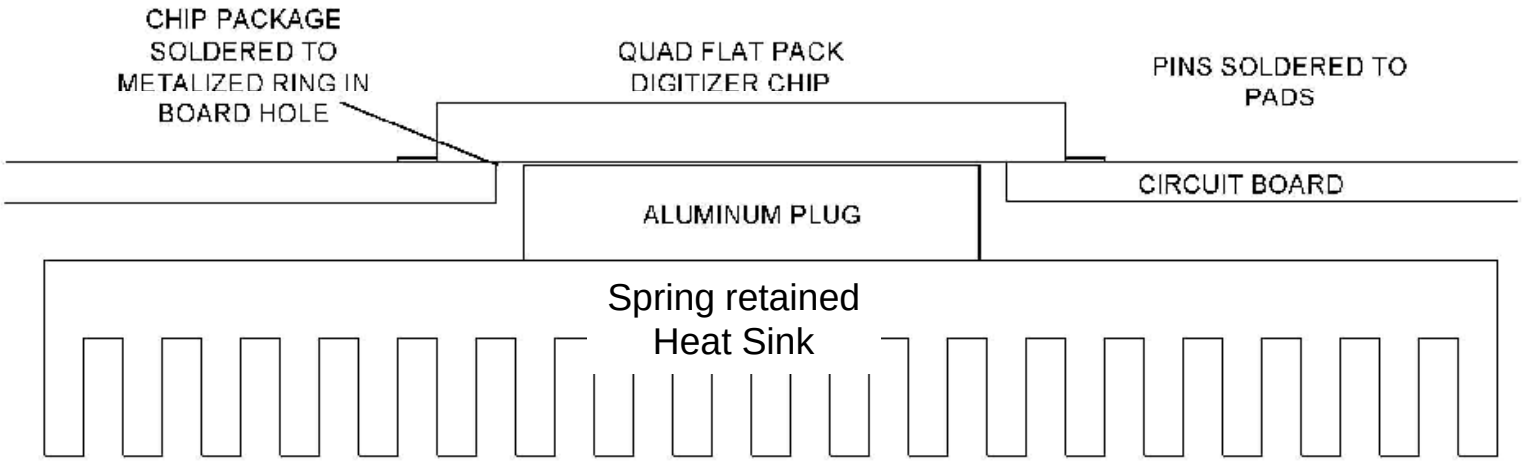
Preproduction Board Laboratory tests

- Spur Free Dynamic Range (SFDR) of ~18dB indicates a successful implementation
- 2048 point FFT
- Data collected in Deformatter board FPGA



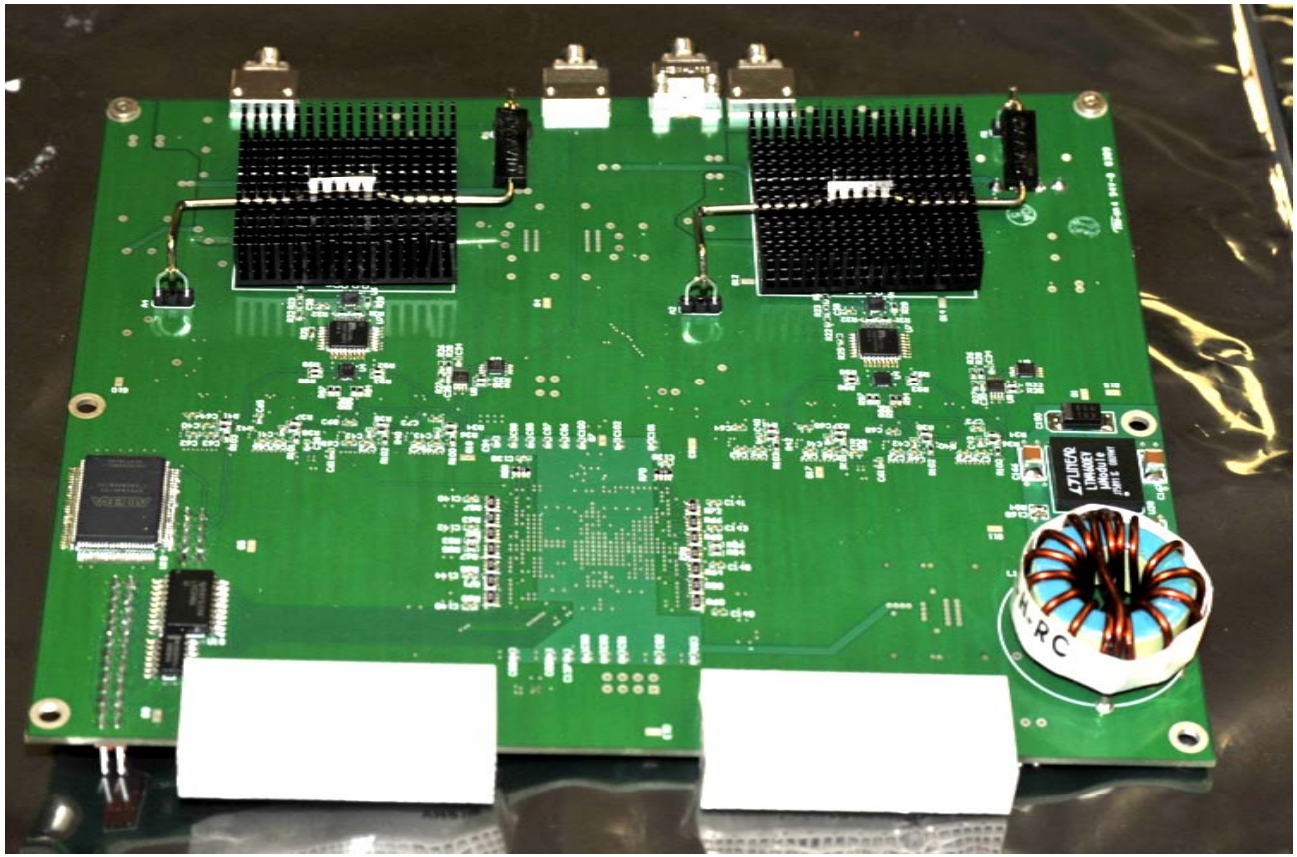
3-Bit Digitizer Heat Dissipation

- 4 GHz clock rate power dissipation ~7.5 W out the back
- Board layout optimized for high speed data performance
- Forced air ventilation and heat sinks provide the cooling
- Temperature sensors will be installed on each heat sink



Lab bench test indicate the heat sinks provide adequate cooling. Chip case temperature is under 40 C

Module is designed dissipate 200 W … present ~80 W



Development History

- Original design (2006) constructed with 2001 date code de-multiplexers
- Prototype passed engineering laboratory tests (2006)
- Decision to proceed with Teledyne based design November 2006
- Contract to purchase Teledyne digitizers awarded in September 2007
  - Delivery of digitizers began in September 2008
- Preproduction prototype constructed September 2008 with production parts failed lab tests because of clock rise time problems
  - Problem traced to de-multiplexer chips with date code 2006 and 2008
  - Modified the design and layout to slow rise times. (Version G)
- Version G is under test

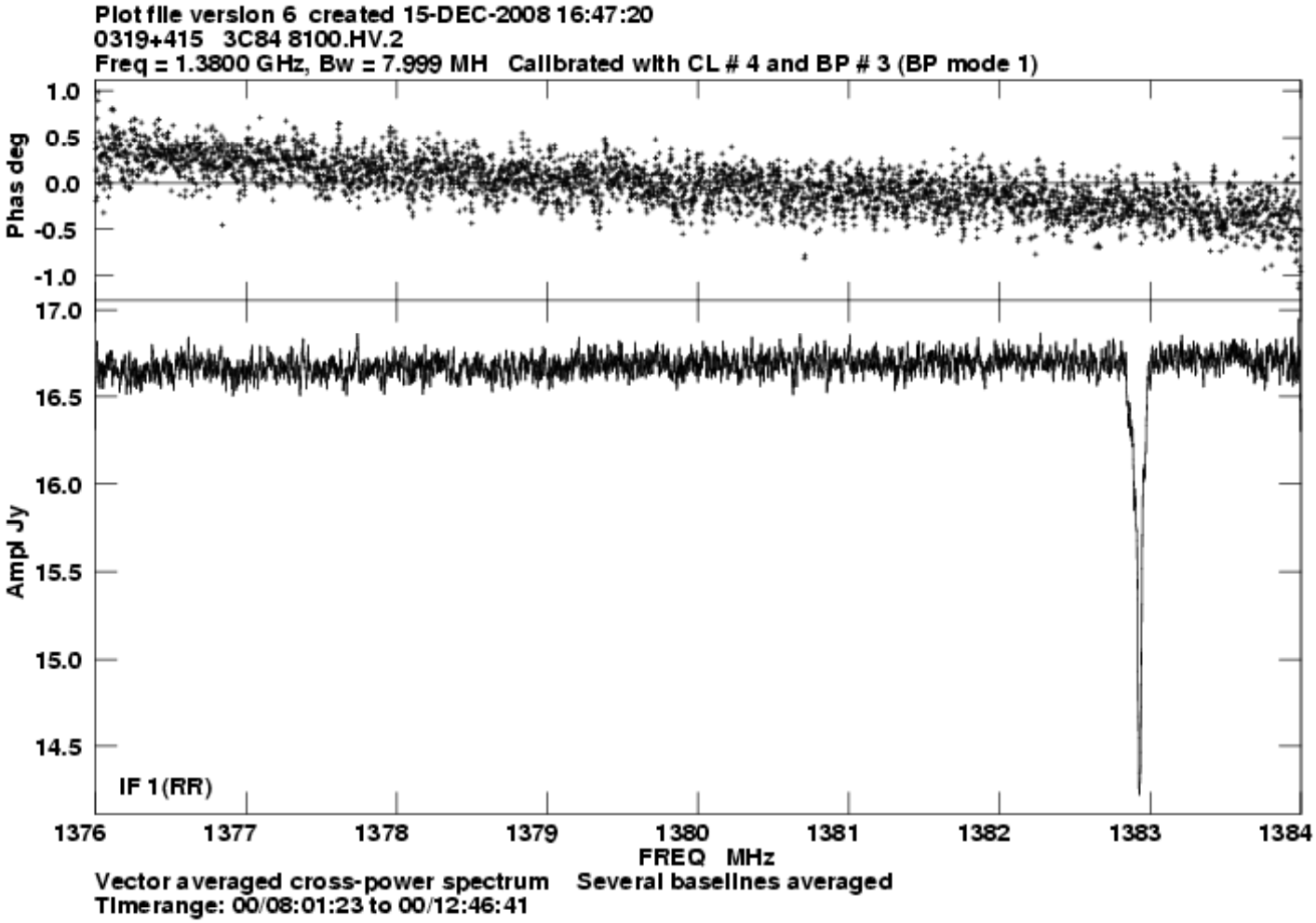
- Scheduled to start installation in the array June 2009
- Plan is to retrofit 18 antennas (8 digitizers each) by July 2010

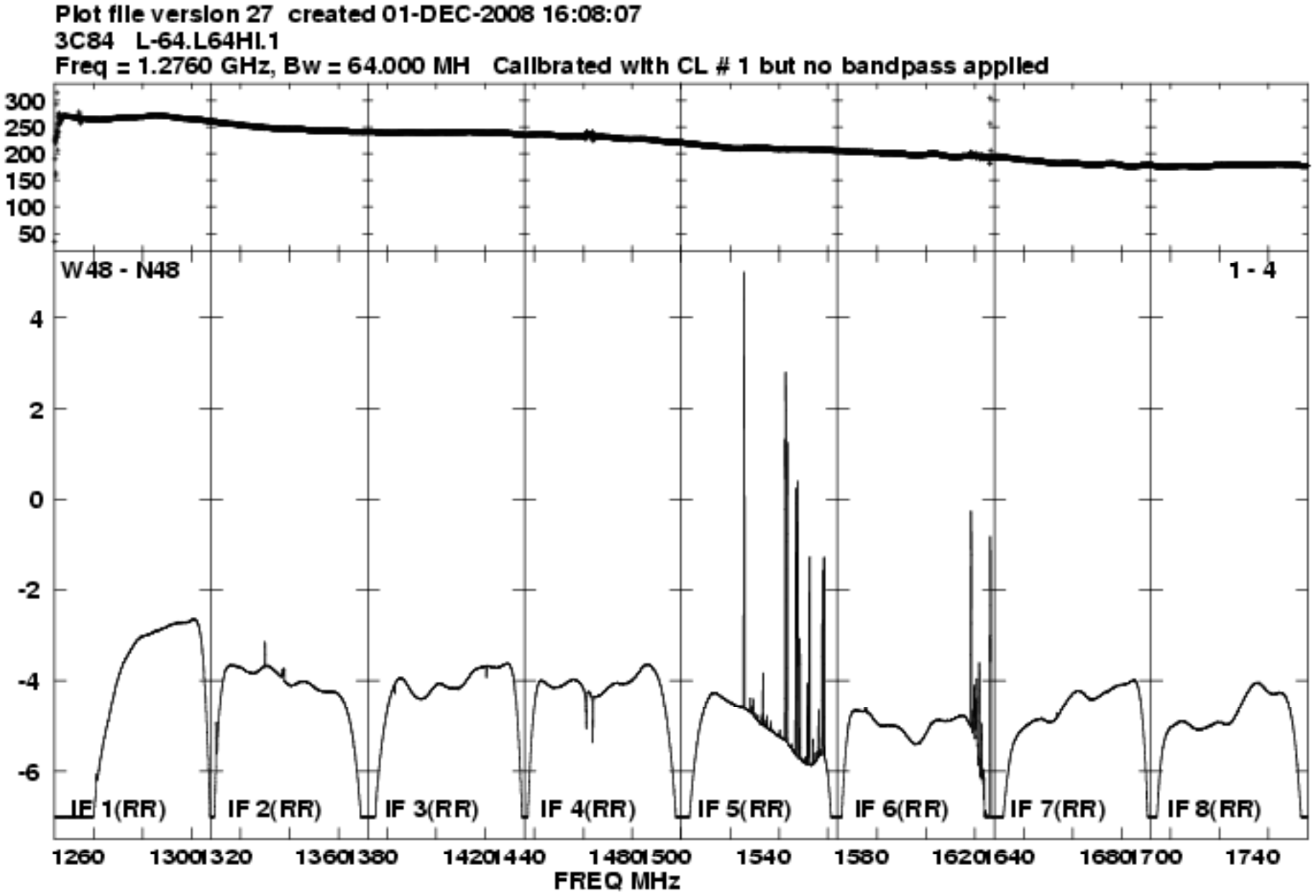
3-bit Digitizer Summary

- Version G under test
- Installation scheduled to start June 2009
- Farm-out board assembly – install in existing DTS modules
- 75% of Teledyne digitizers are in house, remainder by April 2009
- 100% of the digitizers chips tested by manufacturer

- WIDAR verification pending (end-to-end system test)

Questions


Plot file version 6 created 15-DEC-2008 16:47:20
0319+415 3C84 8100.HV.2
Freq = 1.3800 GHz, Bw = 7.999 MH Calibrated with CL # 4 and BP # 3 (BP mode 1)
Phas deg
1.0
0.5
0.0
-0.5
-1.0
17.0
16.5
16.0
15.5
15.0
14.5
Ampl Jy
IF 1(RR)
1376
1377
1378
1379
1380
1381
1382
1383
1384
FREQ MHz
Vector averaged cross-power spectrum Several baselines averaged
Timerange: 00/08:01:23 to 00/12:46:41


Plot file version 27 created 01-DEC-2008 16:08:07
3C84 L-64.L64HI.1
Freq = 1.2760 GHz, Bw = 64.000 MH Calibrated with CL # 1 but no bandpass applied
300
250
200
150
100
50
W48 - N48
1 - 4
4
2
0
-2
-4
-6
IF 1(RR)
IF 2(RR)
IF 3(RR)
IF 4(RR)
IF 5(RR)
IF 6(RR)
IF 7(RR)
IF 8(RR)
1260
1300
1320
1360
1380
1420
1440
1480
1500
1540
1580
1620
1640
1680
1700
1740
FREQ MHz
Lower frame: Log10(Amp) Jy Top frame: Phas deg
Scalar averaged cross-power spectrum Baseline: W48 (01) - N48 (04)
TImerange: 00/06:40:46 to 00/06:52:23

6 Bit 4 GS/s Analog to Digital Converter

Features

- 6-Bit Resolution
- Up to 4 GS/s Sampling Rate
- Integrated Dual Track and Hold
- 0.5 Vpp Differential Full Scale Range
- 6 GHz Full Power Bandwidth (min)
- DNL: 0.5 LSB
- INL: 1 LSB
- ENOB: 4.5 Typical (DC to 4 GHz)
- No Missing Codes
- LVDS Compatible, Adjustable CML Output
- Grey Code Output
- Over-Range Indicator Output
- Integrated Pseudo Random Pattern Generator
- 2 Clock Cycles Latency
- 88 Pin QFP Package
- 7.5 W Power Dissipation
- 1 to 4 Demultiplexed Binary Output when Coupled with RDX004M4
- ROHS Compliant

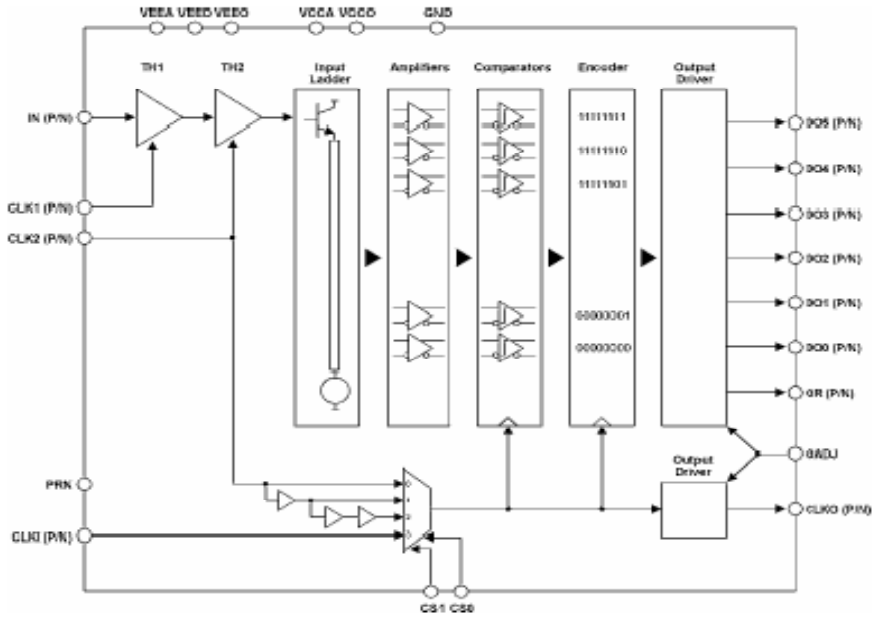


Figure 1 - Functional Block Diagram