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Expanded Very Large Array

The EVLA Correlator

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National Research Council Canada

Corrélateur WIDAR Correlator

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Outline

1. Correlator Performance Goals
2. Hardware Progress
3. Software Progress
4. System Progress
5. Prototype Testing
6. Funding, Budget & Schedule
7. Risk Issues

Key EVLA Processing Capabilities

Deep Imaging Polarization

- ✓ 8 GHz Bandwidth (dual polarization).
- ✓ Full polarization processing.
- ✓ Wide-field imaging.

Narrow spectral lines Wideband searches

- ✓ 16,000 channels at max. bandwidth (BW).
- ✓ $>10^6$ channels at narrow BWs.
- ✓ Spectral resolution to match any linewidth.
- ✓ Spectral polarization (Zeeman Splitting).

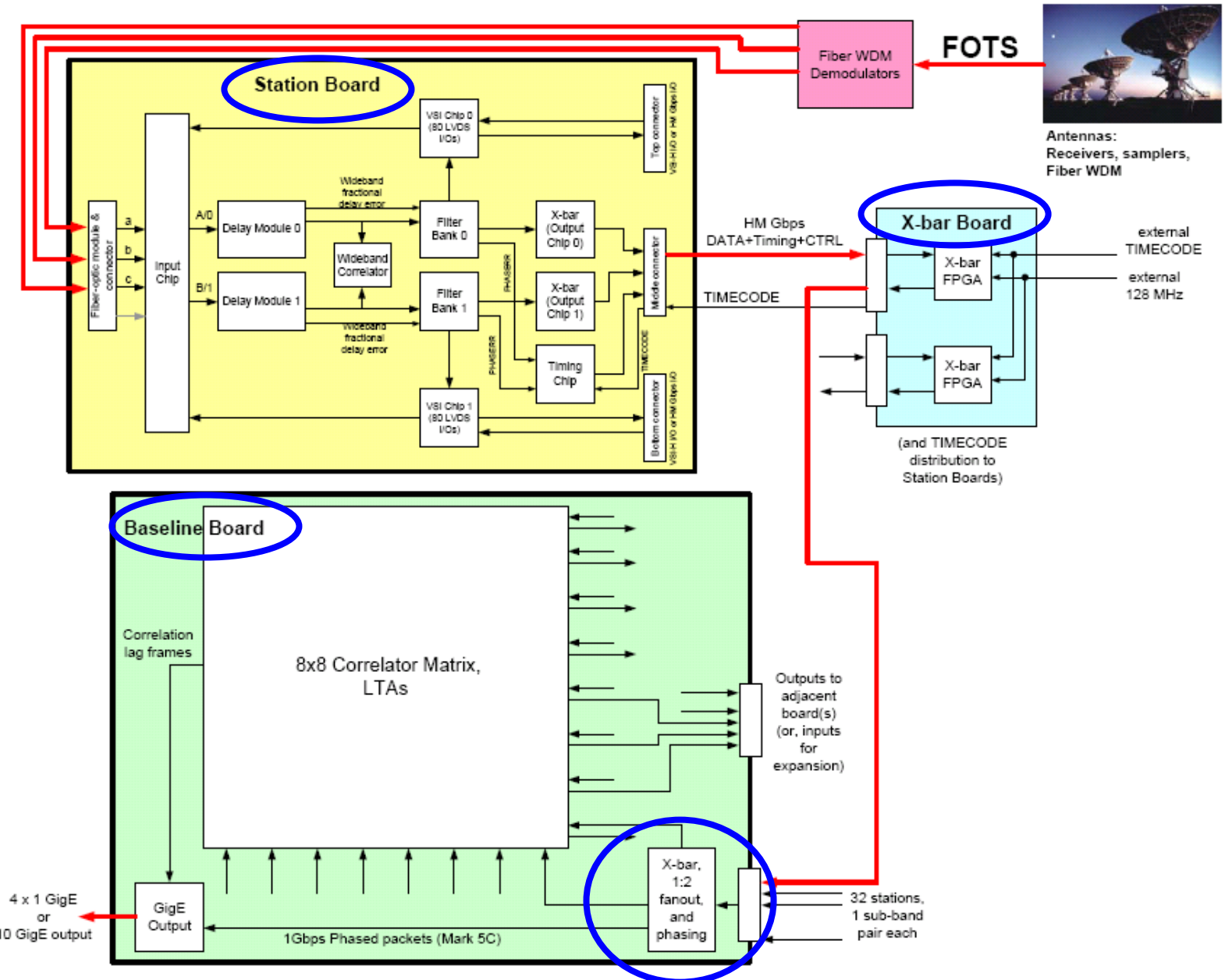
Flexibility Many resources

- ✓ 8 tunable 2 GHz wide bands.
- ✓ Each band - 16 tunable sub-bands.
- ✓ Sub-band – independent spectral resolution.
- ✓ Simultaneous line and continuum.

High time resolution

- ✓ 1000 pulsar “phase bins”.
- ✓ “Single-dish” data output to user instruments.
- ✓ Very fast time sampling (<20 μs).

EVLA Correlator System Diagram



Significant Events Since May, 2006

- All 1st prototype circuit boards have been extensively tested and small revisions implemented.
  - Second prototypes will be ordered mid-Sept.
- Correlator Chip Production CDR – May/07
  - Production quantity now on order ($US2.3M).
- Correlator power system is installed ($US270k).
- $2.8M worth of production parts on order.
  - FPGA's, COTS & other chips, cables, racks, subracks.
- Total production stage expenditures: $US7.2M
- Software development paralleling H/W.
  - Software already in use for H/W and will be used for OTS.
- Assembly of racks to begin in autumn.
- Connectivity Design Review – Jul/07.
  - Simplified architecture.

New Connectivity Scheme

- Efficient use of hardware, especially correlator boards.
- Simultaneous VLBI, New Mexico Array no longer needed.
- Improvements in numbers of channels, especially more flexible use of recirculation.
- Simplified structure – easier to allocate resources.
- Somewhat more reliable
  - Fewer connections.
- Small changes to baseline board needed, now done.
  - Xbar switch to provide flexibility of sub-array allocation.
  - Phased sum possible with full 8 GHz (2 pol) bandwidth.
- Somewhat less expensive system.
- Expansion remains possible, but more restrictive.
- Reversible if required, although parts count would increase.
- Recently reviewed.

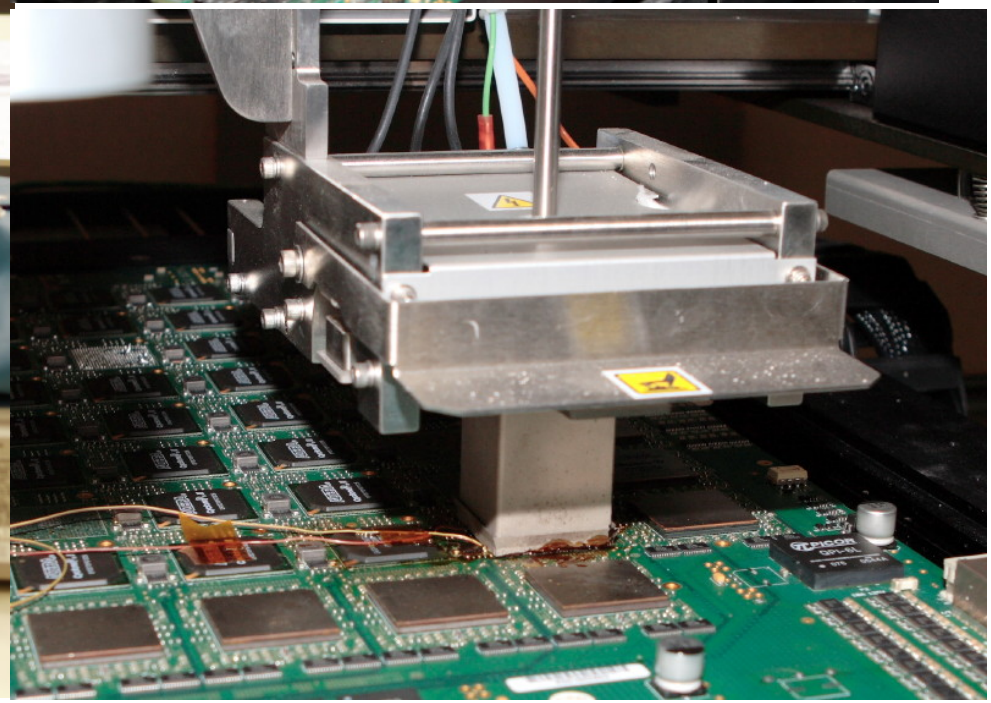
Hardware Progress Summary

- FPGA's
  - Almost all FPGA's are designed and tested thoroughly, including the Filter Chip.
  - Remaining FPGA's are RXP (retiming & phasing) and the X-bar.
  - Any remaining bugs in FPGA's can be fixed in-system.
- Station board
  - Data paths have been validated.
  - Requires some "bug fixes" and a re-spin.
  - Functional testing, including integration with Baseline Board is almost complete.
  - Second prototype to be sent for manufacture mid-Oct.
- Baseline Board
  - Baseline Board requires a revisions to accommodate a cross-bar switch.
  - Functional testing with a sub-set of correlator chips is complete.
  - Phasing board no longer needed – phased array now incorporated into Baseline Board.
  - Second prototype to be sent for manufacture end of Sept.
- Other boards
  - Fan-out board replaced by X-bar board in Station subsystem.
  - Daughter boards exist and have been tested.
  - A few simple boards remain to be done.
- System (see subsequent slide)

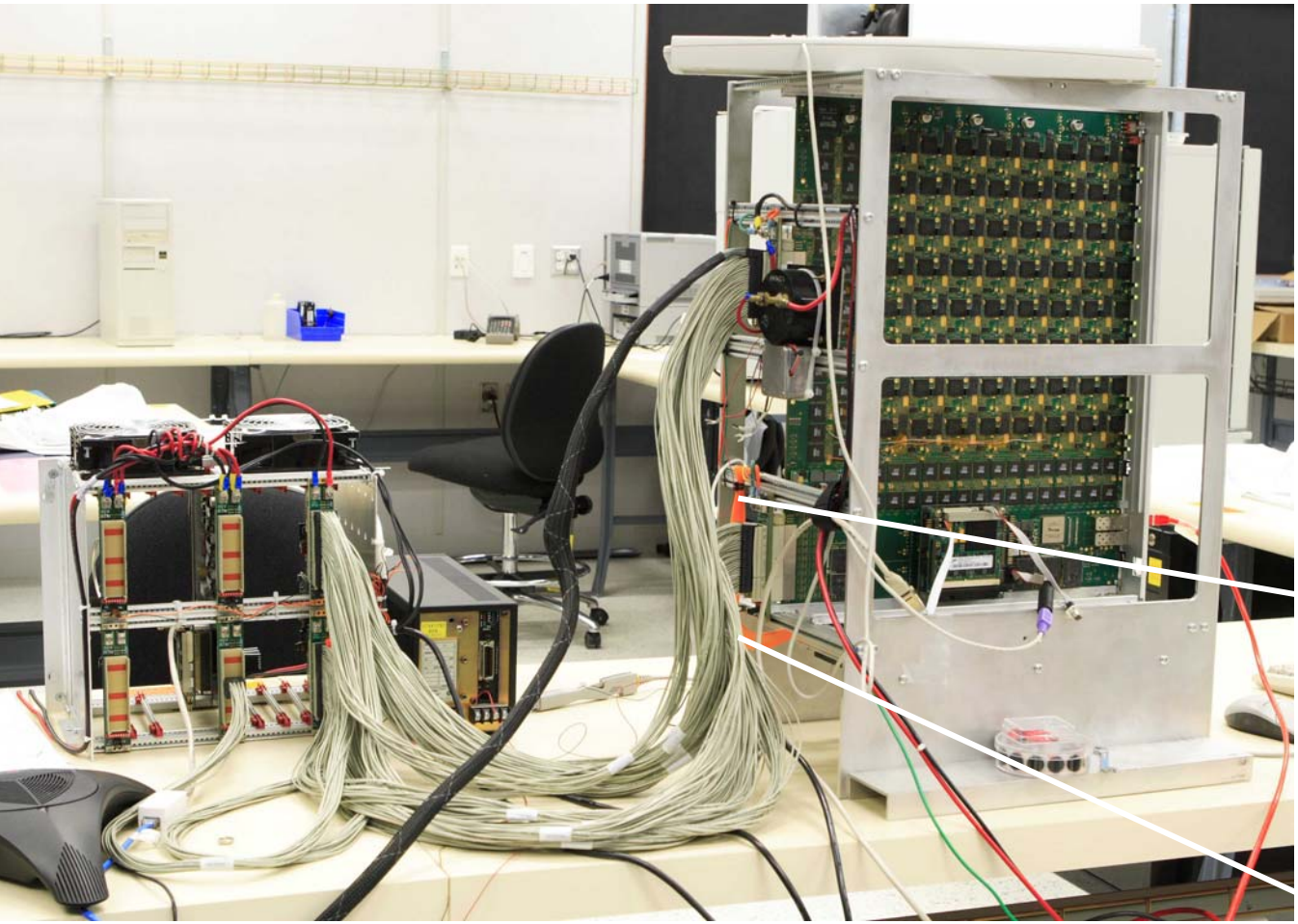
Hardware Prototype/Production Stages

- Stage 1: 1st prototypes – these are in hand now and being tested.
- Stage 2: 2nd prototypes – two of each board (Station and Baseline) will be built, along with 14 bare boards. We will take a chance on the manufacture of bare boards, but not on the value of the parts. Assembly will be held off until Stage 3.
- Stage 3: 3rd prototypes – assembly of remaining boards from Stage 2 (or re-spin boards, if necessary). Use for On-the-Sky tests.
- Stage 4: Full production and production testing of boards.

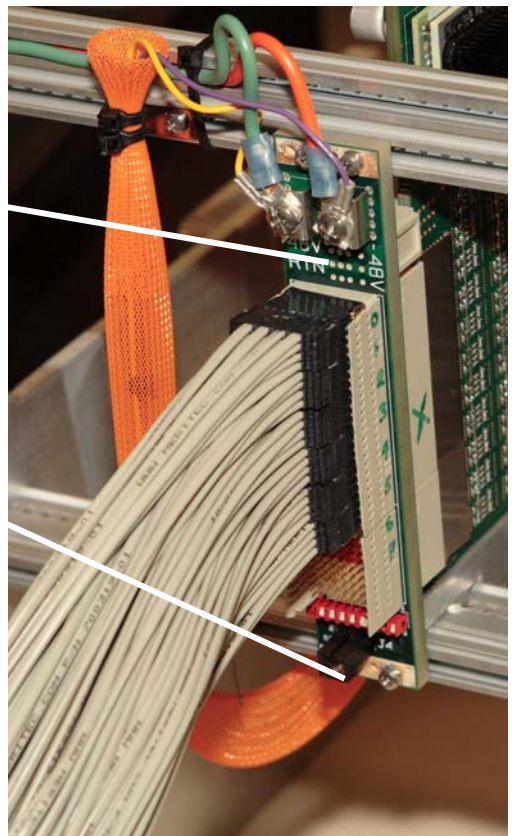
EVLA Correlator Tests – Lab Scenes



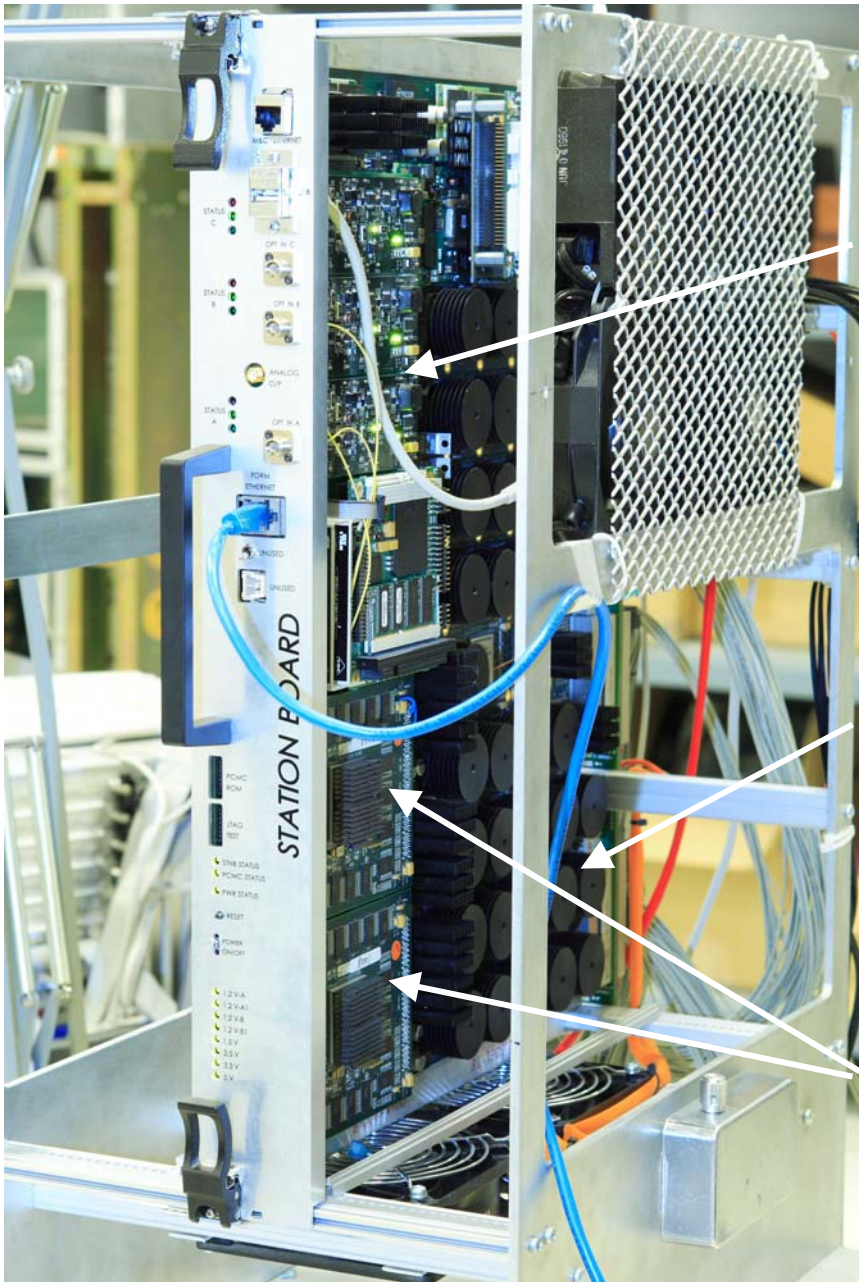
EVLA Correlator Tests – Baseline Board



Connector carrying 32 x 4 = 128 Gbits/s.



EVLA Prototype Station Board

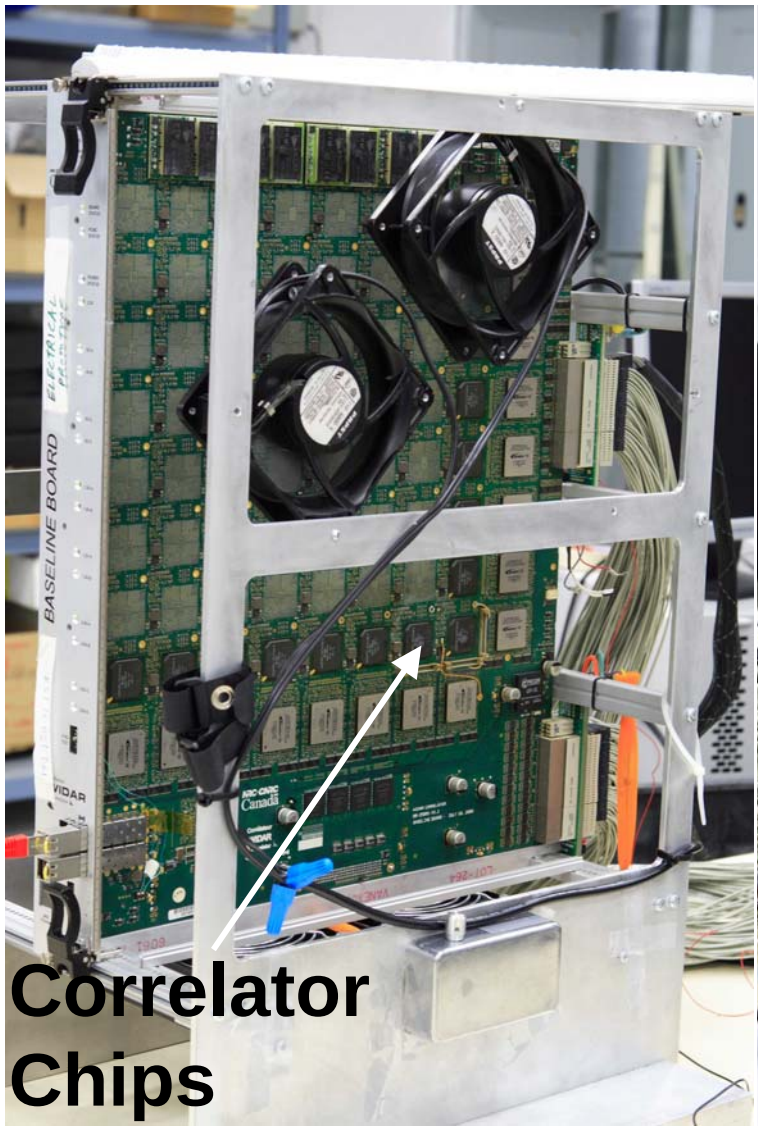


Fiber Optic Receiver Module

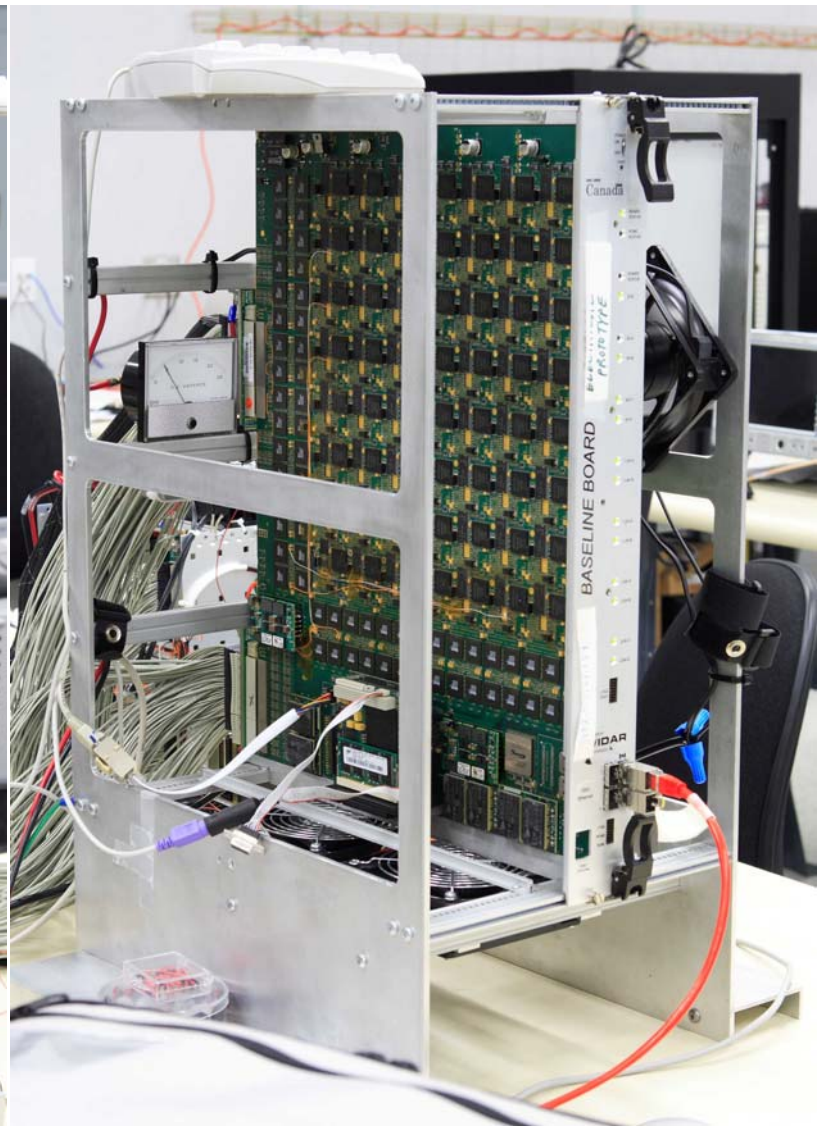
Filter FPGA Chips

Delay Boards

EVLA Prototype Baseline Board

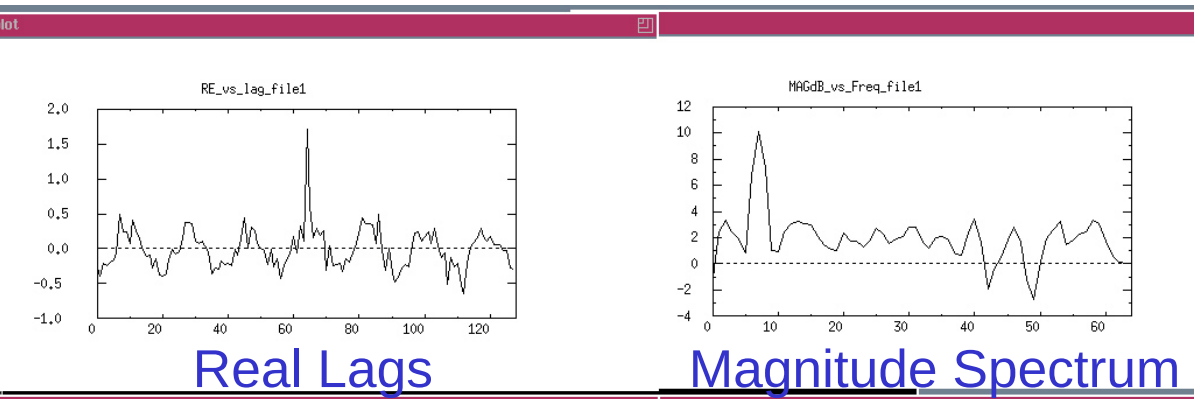


Front Side



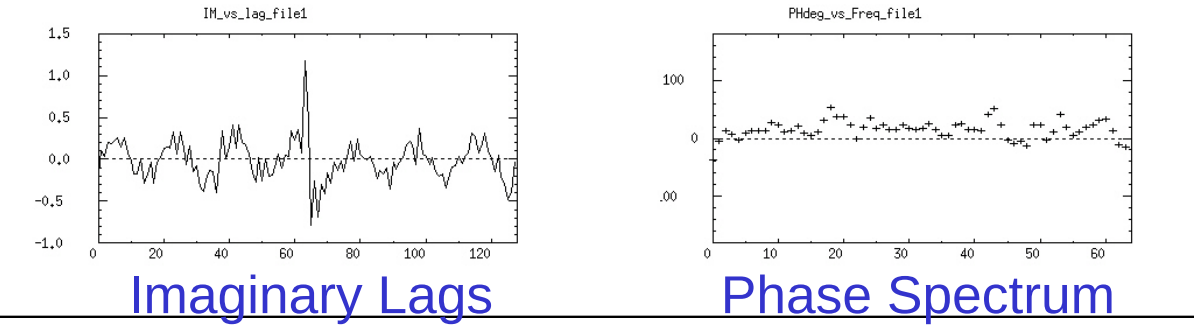
Back Side

First “H/W Fringes” on EVLA Correlator



Real Lags

Magnitude Spectrum



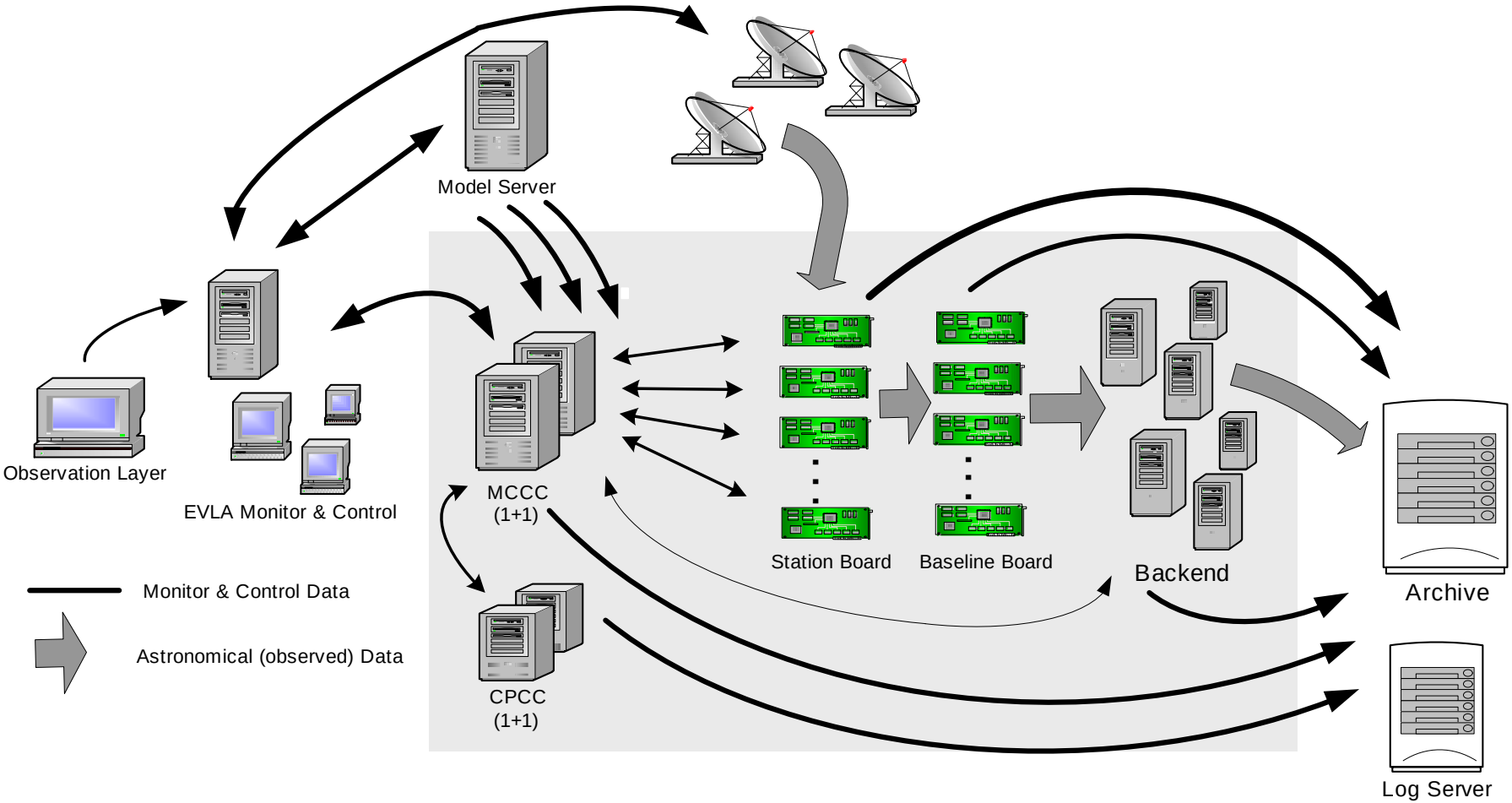
Imaginary Lags

Phase Spectrum

- 128 MHz BW, 4-bit samples, 128 complex lags
- Utilizes 1/16th capacity of one of the 64 chips on the Baseline Board.

- Almost an end-to-end test (data from test generator board).
- Each correlator chip is capable of ~1 GHz bandwidth (4 x 2 pol x 128 MHz).
- Output data rate throttled to ~260 frames/sec for this test.
- Link capable of 110k frames/sec.

Correlator Software System Context

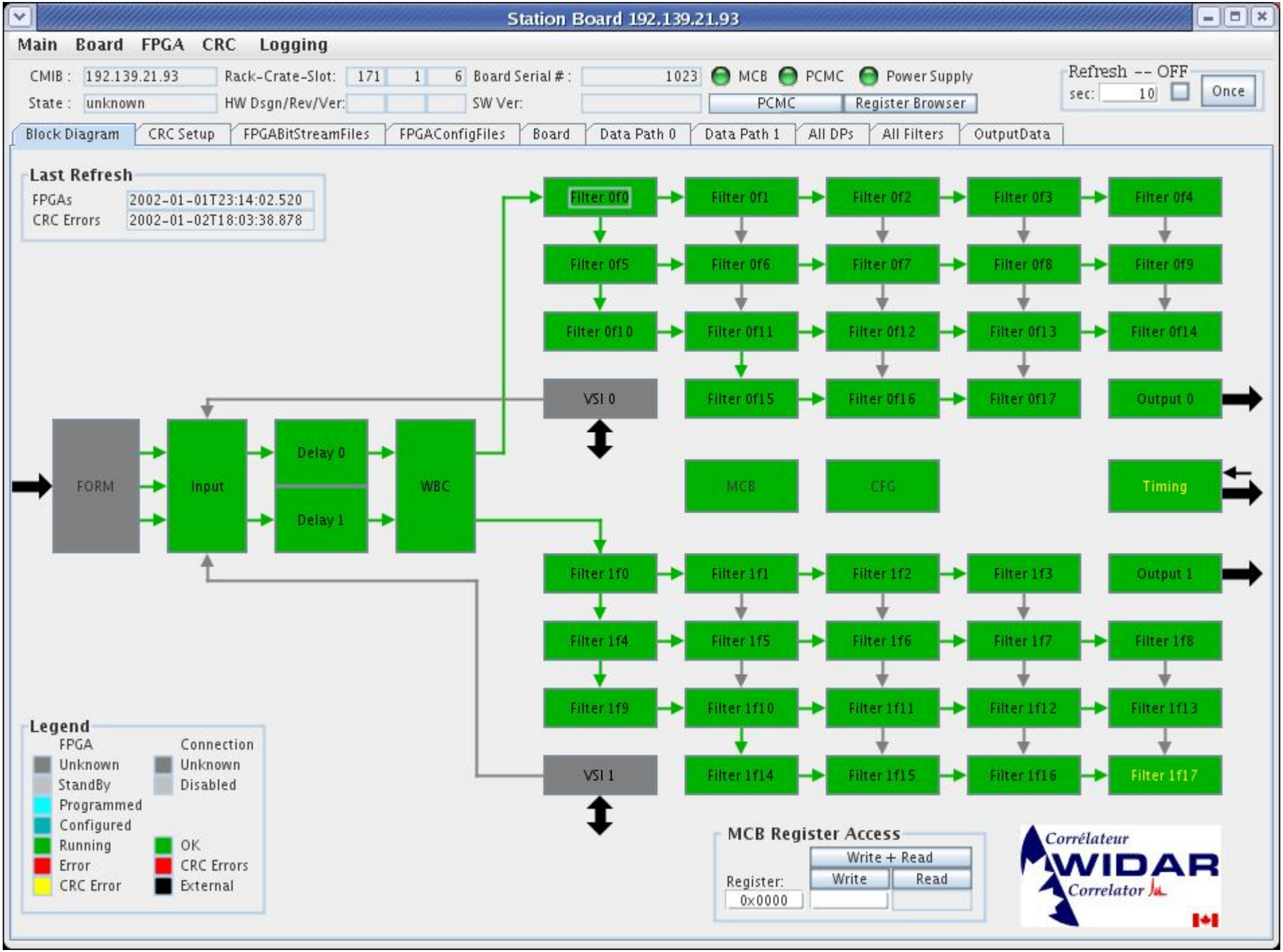


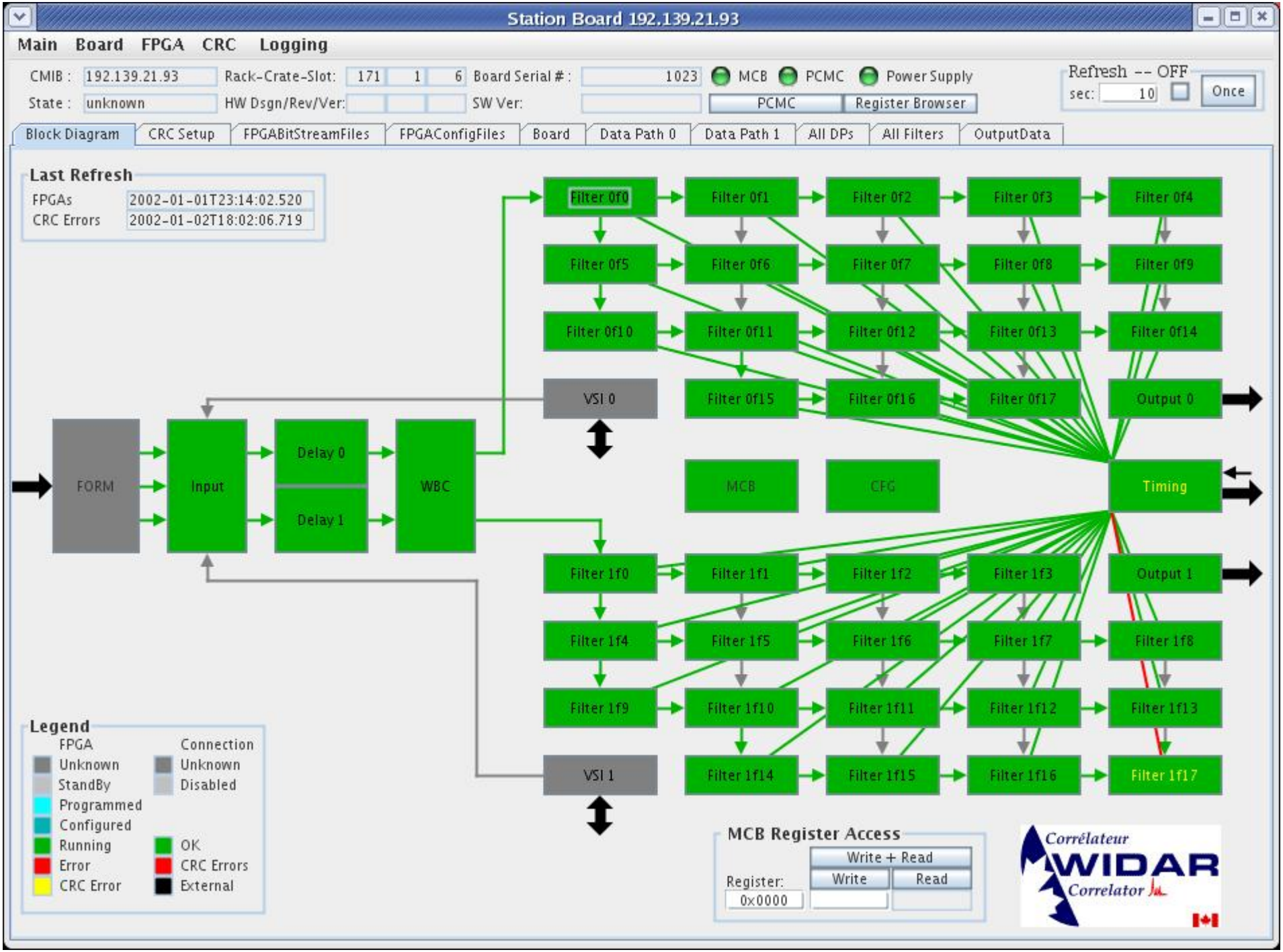
Software Progress

- CMIB & GUI's
  - GUI's provide "engineer's view" of correlator system.
    - Permanent maintenance value.
  - S/W team continues support of prototype board testing.
  - All FPGA's are supported now with Module Access Handlers, GUI's, etc.
- Real-Time Data Display (RTDD)
  - Graphical representation of Station Board output.
  - First release is available, and is being used in the lab.
  - Able to display Station Board output data in real time and to analyze previously stored data.
  - Will likely be used for initial inspection of baseline board data.
- Correlator Back End Software
  - Current state of development sufficient to support on-the-sky testing.
  - Binary Data Format definition and design is near complete.

Software Progress (cont'd)

- Virtual Correlator Interface (VCI) & MCCC software
  - Being updated to handle new connectivity scheme (simpler).
  - Beginning work on implementation.
- Throughput
  - Analysis of throughput done by Sonja Vrcic (Memo 27).
  - Martin Pokorny is working on a second throughput analysis.
- Bottom Line
  - Sufficient software to fully test hardware – hardware is not "just sitting there".
  - If necessary could even collect EVLA data with the addition of delay-model and antenna pointing support.


Station Board 192.139.21.93
Main Board FPGA CRC Logging
CMIB : 192.139.21.93
Rack-Crate-Slot: 171 1 6
Board Serial # : 1023
MCB PCMC Power Supply
State : unknown
HW Dsgn/Rev/Ver:
SW Ver:
PCMC Register Browser
Refresh -- OFF
sec: 10
Once
Block Diagram
CRC Setup
FPGABitStreamFiles
FPGAConfigFiles
Board
Data Path 0
Data Path 1
All DPs
All Filters
OutputData
Last Refresh
FPGAs 2002-01-01T23:14:02.520
CRC Errors 2002-01-02T18:03:38.878
Filter 0f0
Filter 0f1
Filter 0f2
Filter 0f3
Filter 0f4
Filter 0f5
Filter 0f6
Filter 0f7
Filter 0f8
Filter 0f9
Filter 0f10
Filter 0f11
Filter 0f12
Filter 0f13
Filter 0f14
VSI 0
Filter 0f15
Filter 0f16
Filter 0f17
Output 0
FORM
Input
Delay 0
Delay 1
WBC
MCB
CFG
Timing
Filter 1f0
Filter 1f1
Filter 1f2
Filter 1f3
Output 1
Filter 1f4
Filter 1f5
Filter 1f6
Filter 1f7
Filter 1f8
Filter 1f9
Filter 1f10
Filter 1f11
Filter 1f12
Filter 1f13
VSI 1
Filter 1f14
Filter 1f15
Filter 1f16
Filter 1f17
Legend
FPGA
Unknown
StandBy
Programmed
Configured
Running
Error
CRC Error
Connection
Unknown
Disabled
OK
CRC Errors
External
MCB Register Access
Register:
0x0000
Write + Read
Write
Read
Corrélateur
WIDAR
Correlator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Filter 0f0
Filter 0f1
Filter 0f2
Filter 0f3
Filter 0f4
Filter 0f5
Filter 0f6
Filter 0f7
Filter 0f8
Filter 0f9
Filter 0f10
Filter 0f11
Filter 0f12
Filter 0f13
Filter 0f14
VSI 0
Filter 0f15
Filter 0f16
Filter 0f17
Output 0
FORM
Input
Delay 0
Delay 1
WBC
MCB
CFG
Timing
Filter 1f0
Filter 1f1
Filter 1f2
Filter 1f3
Output 1
Filter 1f4
Filter 1f5
Filter 1f6
Filter 1f7
Filter 1f8
Filter 1f9
Filter 1f10
Filter 1f11
Filter 1f12
Filter 1f13
VSI 1
Filter 1f14
Filter 1f15
Filter 1f16
Filter 1f17
Legend
FPGA
Unknown
StandBy
Programmed
Configured
Running
Error
CRC Error
Connection
Unknown
Disabled
OK
CRC Errors
External
MCB Register Access
Write + Read
Write
Read
Register:
0x0000
Corrélateur
WIDAR
Correlator

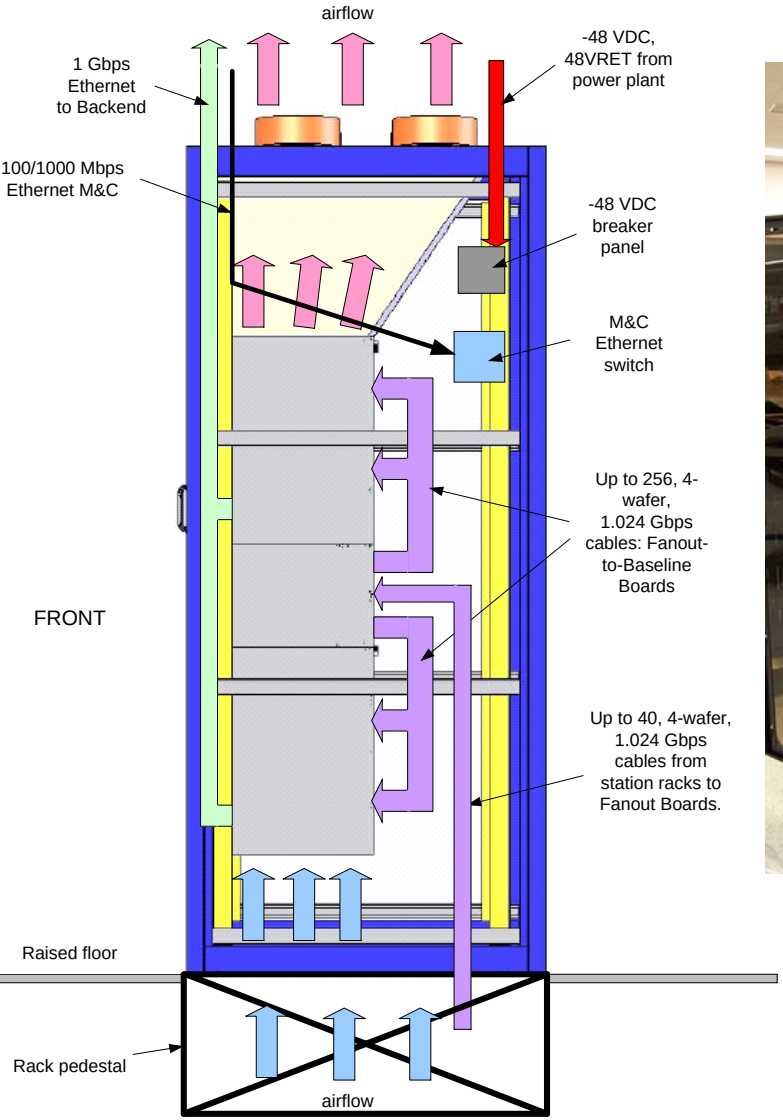
Correlator Software Team

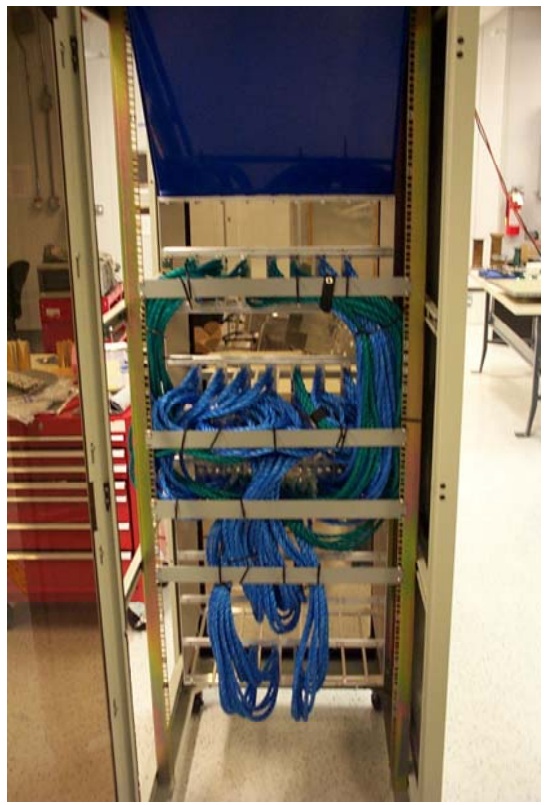
- Substantial (and growing team), commensurate with growing importance of S/W.
- Sonja Vrcic (Penticton)
  - Coordinates overall design and specification.
  - Virtual Correlator Interface (VCI) definition.
  - Master Correlator Control Computer (MCCC) S/W.
- Bruce Rowen & Pete Whiteis (Socorro)
  - Correlator hardware control S/W (CMIB).
- Kevin Ryan (Socorro)
  - GUI development and hardware control S/W.
- Martin Pokorny (Socorro)
  - Correlator Backend software.
- Michael Rupen, Jon Romney, Bryan Butler, Ken Sowinski, Barry Clark, Bill Sahr, Rick Perley, Dave Harland (Socorro).
  - Advisory capacity.

System Progress

- Racks are being ordered in lots of eight.
- Sub-racks and all other mechanical parts are on order.
- Rack Assembly to begin in fall.
  - Contract hire to help with this task.
- Racks to be assembled and tested in lots of eight.
  - Testing will require fully loaded rack for first one.
- Correlator room is complete
  - DC power plant is installed.

Correlator Rack Layout

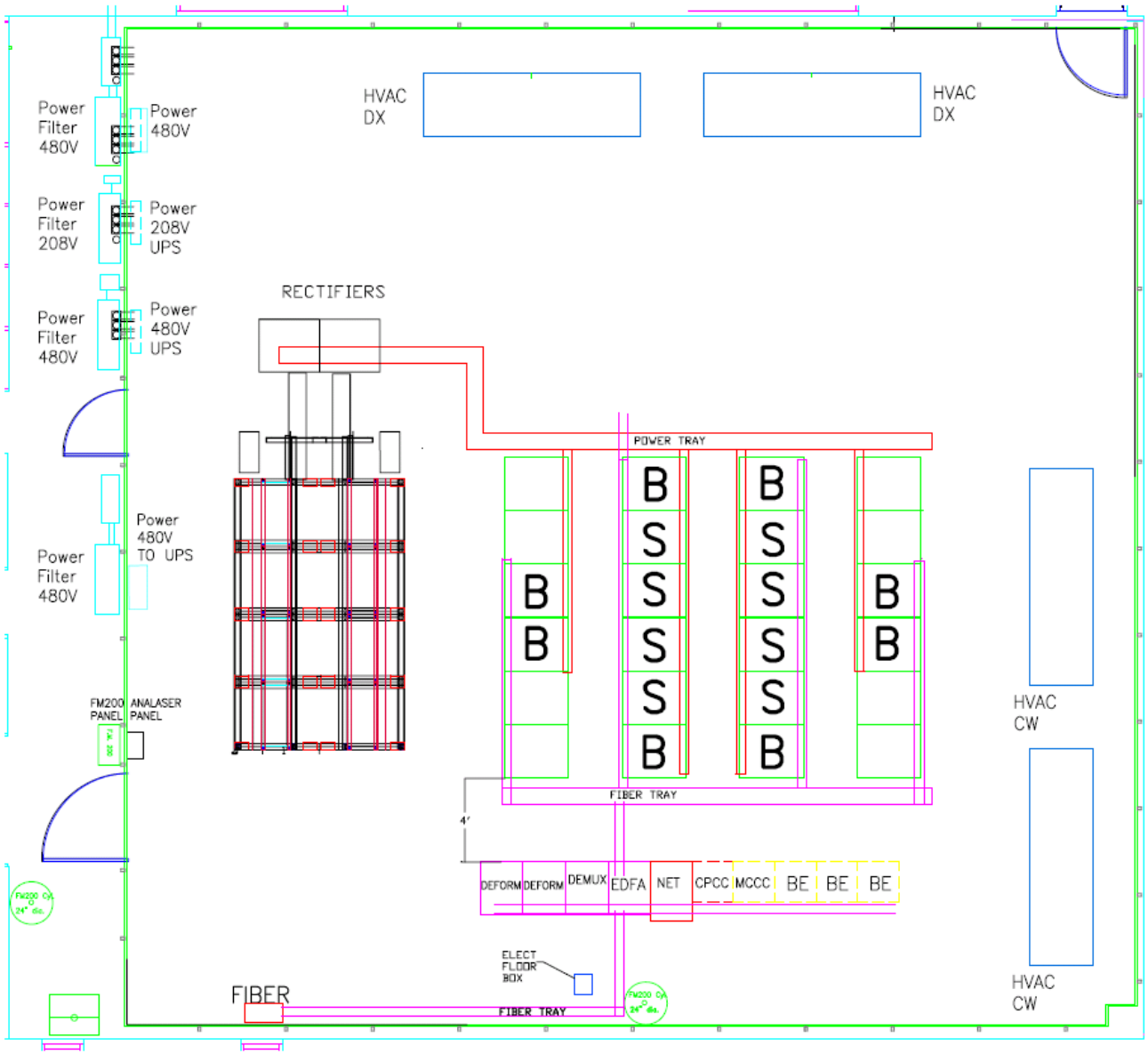




Correlator Room Layout

Room Dimensions

14.6 x 14.3 m



Correlator Testing

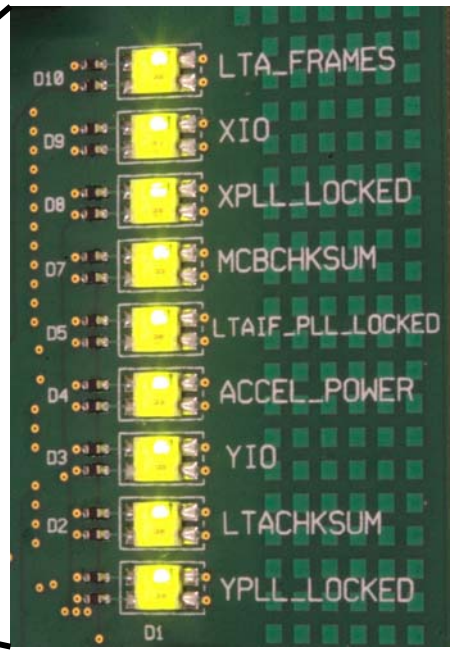
- Stage 1/2: Prototyping and testing.
- Stage 3 Prototype testing
  - 16SB/16BB in racks will form “testable unit sub-systems”, loaded in a way that is very similar to final rack configuration.
  - Subjected to as many tests as possible in lab environment.
  - When complete, the OTS system will be shipped to Socorro.
- On-the-Sky (OTS) – 10-antenna.
  - Principal DRAO purpose is to verify hardware in-system.
  - Long integration times available.
  - Check for HST-style bloopers.
  - See Mark McKinnon & Michael Rupen talks for more info.
- Production Testing
  - Both correlator chips and finished circuit boards will be subjected to temperature cycling and subsequent testing/burn-in before leaving DRAO.
  - Methodology is worked out, but precise details are not.
  - Testing hardware and equipment has been purchased or developed.

EVLA Correlator Chip Function Test Board

- Large Battery of Tests
- Tests done at full clock speed (or slightly higher)
- One chip running successfully for days.

Correlator chip (ZIF) test socket

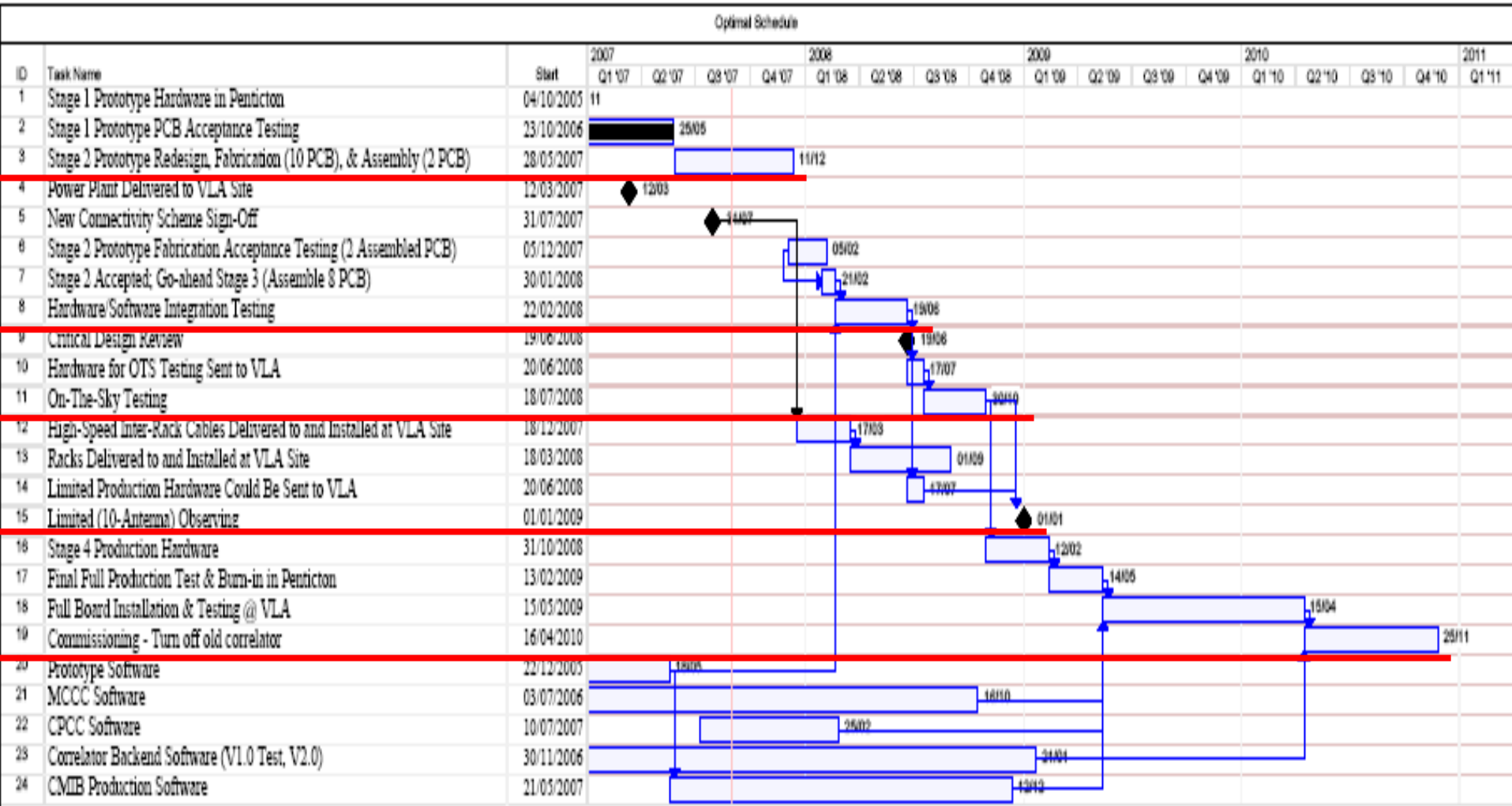
FPGA signal test source



On-the-Sky Testing

- Primary purpose – DRAO led (Critical OTS Tests).
  - Verify Hardware so that production phase can proceed.
  - Long integration times available.
  - Check for HST-style bloopers.
- Secondary Purpose – NRAO led.
  - Integration of a “small” system with EVLA software.
  - Testing of such, and further checks of software through-put.
- Tertiary Purpose – NRAO led.
  - Test wide-band observing.
  - Develop wide-band calibration techniques.
- Quaternary Purpose – NRAO led.
  - Look at wide-band RFI environment.
  - Develop evasion/expurgation measures.
- Quinary Purpose – NRAO led.
  - Carry out early observations where possible.

Correlator Summary Schedule

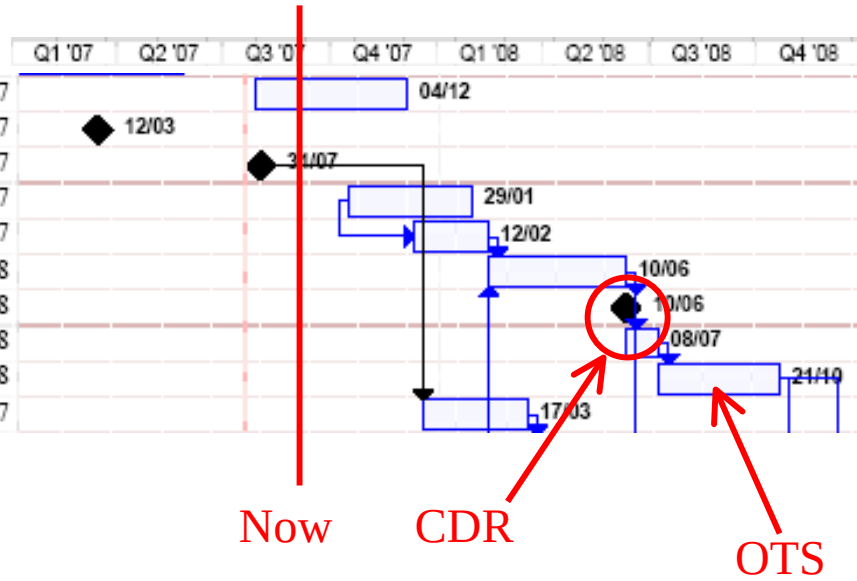


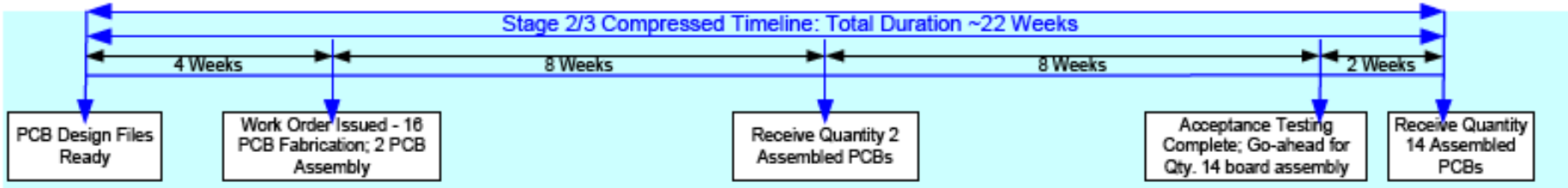
Note on CDR Timing

- Current plan is to hold CDR
  - Before the OTS tests,
  - After the DRAO "hardware/software integration" tests.
- This provides the CDR committee with the opportunity
  - to review lab performance in its entirety and possibly suggest extensions.
  - to review suggested "critical OTS" tests and suggest alternatives or additional tests.
- CDR committee will be informed of OTS results by email and asked for a quick ratification.
- CDR committee makes recommendations, not final decisions.

“Compressed” Schedule (Best Case)

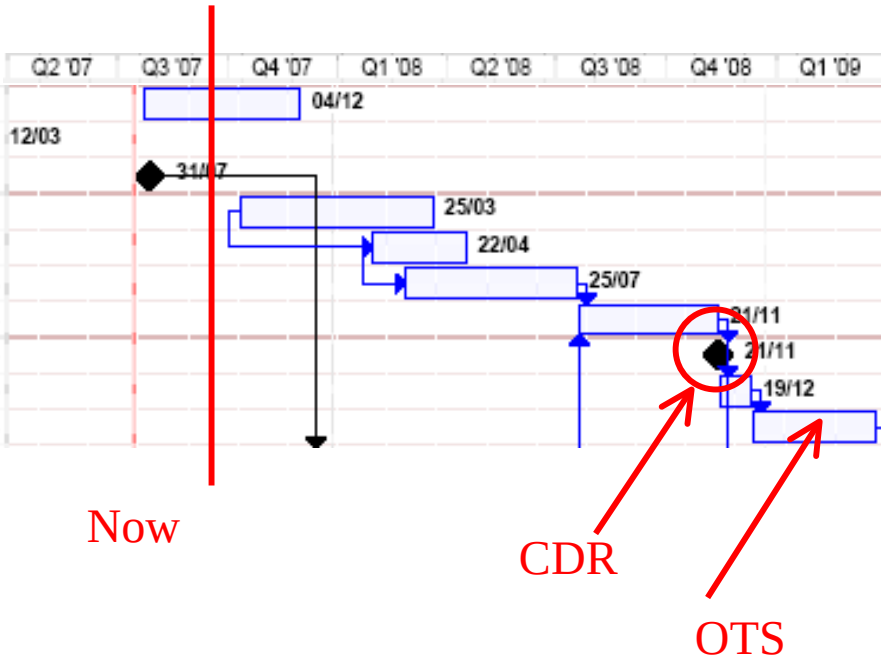
Stage 2 Prototype Fabrication (16 PCB) & Assembly (2 PCB)	27/07/2007
Power Plant Delivered to VLA Site	12/03/2007
New Connectivity Scheme Sign-Off	31/07/2007
Stage 2 Prototype Fabrication Acceptance Testing (2 Assembled PCB)	15/10/2007
Stage 2 Accepted; Go-ahead Stage 3 (Asssemble 14 PCB)	10/12/2007
Hardware/Software Integration Testing	13/02/2008
Critical Design Review	10/06/2008
Hardware for OTS Testing Sent to VLA	11/06/2008
On-The-Sky Testing	09/07/2008
High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site	18/12/2007

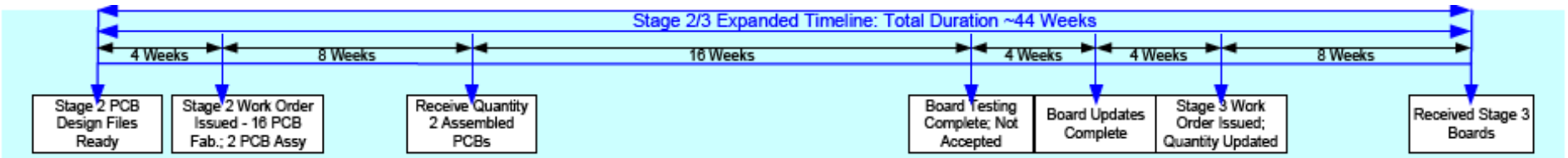




“Expanded” Schedule

Stage 2 Prototype Fabrication (16 PCB) & Assembly (2 PCB)	27/07/2007
Power Plant Delivered to VLA Site	12/03/2007
New Connectivity Scheme Sign-Off	31/07/2007
Stage 2 Prototype Fabrication Acceptance Testing (2 Assembled PCB)	15/10/2007
Stage 2 Not Accepted; Design Updates	04/02/2008
Stage 3 Work Order Issued & Hardware Built	03/03/2008
Hardware/Software Integration Testing	28/07/2008
Critical Design Review	21/11/2008
Hardware for OTS Testing Sent to VLA	24/11/2008
On-The-Sky Testing	22/12/2008

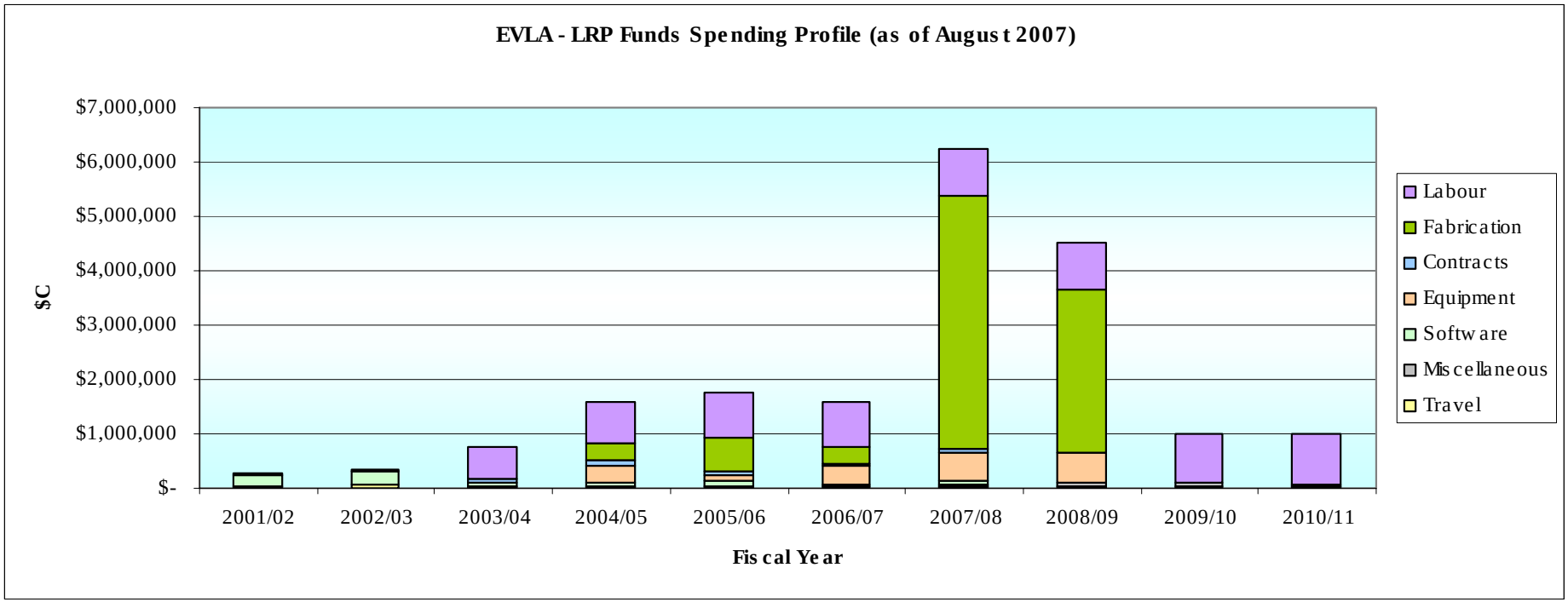




Funding in Canada

- Aug/03 – Canadian Treasury Board approval of submitted budget ($C 20M over 5 years).
  - Five-year period is up in Mar 31, 2008.
  - Time extension required
    - Not guaranteed – documentation submitted.
- Documentation has been submitted.
- Actual budget is healthy but not flush.
  - Contingency diminishing.
  - Risks are also diminishing.

Correlator Projected Spending Profile



Non-Technical Program Risks

- Funding
  - Time extension is required as already noted.
  - Small risk, but could lead to delays, questions, etc.
- Schedule slippage?
  - Technical progress slower than the deliberately aggressive initial schedule.
  - Unexpected “Re-spins” will present additional schedule risk.
  - Concerns over procurement processes.
    - This risk is retired.
- Inadequate contingency?
  - Contingency now small.
  - Cost risk greatly reduced now that prototypes are tested and parts prices most fixed.
  - Manufacturing cost remains a risk.
  - Exchange-rate changes have been favourable to date.
  - Labour costs continue.
  - New connectivity scheme has brought back small contingency.

Technical Program Risks

- Technical risk is greatly reduced since May 2006.
  - Prototype hardware has been thoroughly tested in the lab, although this is not quite over.
- Manufacturing should be fairly risk-free, but ….
- Assembly into a final system could present risk.
- Software completion could present a schedule risk.

Descoping

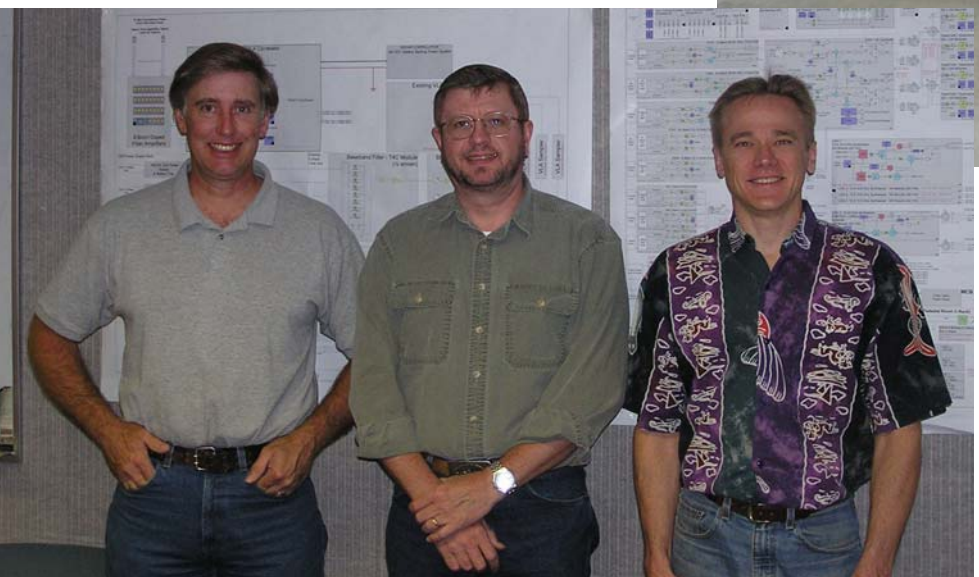
- Unlikely to be required.
- Difficult to see what can be descoped at this stage.
  - Would need to be presented with a problem before spending time thinking about this.

Project Summary

- Are we meeting the required schedule?
  - We may be about a year later than original delivery date.
- Are we over budget at this stage?
  - Budget is slimly allocated, but we are not over budget.
- Are we planning to deliver on what we said we would do?
  - Yes, with minor improvements.
- What are the major risks at this stage?
  - Hypothetical funding difficulty after Mar 31 2008.

EVLA Correlator Group

DRAO-based.



NRAO-based.

End