

The EVLA Correlator

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Outline

1. Correlator Performance Goals
2. Hardware Progress
3. Software Progress
4. System Progress
5. Prototype Testing
6. Installation Estimates
7. Funding, Budget & Schedule
8. Risk Issues

Key EVLA Processing Capabilities

Deep Imaging Polarization

- ✓ 8 GHz Bandwidth (dual polarization).
- ✓ Full polarization processing.
- ✓ Wide-field imaging.

Narrow spectral lines Wideband searches

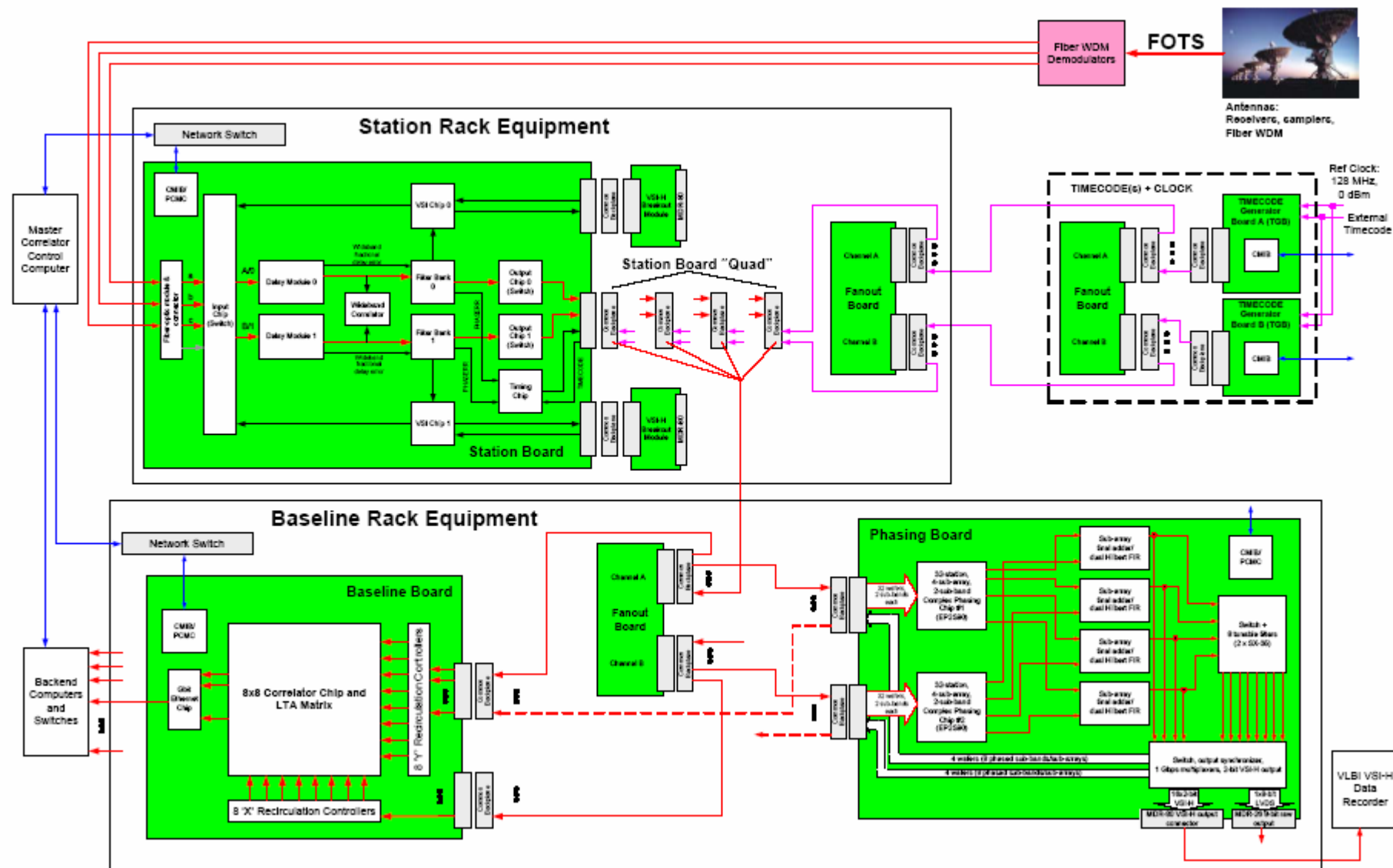
- ✓ 16,000 channels at max. bandwidth (BW).
- ✓ $>10^6$ channels at narrow BWs.
- ✓ Spectral resolution to match any linewidth.
- ✓ Spectral polarization (Zeeman Splitting).

Flexibility Many resources

- ✓ 8 tunable 2 GHz wide bands.
- ✓ Each band - 16 tunable sub-bands.
- ✓ Sub-band – independent spectral resolution.
- ✓ Simultaneous line and continuum.

High time resolution

- ✓ 1000 pulsar “phase bins”.
- ✓ “Single-dish” data output to user instruments.
- ✓ Very fast time sampling ($<20 \mu\text{s}$).





Significant Events Since Dec. 2004

- Correlator Chip CDR – Jan/05
- Software Review – Jan/05.
- Correlator Preliminary Design Review – July/05.
- PCB fabricator contract signed – Jan/06.
- Prototype Correlator chip wafers fab'd – Feb/06.
- Software Review – Mar/06.
- Prototype chip delivery – early Jun/06.
- Baseline Board prototype delivery – Jun/06.
- Station Board prototype delivery – est. Aug/06.

Hardware Progress

- FPGA's
 - All FPGA's are designed, including the Filter Chip.
- Station board
 - Layout is close to completion, including Design-for-Manufacture approval.
 - Presently undergoing signal integrity simulation.
 - Prototype fabrication order expected in June.
- Baseline Board
 - Prototype fabrication under way.
- Phasing board
 - Draft specification (RFS) released.
 - Deferred in time but not reduced in priority.
- Other boards
 - Prototypes for all other boards already fabricated.
 - Fan-out board needs redesign for better signal margins.
- System
 - Racks designed and prototyped; thermal analysis done.
 - Power system RFP draft written.
 - Reliability analysis system in place – first draft of analysis complete.

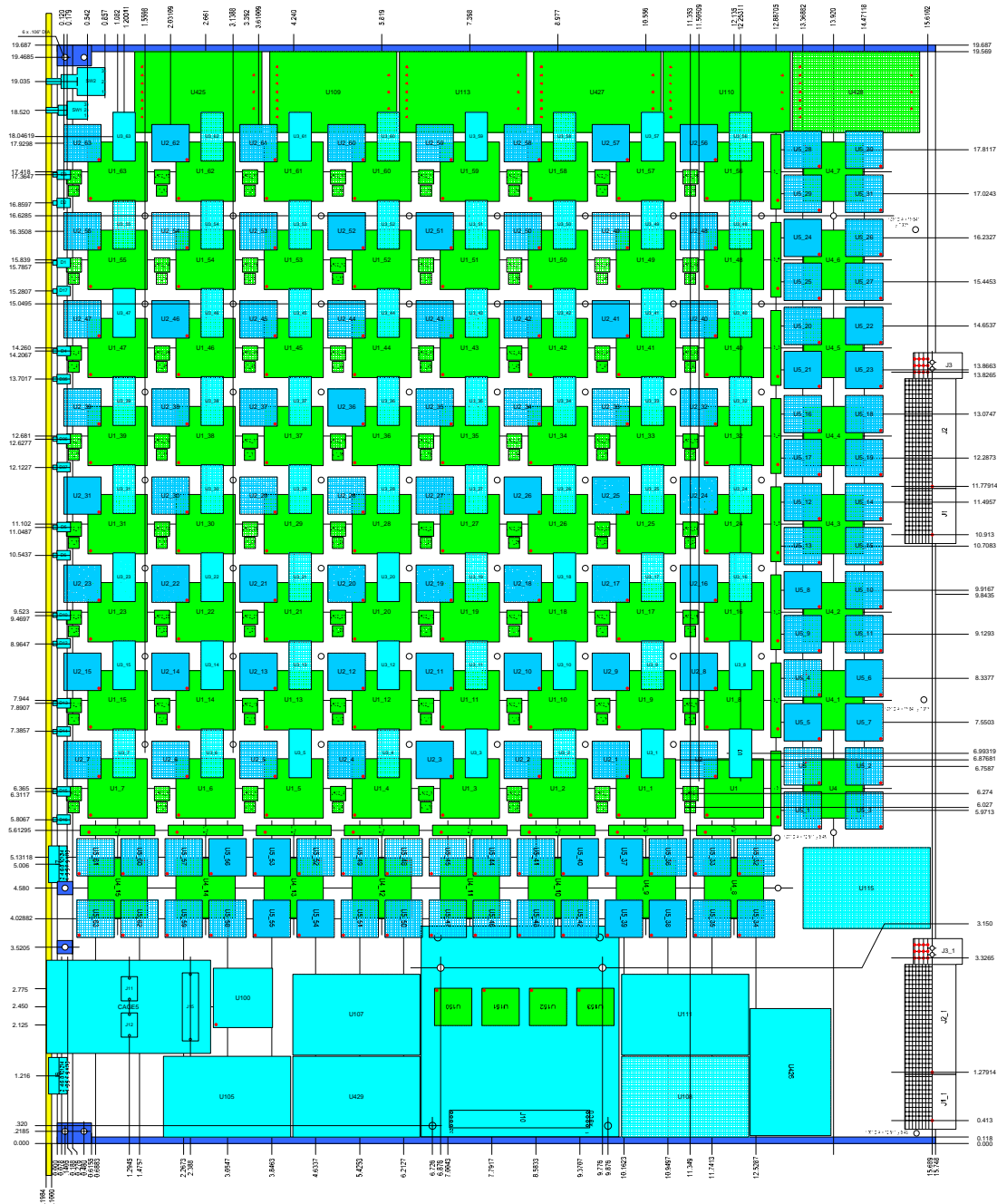
Station Board Layout

- “Daughter” Board - brown.
- Power Supplies – pink.
- FPGA’s – Green
- Connectors – light brown and white.
- ~5000 parts.
- 140 required for EVLA.



- Green chips – front side.
- Blue chips – back side.
- 8 x 8 array of correlator chips.
- LTA chips on the back side.
- Recirculation Controller.
- ~12000 parts
- ~177 required for EVLA.

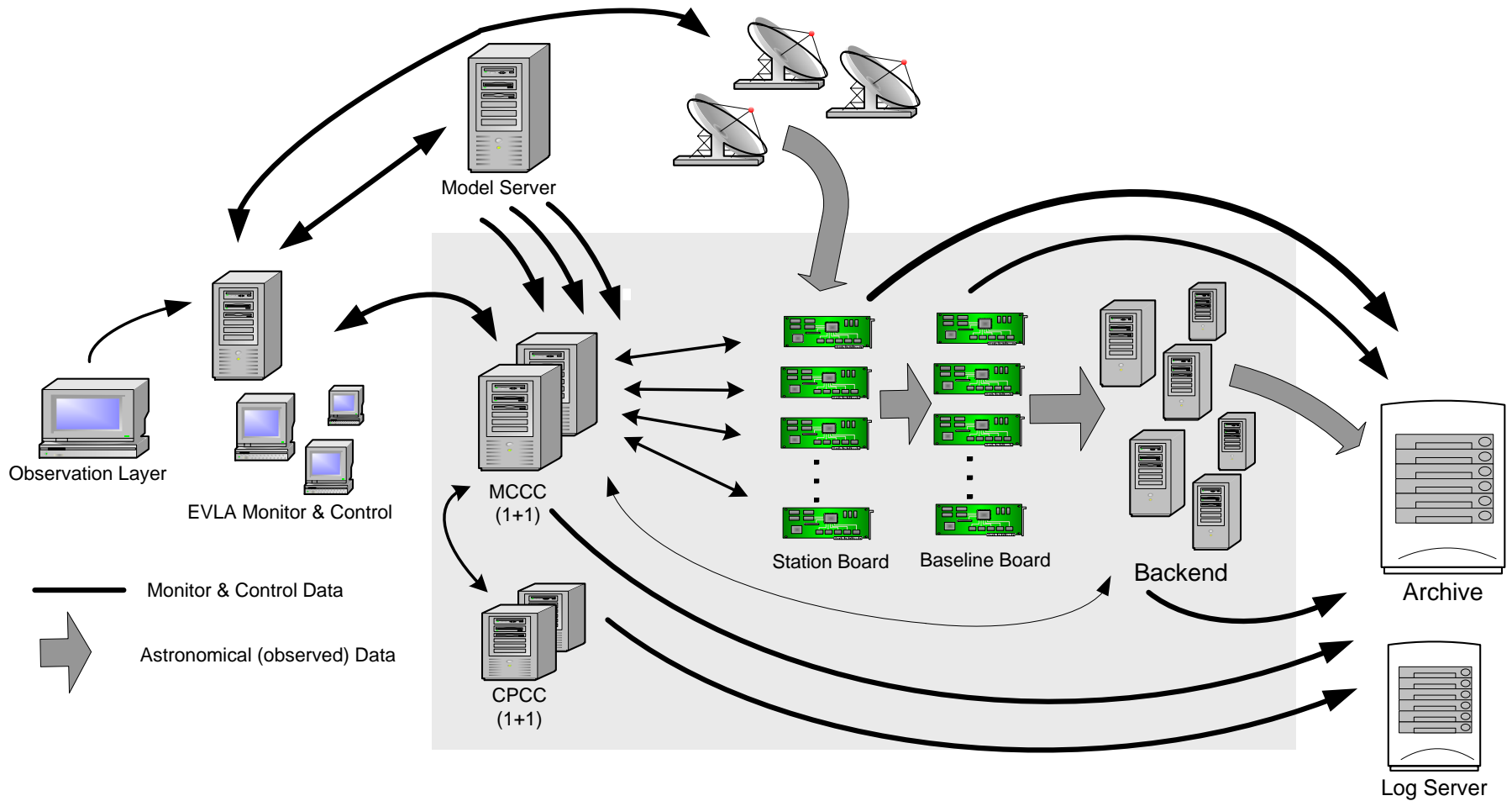
NRC - CNRC



Software Progress

- GUI-based prototype testing software
 - Complete enough to be useful already.
 - All FPGA's covered except Phasing Board.
 - **Provides “engineer’s view of correlator system.”**
 - **Permanent maintenance value.**
 - Top-level GUI's now under development.
- Virtual Correlator Interface
 - Well defined except for correlator output area.
 - Communications protocol well defined except for transport layer.
- Master Correlator Control Computer (MCCC)
 - Work deferred for GUI development.
 - Architecture/scope well defined.
- Real-time control software
 - “CMIB” processor on each board.
 - Operating system has been working for a long time.
 - XML-based communication with “outside world”.
 - Drivers for FPGA's are well under way.

Correlator Software System Context



Correlator System GUI

WIDAR Correlator - Top level system view (40 stations configuration)
Main

MCCC 1
Active

MCCC 2
Standby

CPCC 1
Standby

CPCC 2
Active

Backend

Log Server

Boot Server

Rack 001

Rack 002

Rack 003

Rack 004

Rack 005

Rack 006

Rack 007

Rack 008

Rack 009

Rack 010

Rack 100

Rack 101

Rack 102

Rack 103

Rack 104

Rack 105

Rack 106

Rack 107

Rack 008

Rack 109

Rack 110

Rack 111

Rack 112

Rack 113

Rack 114

Rack 115

Power Systems

Heating and Cooling

	TGM 0	TGM 1
Board	101-1-7	110-1-7
Status	Running	Running
Time 0	2007-123-09:45:34.010	2007-123-09:45:34.010
Time 1		
Time 2		
	Details	Details

Observation	Start Time	Status
V013Q22	2007-123-09:30:00.000	In progress
V013Q23	2007-123-10:35:30.000	Accepted
V021A90	2007-123-09:45:34.000	In progress
V014Q01	2007-124:11:05:00.000	Rejected
V01V22	2007-122:23:30:00.000	In progress
V01V23	2007-123-10:15:00.000	Accepted
Test21	2007-123-09:30:00.000	In progress

Antenna	Quad	#Boards	Board1	Board2
EVLA01	01	4	001-0-0	001-0-1
EVLA02	02	4	001-0-4	001-0-5
EVLA03	03	4	001-1-0	001-1-1
EVLA04	04	4	001-1-4	001-1-5
EVLA05	05	2	002-0-0	002-0-1
EVLA06	05	2	002-0-2	002-0-3
EVLA07	06	2	002-0-4	002-0-5

Individual Rack

WIDAR Correlator - Rack

Main

Rack 001

Crate 0

0

1

2

3

4

5

6

7

Station Board

Station Board

Station Board

Station Board

Baseline Board

TIMECODE Gen

Crate 1

0

1

2

3

4

5

6

7

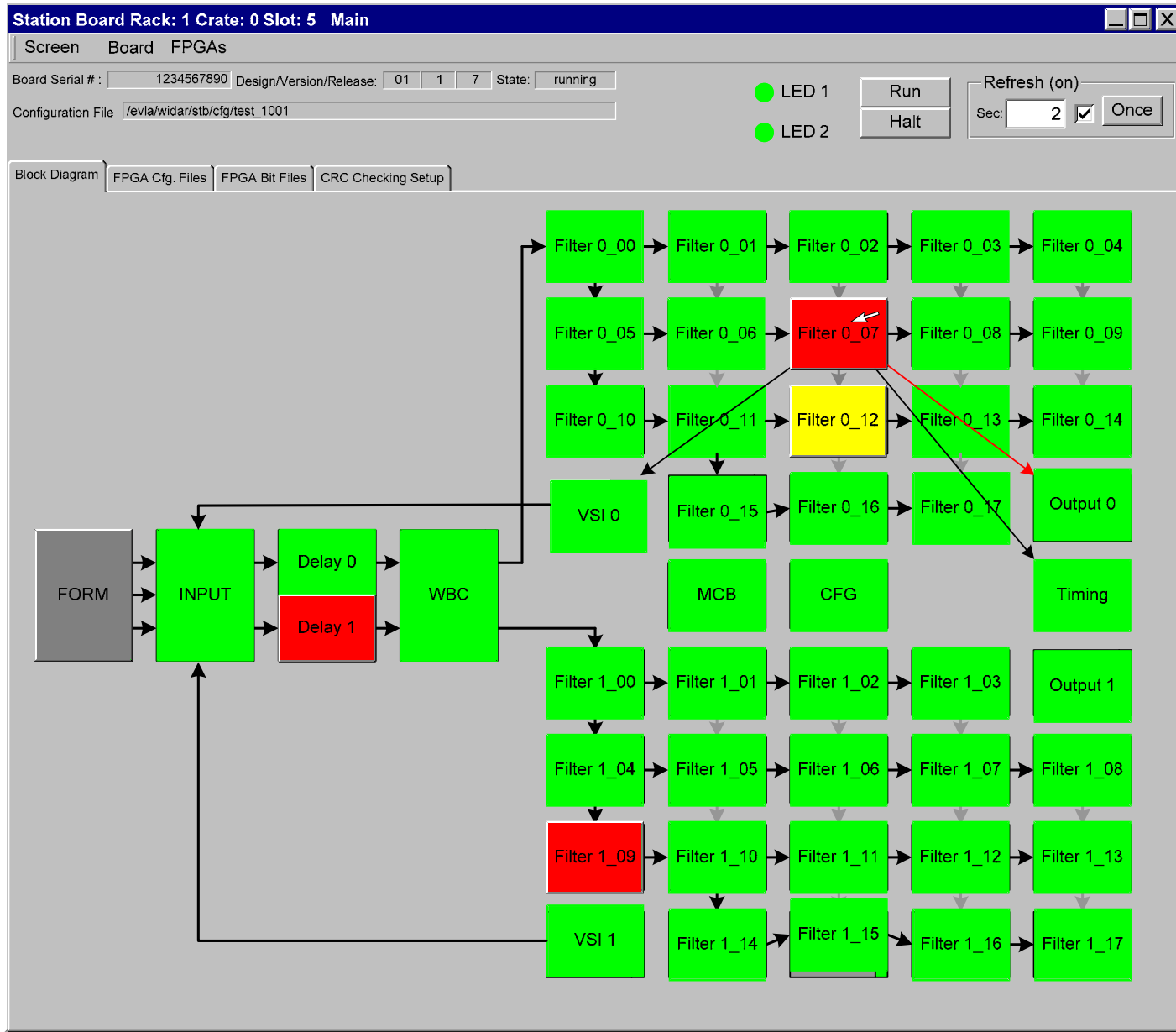
Board	Status	IP	Type
0	OK	123.23.1.1	STB
1	OK	123.23.1.9	STB
2	OK	123.23.1.17	STB
3	Initializing	123.23.1.25	STB
4	OK	123.23.1.34	BLB
5	---		
6	---		
7	OK	123.23.1.60	TGM
8	---		
9	---		
10	---		
11	---		
12	---		
13	---		
14	---		
15	---		

Operator Log

2007-90-11:15 Replaced STB1

2007-89-13:45 Initial installation

Station Board Top Level



Filter Control GUI

Station Board Rack: 1 Crate: 0 Slot : 5 Filter 0_12

Screen Configuration Hardware

General

Design/Revision/Version: 01 1 7 State: running
Configuration File /evla/widar/stb/filter/cfg_01.xml Browse
FPGA Bit File /evla/widar/stb/filter/bit/abc Browse

VCI

Input band width (MHz): 2048 Setup
Input # bits: 3
Input # bands: 1 Fbit:
Input band: 1 Flip:
Output band width (MHz): 128.0000 Mix:
Output band center (MHz): 192.0000000 LSB:
Output # bits: 4
Accumulation (interrupts): 100
Results file: /evla/widar/stb/filter/fm/out/abc Browse

Status

Input delay calibration:
Input delay adjust:
System clock:
Delay Module Input:
Read/Write:
Reset status indicators

CRC

Auto
View Error Counts
Reset Error Counts

Format

Output File: /evla/widar/stb/filter/fm/out/abc Browse
Select Data: 4 Power on 12345 off 12344
Valid on 313 off 312
Select Clip: 1 Clip Count 1234567
RFI Detect Level: 0x17534 RFI Detections 2
RFI Detect Length: 256
Sideband Flipper On
Quantizer Scaling: 0x1234 Quantizer Power 1234567
Quantizer # Bits: 4 Quantizer Clip Count 1
Quantized State: Auto -3 Quantizer State Count 4 Histogram
TEX Trig File /evla/widar/stb/filter/fm/tex/trig/abc Browse
TEX Phase Model External
TEX Phase: 0x12345678 TEX Valid 625
TEX Phase Rate: 0xFEDCBA9 TEX Sums cos 1234 sin 252

Read/Write Registers

Read Write Write/Read
Register: Write: Read:

Refresh

Sec: Once

Test Port

TP0 TP1 TP2 TP3
5 17 255 33

InOut

Input: A Output Enable: A B
Input Delay: 37 Daisy Delay: 112
Time Interval : 1234567

Delay

Data Input Rate: 0 Demux Factor: 15
Delay Model: External Phase Factor: 0x4000
Delay: 123456 Delay Rate: 0

Stage 1

Product File: /evla/widar/stb/filter/s1prd/abc Browse
Data Output Rate: 0 XBAR
Invalid Stretch Length : 32 Filter Delay : 16
Scale Factor : 1 Number of Taps : 512

Mixer

Mixer Trig File /evla/widar/stb/filter/s2mix/abc Browse
Use mixer Mixer Phase Model: External
Phase: 0x00000000
Phase Rate 0xFEDCBA9

Stage 2

Coefficient file /evla/widar/stb/filter/s2cof/abc Browse
Output Rate: 4 Calculation Rate: 0
Invalid Stretch Length : 32 Filter Delay : 16
Scale Factor : 1 Number of Taps 512

Stage 3

Coefficient file /evla/widar/stb/filter/s3cof/abc Browse
Output Rate: 8 Calculation Rate: 0
Invalid Stretch Length : 32 Filter Delay : 16
Scale Factor : 1 Number of Taps 512

Stage 4

Coefficient file /evla/widar/stb/filter/s4cof/abc Browse
Output Rate: 12 Calculation Rate: 0
Invalid Stretch Length : 32 Filter Delay : 16
Scale Factor : 1 Number of Taps 512

Correlator Software People

- **Sonja Vrcic (Penticton)**
 - Coordinates overall design and specification.
 - Virtual Correlator Interface (VCI) definition.
 - Master Correlator Control Computer (MCCC) S/W.
- **Bruce Rowen (Socorro)**
 - Correlator hardware control S/W (CMIB).
- **Kevin Ryan (Socorro)**
 - GUI development and hardware control S/W.
- **Martin Pokorny (Socorro)**
 - Correlator Backend software.
- **Michael Rupen, John Romney, Bryan Butler, Ken Sowinski, Barry Clark, Bill Sahr (Socorro)**
 - Advisory capacity.

Correlator-related Software Issues

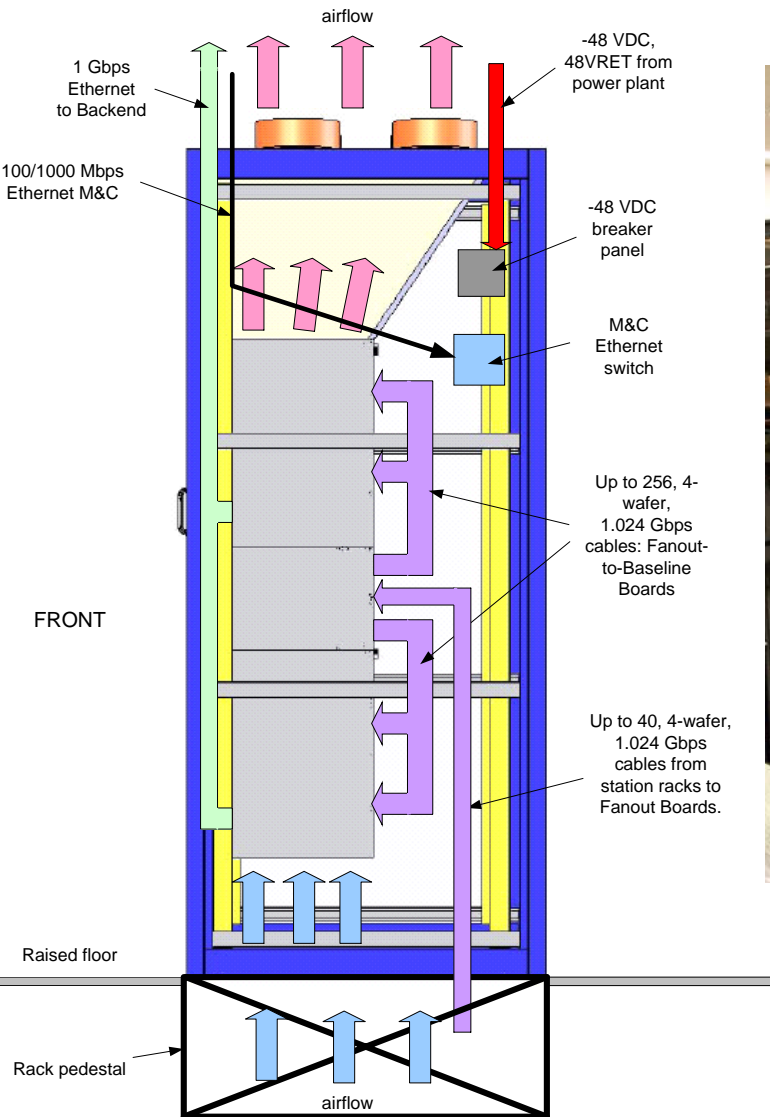
- Correlator output: ALMA Science Data Model (ASDM) must be qualified for EVLA use.
 - On the surface ASDM looks all right in the sense that additions can be made to meet EVLA requirements.
 - Is ALMA effort required and is it available?
 - This issue is to be addressed later in the series of presentations.
- Preliminary plans to add “blocks” in the Correlator Back End (CBE).
 - Additional Ethernet Switch and output Fast Data Formatter computer(s).
 - Formatting to ASDM spec’s will probably take place in the Fast Data Formatter.
 - Details to be worked out.
- Virtual Correlator Interface (VCI) Transport protocol is to be defined.
- Potential unknown throughput issues could arise.

System Progress

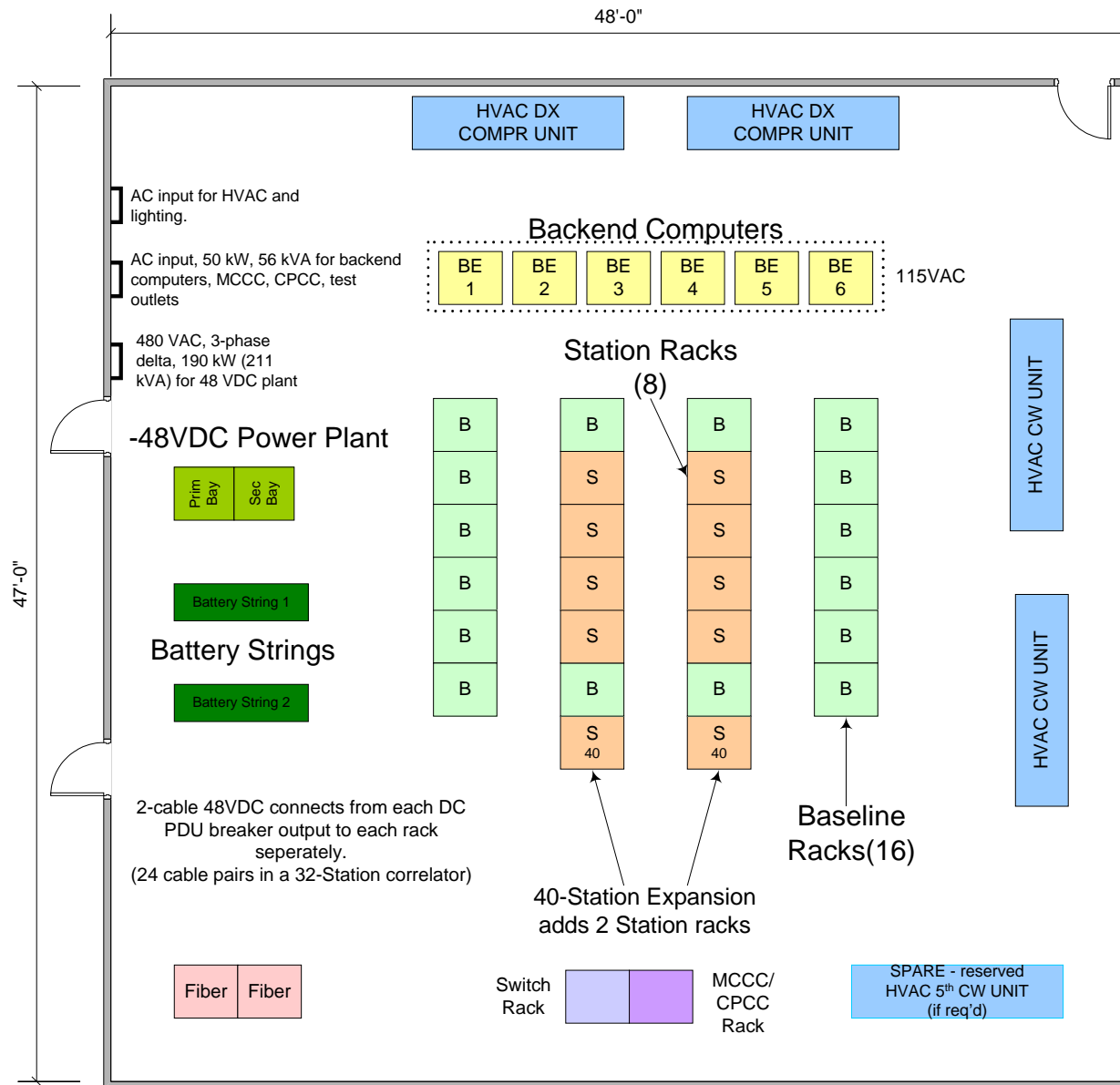
- **NRAO work on correlator room is progressing rapidly.**
- **Design of overall room layout is complete.**
- **Environmental specifications have been developed.**
 - Air flow & temperature: ~1700 cfm per rack, 15 °C.
 - ElectroStatic Discharge (ESD)
 - 90 nm devices used extensively (<1/1000 thickness of human hair)
 - Humidity specs.
 - Strict handling and servicing procedures.
 - Air quality
 - ISO 14644-1 class 8 + MERV 13 filter.
- **Racks**
 - “Thermal prototypes” have been built and tested.
 - “Mechanical prototypes” ditto.
 - Preliminary fabrication plan is being developed.
- **Preliminary installation plan is being developed.**
- **Power plant specifications/RFP draft written for acquisition this fiscal year (ends Mar 31/07).**

5 for 4 2006

Correlator Rack Layout



Correlator Room Layout



ElectroStatic Discharge (ESD)



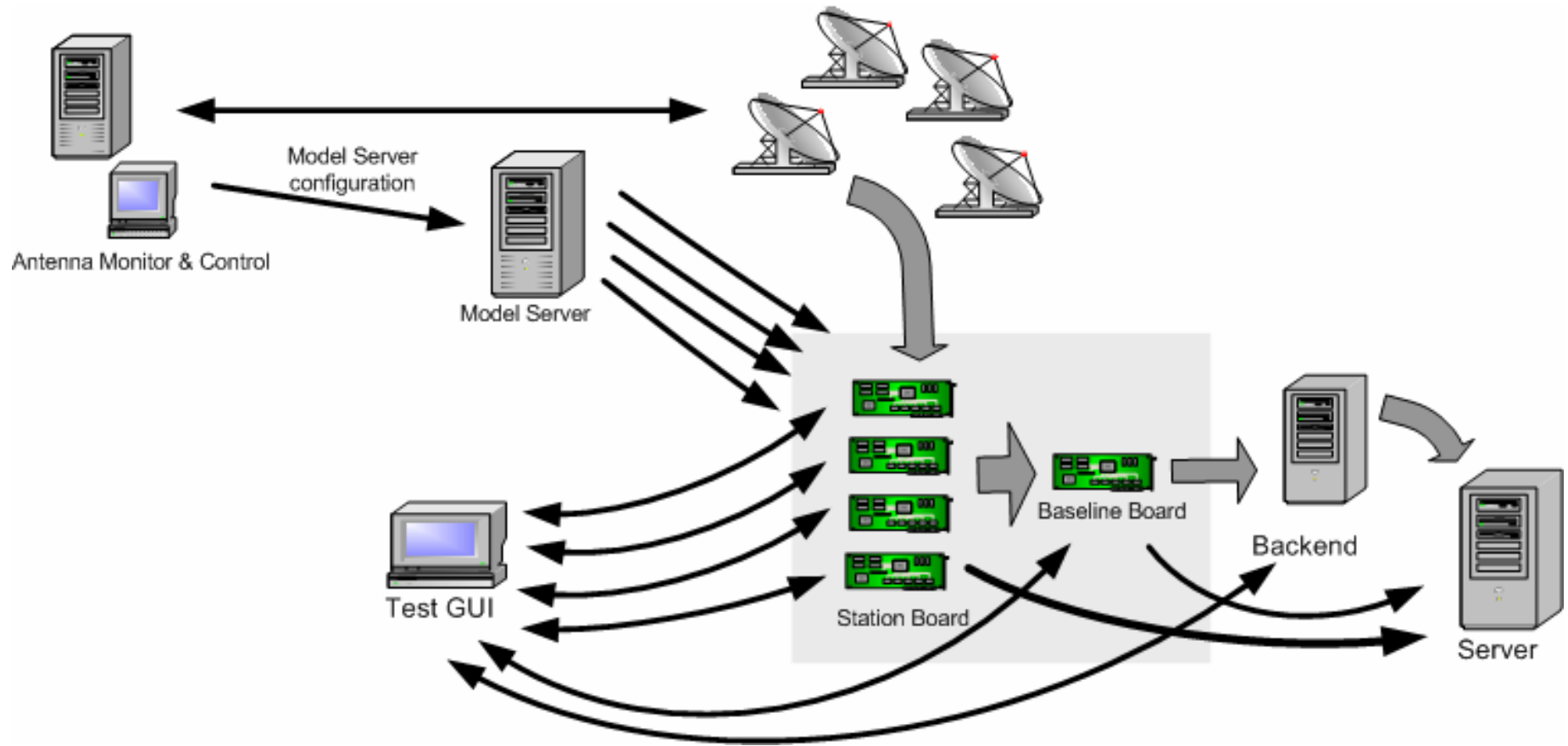
Correlator Testing

- Production correlator chip tests
 - Functional acceptance test by supplier using DRAO-supplied equipment.
 - At speed, but not over temperature range.
 - DRAO lab tests: special jig to be fabricated.
 - HALT/HASS tests being investigated (advanced version of “burn-in”).
- Unit PCB hardware tests during production:
 - Fast functional tests performed at factory in DRAO-supplied equipment.
- Unit hardware tests after acceptance
 - HALT/HASS tests of circuit boards (or equivalent).
 - Extended functional tests.

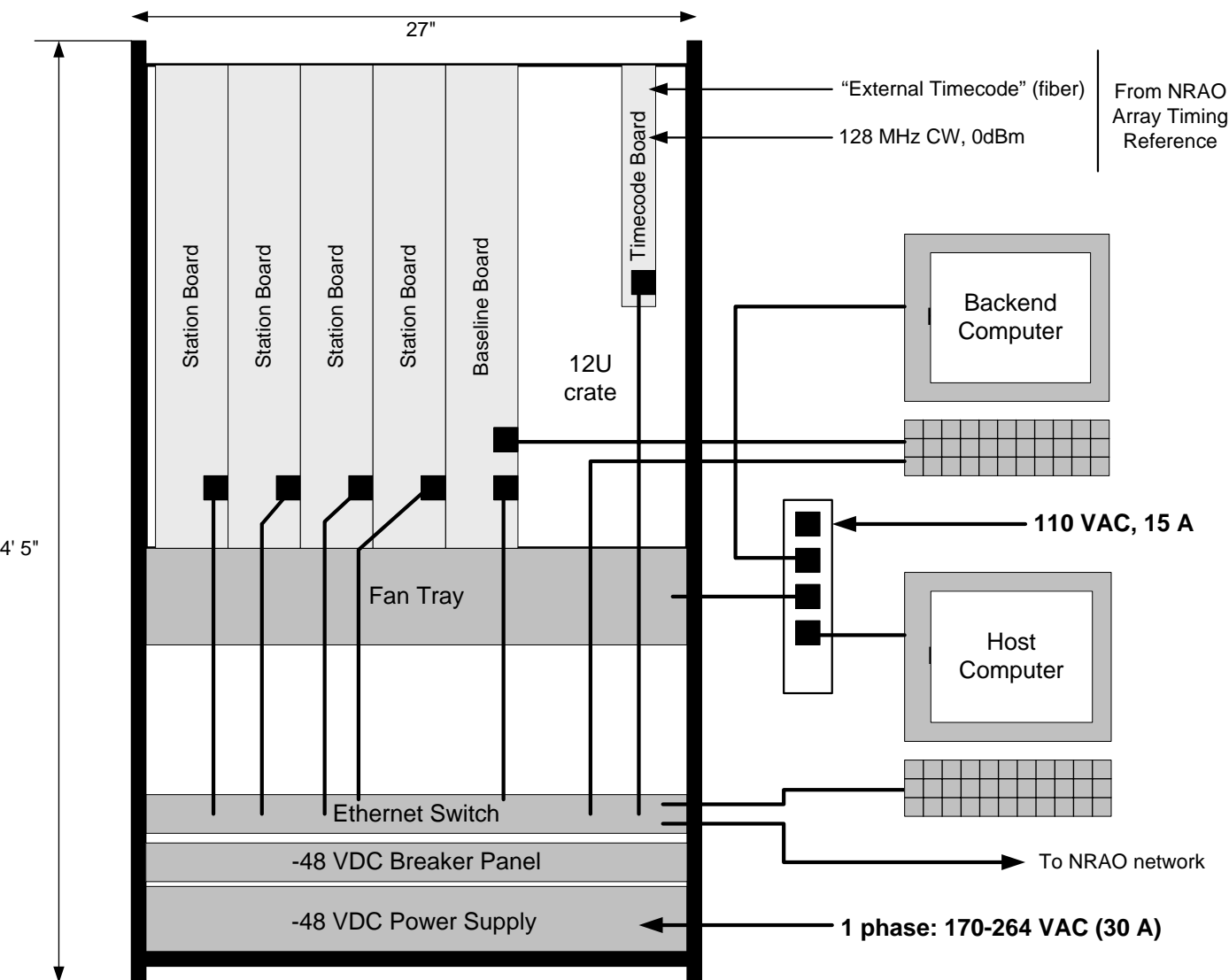
Correlator Testing (cont'd)

- System Tests
 - Prototype Stage
 - Extended testing/debug cycle in lab – all functions.
 - Many self-tests, simulated observations.
 - Should confer a high degree of reliability for On-the-Sky tests.
 - On-the-sky Tests
 - Final demonstration of prototype tests – designed to be quasi-independent of EVLA S/W.
 - Begin System Integration with EVLA software (continuing process).
 - Hardware left at VLA site.
 - Software Tests after On-the-Sky correlator delivered.
 - Continued testing with hardware that will remain at the VLA.
 - Understand interference (RFI) and the “clues” that the WIDAR system provides.

Test Configuration – Software View



On-the-Sky Test Setup



Installation Procedure

(Note: Dates from Apr/06 Long Term Schedule)

- 06-07: Install –48V DC power system.
- 06-07: Install underfloor cables.
- 08: Manufacture racks in Penticton.
- 08: Install overhead power distribution.
- 08: Install control computers, Ethernet switches, backend computers and other COTS equipment.
- 08-09: Install boards into racks in an order that maximizes scientific benefit.

Preliminary Installation Estimates

(Note: Dates from Apr/06 Long Term Schedule)

- Q4-06/Q1-07 – power supply (-48 V DC) .
 - Procurement, installation, training.
 - 40 person-days of NRAO effort.
- Q3/Q4-07 – signal cabling.
 - Installation of inter-rack high-speed cabling.
 - 512 pre-fab cables, 3 different lengths; 24 pre-fab power monitor & control cables.
 - 52 person-days of NRAO effort.
- Q4-07/Q1-08 – Racks
 - 24 racks, pre-fabricated, tested in Penticton.
 - 24 person days of NRAO effort.
- Q1-08 – power cabling.
 - Two cable runs: To distribution panel; distribution panel-to-racks.
 - 20 person-days of NRAO effort.

Preliminary Installation Estimates (cont'd)

- Q2-08 – control computers, M&C Ethernet
 - MCCC, CPCC, Ethernet switches, etc.
 - 120 VAC power required.
 - 8 person-days of NRAO effort.
- Q3-08 – Back-end computers and equipment.
 - Gbit Ethernet system.
 - 20 person-days of NRAO effort.
- Q3-08/Q3-09 – Board installation and test.
 - Occasional NRAO effort.
- Total Est. NRAO installation effort:
 - ≥ 8.2 Person-Months.

EVLA Correlator Group

DRAO-based.

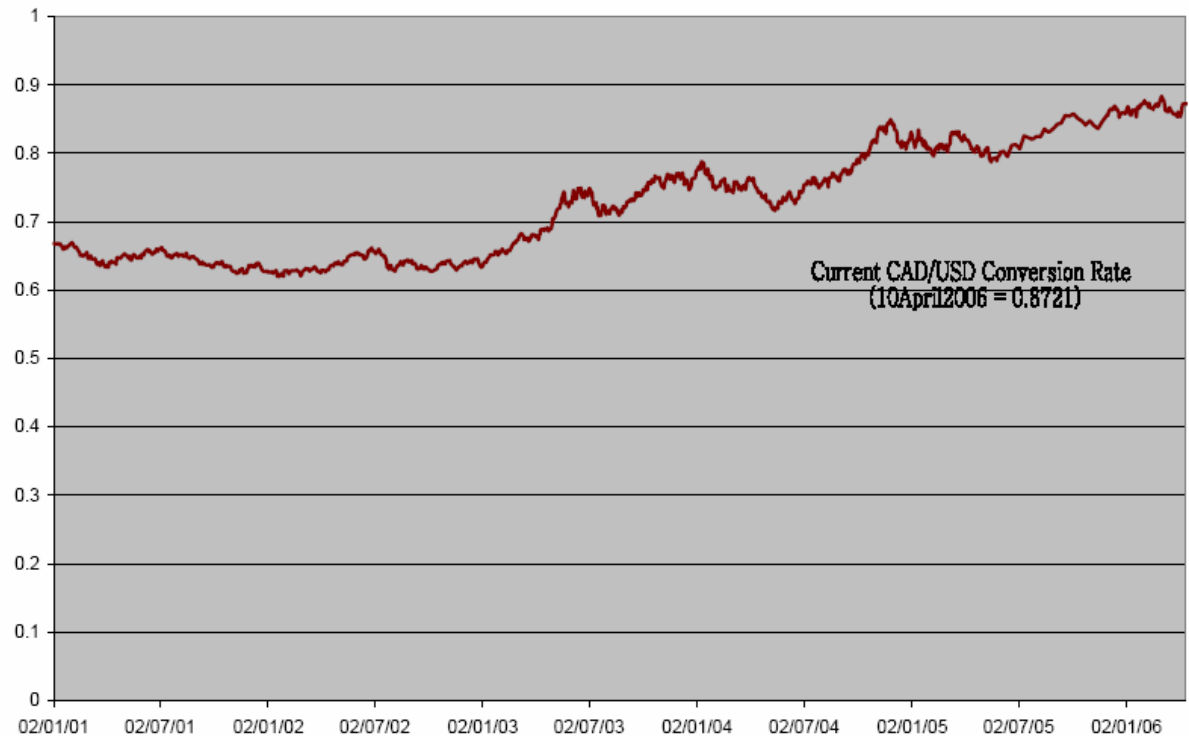


NRAO-based.

Funding in Canada – No Change

Aug/03 – Canadian Treasury Board approval of submitted budget (\$C 20M over 5 years).

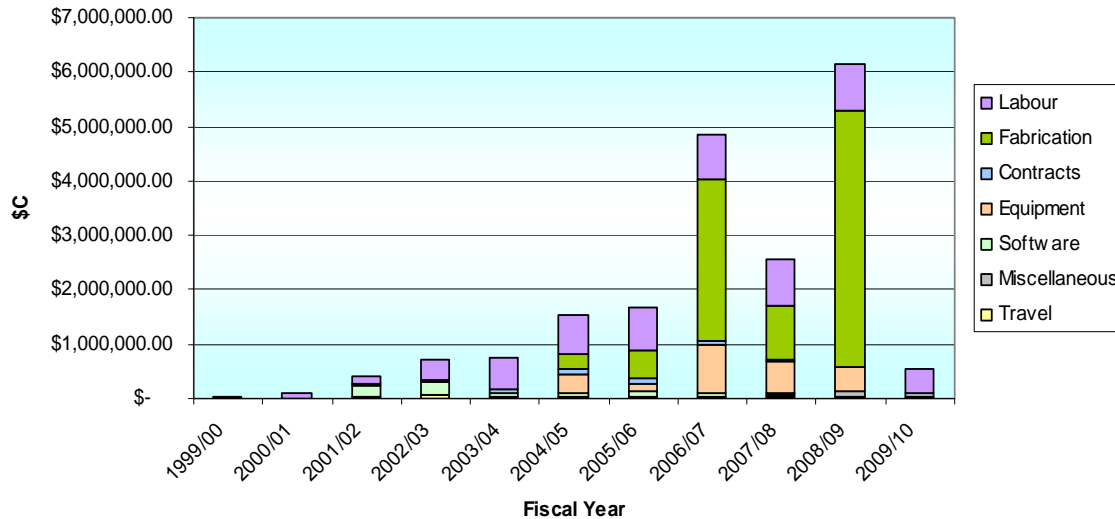
CAD/USD Conversion Rates (02Jan2001 to 10April2006)



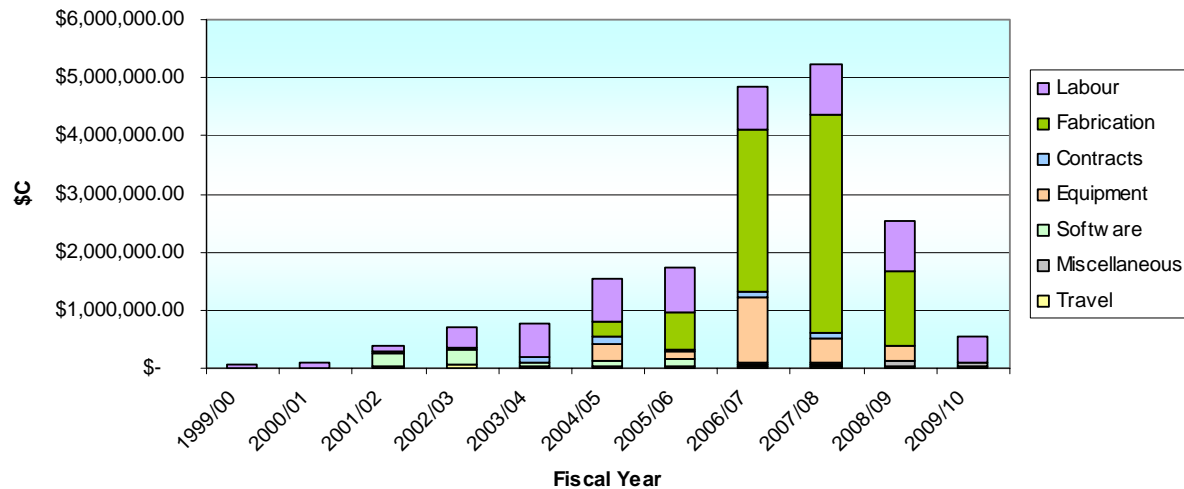
- Most spending in \$US.
- But see risk factors.

Correlator Projected Spending Profile

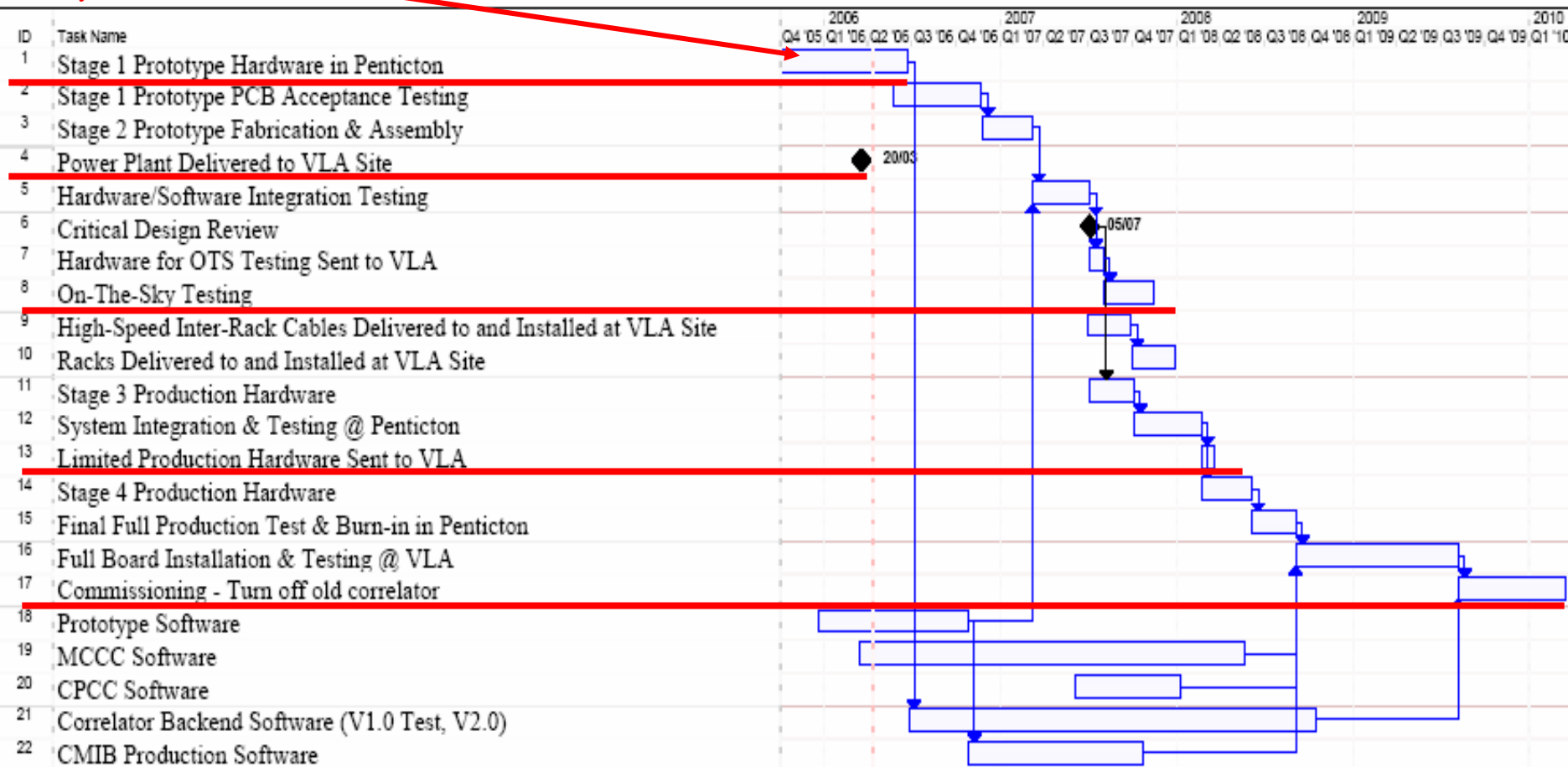
EVLA Spending Profile



EVLA Spending Profile



Very Uncertain Time Scale



** This schedule assumes no re-spins will be necessary.

** This schedule is the current quasi-optimistic view of the project.

** Long Term Schedule Modifications (from the previous edition - 09Mar2006):

----- Task 1: Stage 1 Prototype Hardware in Pentiction end date has been pushed out by four weeks to 23June2006 due to delay in release of Station Board Work Order.

----- Task 2: Stage 1 Prototype PCB Acceptance Testing now pushed out by two weeks due to delay in release of Baseline Board Work Order.

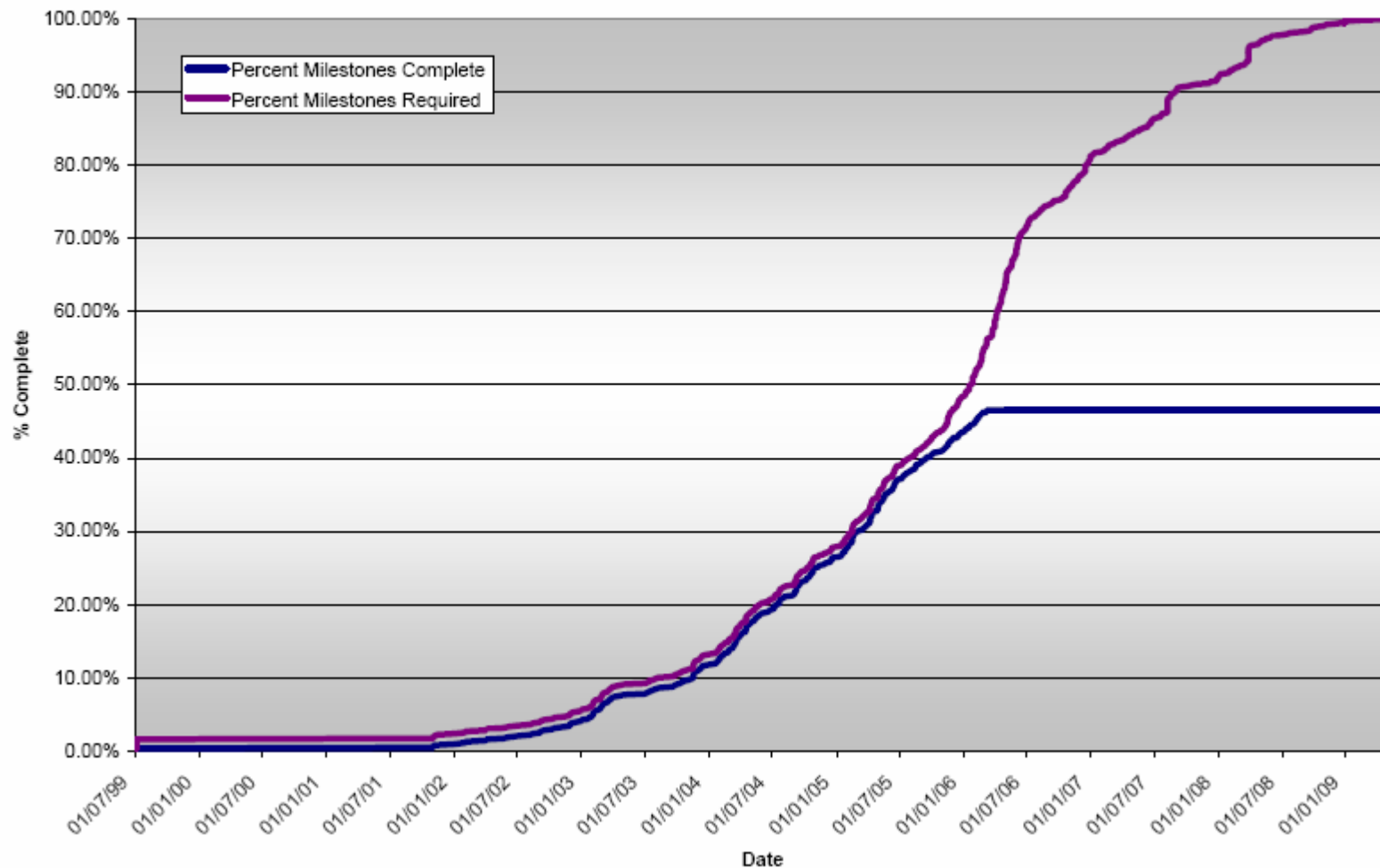
----- Task 4: Power Plant Delivered to VLA Site has been added to schedule.

----- Task 9: High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site has been added to schedule.

----- Task 10: Racks Delivered to and Installed at VLA Site has been added to schedule.

Milestone Progress

Percent Milestones Complete (10Mar2006)



Project Management

- Schedule
 - Detailed schedule periodically updated.
 - Near-term (target) schedule updated weekly.
 - Long-term schedule discussed monthly, and cross-checked against detailed schedule.
- Budget
 - Projections updated with schedule.
- Bills of Materials (BOM's)
 - 1000's of components.
 - Maintenance required.

Correlator Documentation

- Master Document Tracking Spreadsheet Maintained at DRAO.
- 115 documents written so far, including “Memos”.
- Additional 23 documents with designations and titles are anticipated.

Principal Design Reviews

- Three Design Reviews:
 - Conceptual (CoDR – Nov, 2001)
 - Review architecture and overall design.
 - Preliminary (PDR – July, 2005)
 - Review detailed designs before prototypes.
 - Critical (CDR)
 - Review system before “limited production” stage.
 - Scheduled for Q2/Q3, 2007.

Non-Technical Program Risks

- Funding
 - Original allotment of funds was over five years.
 - NRC management was made aware in Aug/03 that this does not fit the project spending profile – they decided that internal cash management could deal with the problem.
 - Will have to apply for an extension, which in the present climate presents a risk.
 - Worst case is that project could hypothetically be halted in April 2008.
 - Active cash management at HIA, NRC level.
- Schedule slippage?
 - Due to a slow start (already happened at the beginning).
 - Concerns over procurement processes.
 - This risk is retired. Major procurement contracts are in place except for power supply.
 - Technical progress slower than the deliberately aggressive initial schedule.
 - “Re-spins” will present additional schedule risk.
- Inadequate contingency?
 - The contingency fractions are much smaller than most high-tech projects.
 - Cost risk will be reduced quickly once prototypes are tested.
 - Exchange-rate changes have been favourable to date.
- Inflation not being recognized in funding profile?
 - Inflation is a corrosive influence.

Technical Program Risks

- Technical risk is currently at a maximum
 - Much design effort and prototype expenditure has taken place.
 - Prototype hardware is being fabricated (or about to be fab'd), but not received/tested.
- But ...
 - Considerable design effort expended to reduce technical risk.
 - Finely divided testing schemes for circuit boards – every path can be checked independently.
 - Correlator chip underwent an independent test and verification process, including a major simulation campaign after the “place-and-route” stage.
 - A separate Design for Manufacturability (DFM) analysis done for circuit boards – results in a major reduction in risk.
- Formal system reliability analysis has been done, and will be updated.
- Funds and design effort has been expended to minimize technical risk.
 - We are optimistic and confident that technical risk is reasonably low.

Descoping

- The correlator is difficult to split, once designed, and saving is inefficient.
- Have not reconsidered descoping options since the budget is currently “under control”.
- If the previously-mentioned non-technical risks become imminent concerns, then descoping options will have to be revisited.

Project Summary

- Are we meeting the required schedule?
 - We are sticking with the original delivery date, although there is now some squeezing of activities towards the end.
- Are we over budget at this stage?
 - Budget is slimly allocated, but we are not over budget.
- Are we planning to deliver on what we said we would do?
 - Yes, with minor improvements.
- What are the major risks at this stage?
 - Hypothetical funding difficulty in 2008.
 - Technical risks should be reduced this year as prototypes are tested.

End