The EVLA Correlator

P. Dewdney

Herzberg Institute of Astrophysics

National Research Council Canada

NRC · CNRC

Outline

1. Correlator Performance Goals
2. Hardware Progress
3. Software Progress
4. System Progress
5. Prototype Testing
6. Installation Estimates
7. Funding, Budget & Schedule
8. Risk Issues

Key EVLA Processing Capabilities

Deep Imaging Polarization

- ✓ 8 GHz Bandwidth (dual polarization).
- ✓ Full polarization processing.
- ✓ Wide-field imaging.

Narrow spectral lines Wideband searches

- ✓ 16,000 channels at max. bandwidth (BW).
- ✓ $>10^6$ channels at narrow BWs.
- ✓ Spectral resolution to match any linewidth.
- ✓ Spectral polarization (Zeeman Splitting).

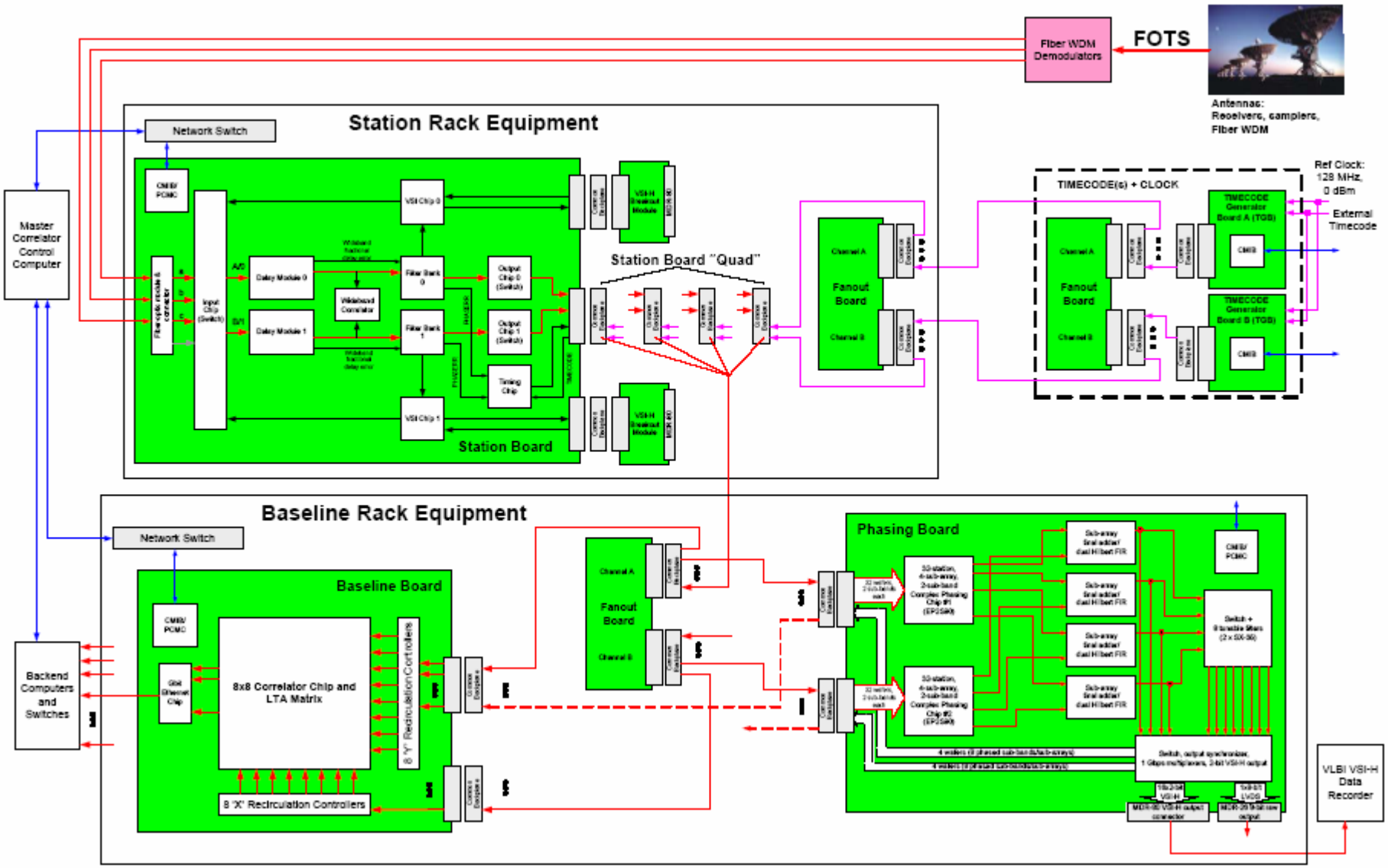
Flexibility Many resources

- ✓ 8 tunable 2 GHz wide bands.
- ✓ Each band - 16 tunable sub-bands.
- ✓ Sub-band – independent spectral resolution.
- ✓ Simultaneous line and continuum.

High time resolution

- ✓ 1000 pulsar “phase bins”.
- ✓ “Single-dish” data output to user instruments.
- ✓ Very fast time sampling (<20 μs).

EVLA Correlator System Diagram



Significant Events Since Dec. 2004

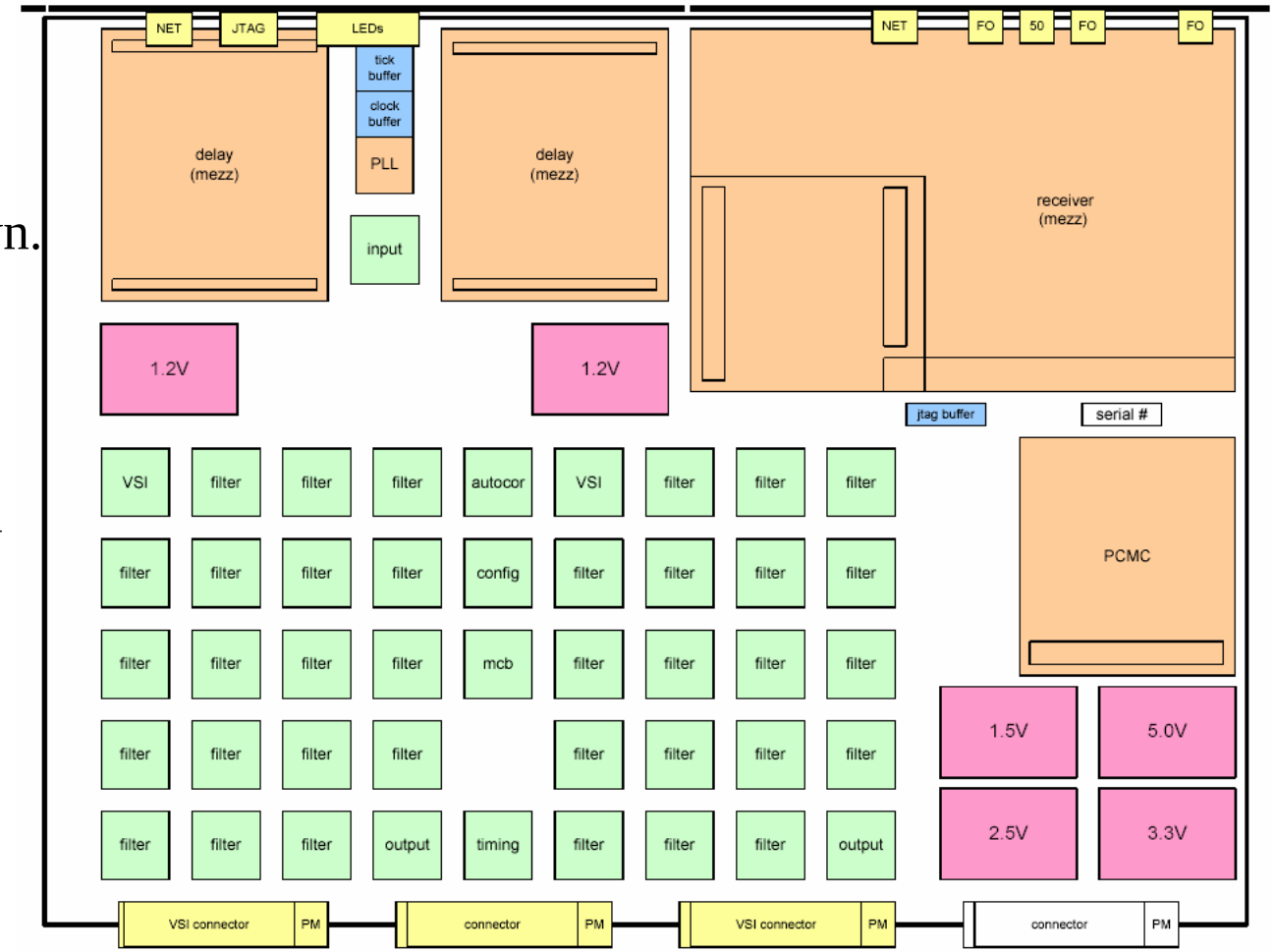
- Correlator Chip CDR – Jan/05
- Software Review – Jan/05.
- Correlator Preliminary Design Review – July/05.
- PCB fabricator contract signed – Jan/06.
- Prototype Correlator chip wafers fab’d – Feb/06.
- Software Review – Mar/06.
- Prototype chip delivery – early Jun/06.
- Baseline Board prototype delivery – Jun/06.
- Station Board prototype delivery – est. Aug/06.

Hardware Progress

- FPGA's
  - All FPGA's are designed, including the Filter Chip.
- Station board
  - Layout is close to completion, including Design-for-Manufacture approval.
  - Presently undergoing signal integrity simulation.
  - Prototype fabrication order expected in June.
- Baseline Board
  - Prototype fabrication under way.
- Phasing board
  - Draft specification (RFS) released.
  - Deferred in time but not reduced in priority.
- Other boards
  - Prototypes for all other boards already fabricated.
  - Fan-out board needs redesign for better signal margins.
- System
  - Racks designed and prototyped; thermal analysis done.
  - Power system RFP draft written.
  - Reliability analysis system in place – first draft of analysis complete.

Station Board Layout

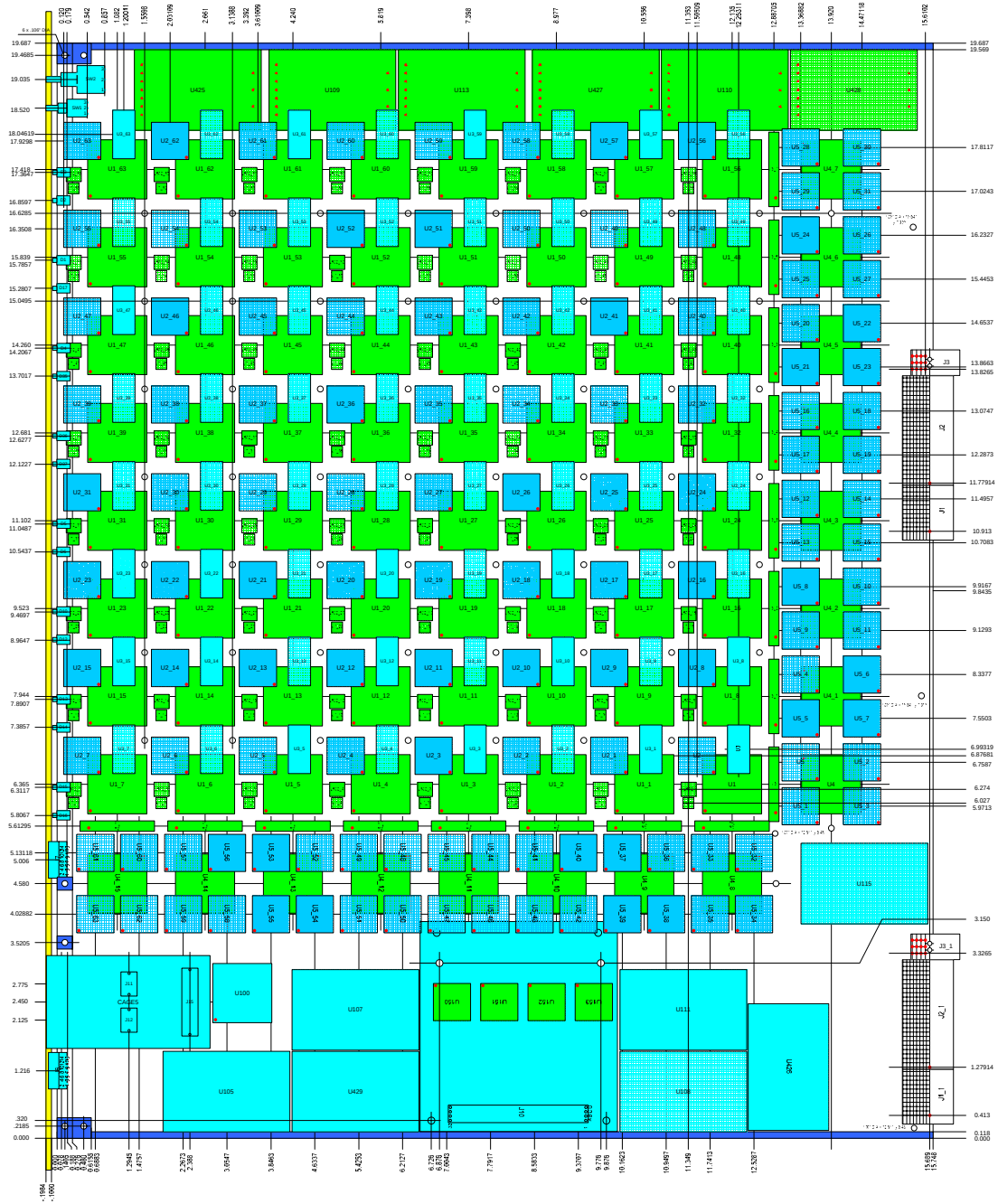
- "Daughter" Board - brown.
- Power Supplies – pink.
- FPGA's – Green
- Connectors – light brown and white.
- ~5000 parts.
- 140 required for EVLA.



Size: ~510 x ~410 mm

Baseline Board Layout

- Green chips – front side.
- Blue chips – back side.
- 8 x 8 array of correlator chips.
- LTA chips on the back side.
- Recirculation Controller.
- ~12000 parts
- ~177 required for EVLA.



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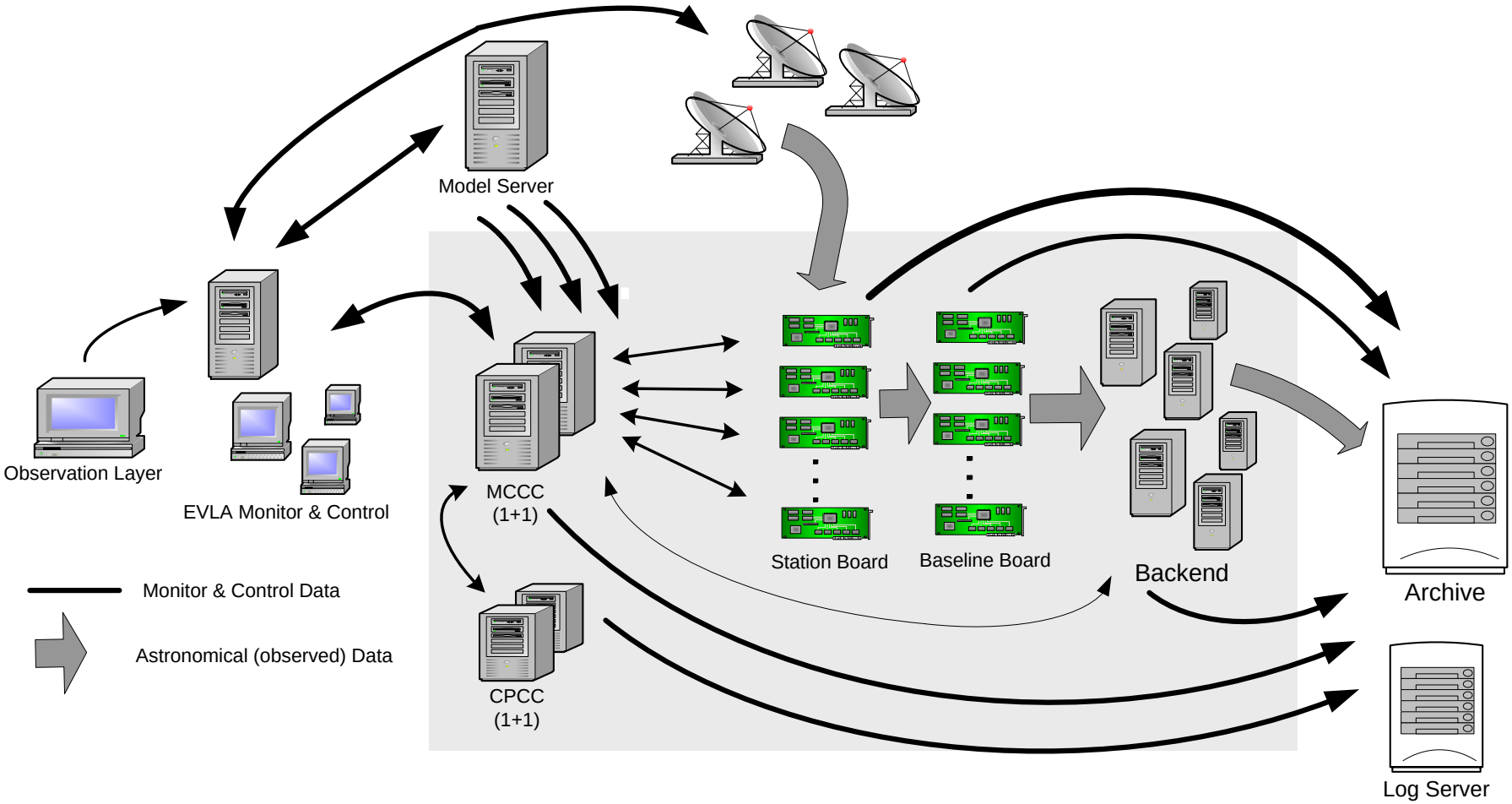
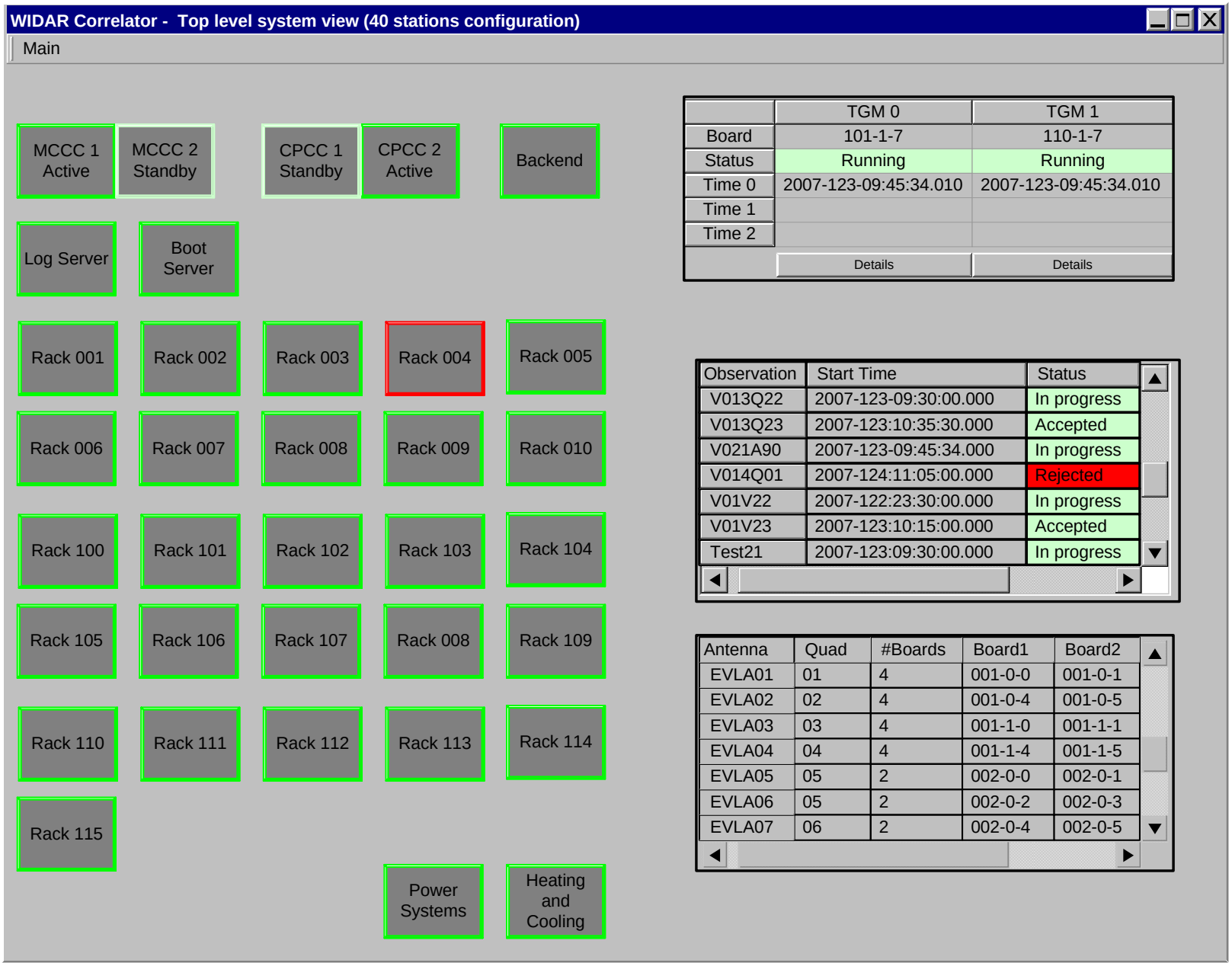
Software Progress

- GUI-based prototype testing software
  - Complete enough to be useful already.
  - All FPGA's covered except Phasing Board.
  - **Provides "engineer's view of correlator system.**
    - **Permanent maintenance value.**
  - Top-level GUI's now under development.
- Virtual Correlator Interface
  - Well defined except for correlator output area.
  - Communications protocol well defined except for transport layer.
- Master Correlator Control Computer (MCCC)
  - Work deferred for GUI development.
  - Architecture/scope well defined.
- Real-time control software
  - "CMIB" processor on each board.
  - Operating system has been working for a long time.
  - XML-based communication with "outside world".
  - Drivers for FPGA's are well under way.

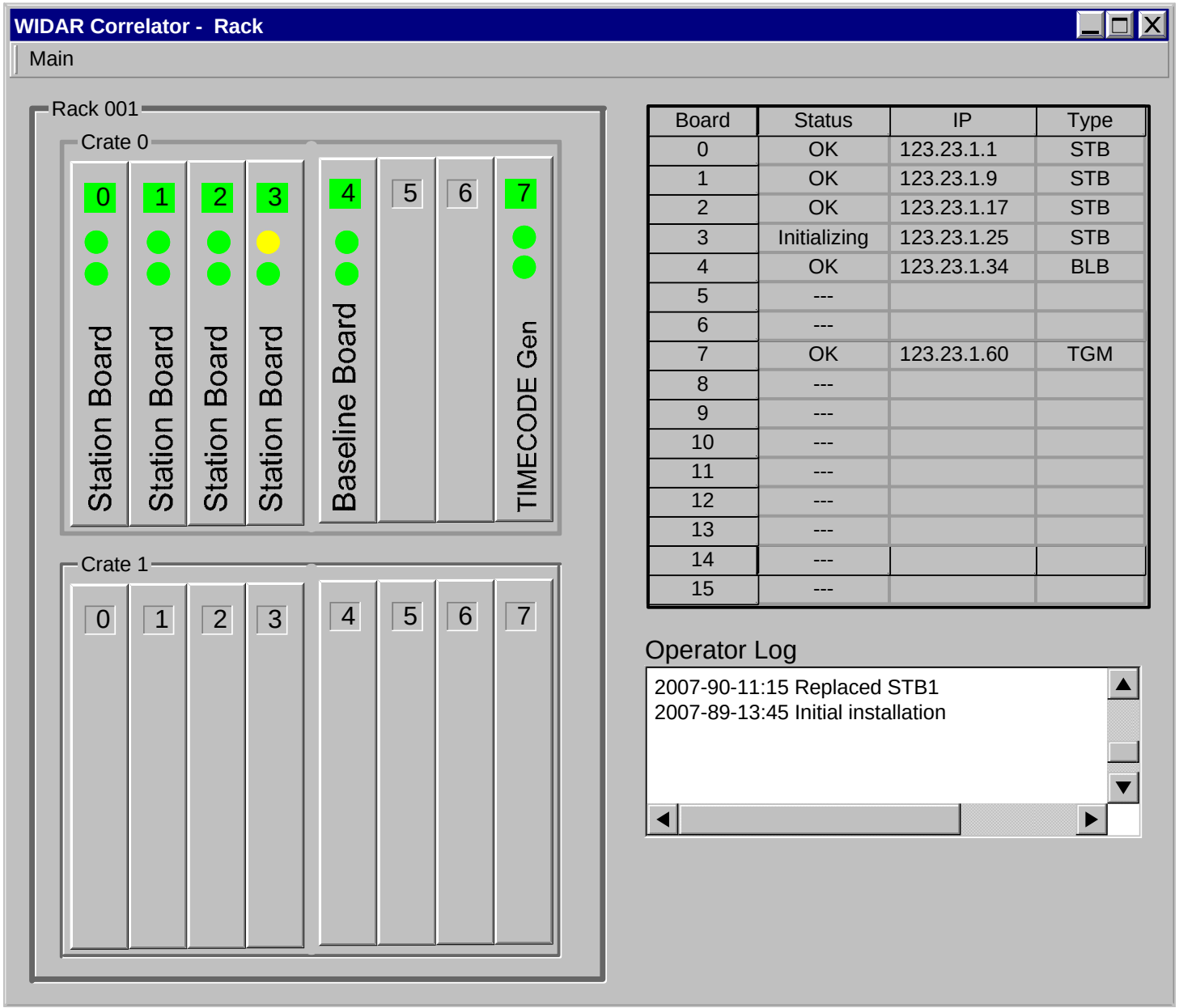
Correlator Software System Context



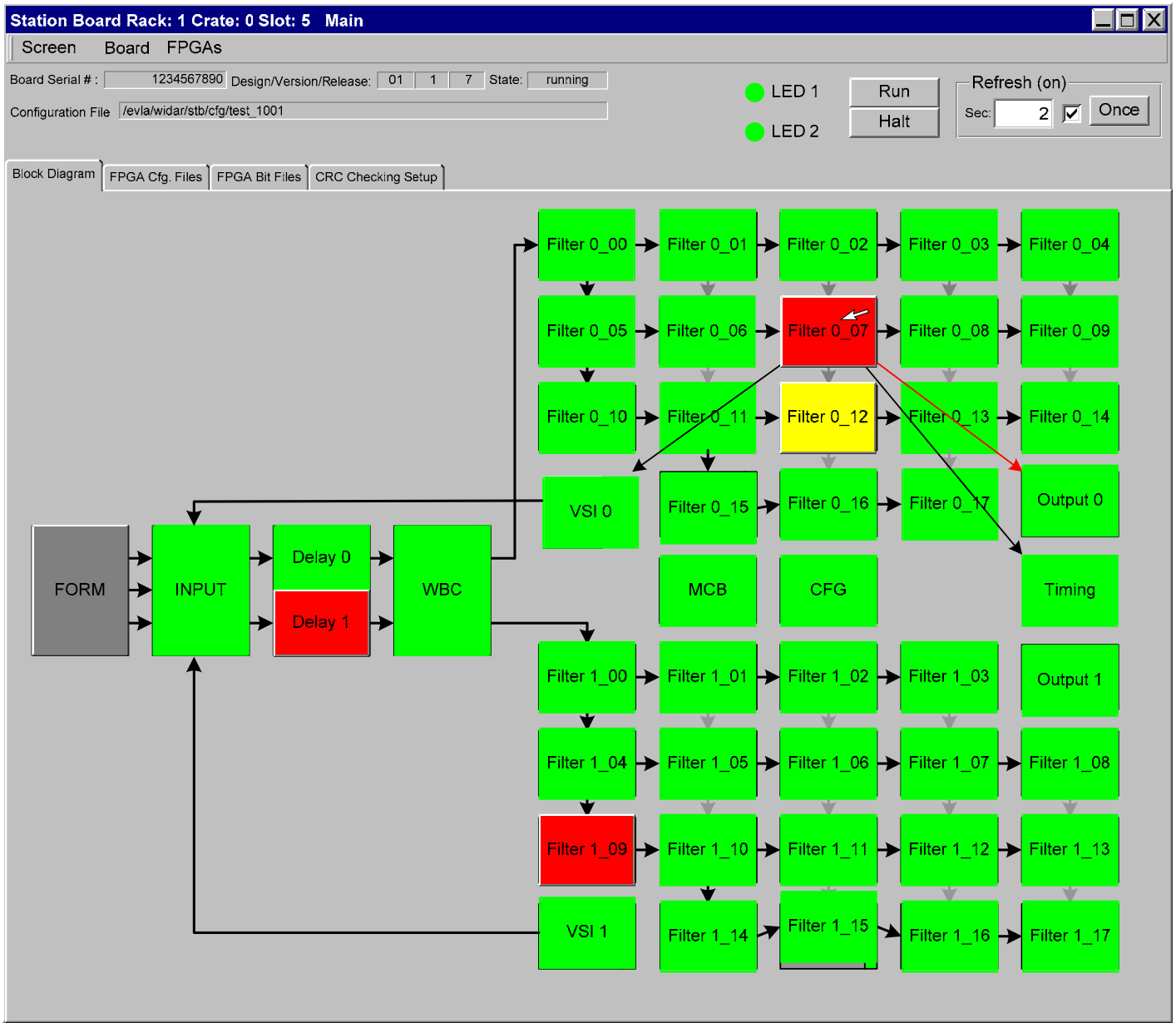
Correlator System GUI



Individual Rack



Station Board Top Level



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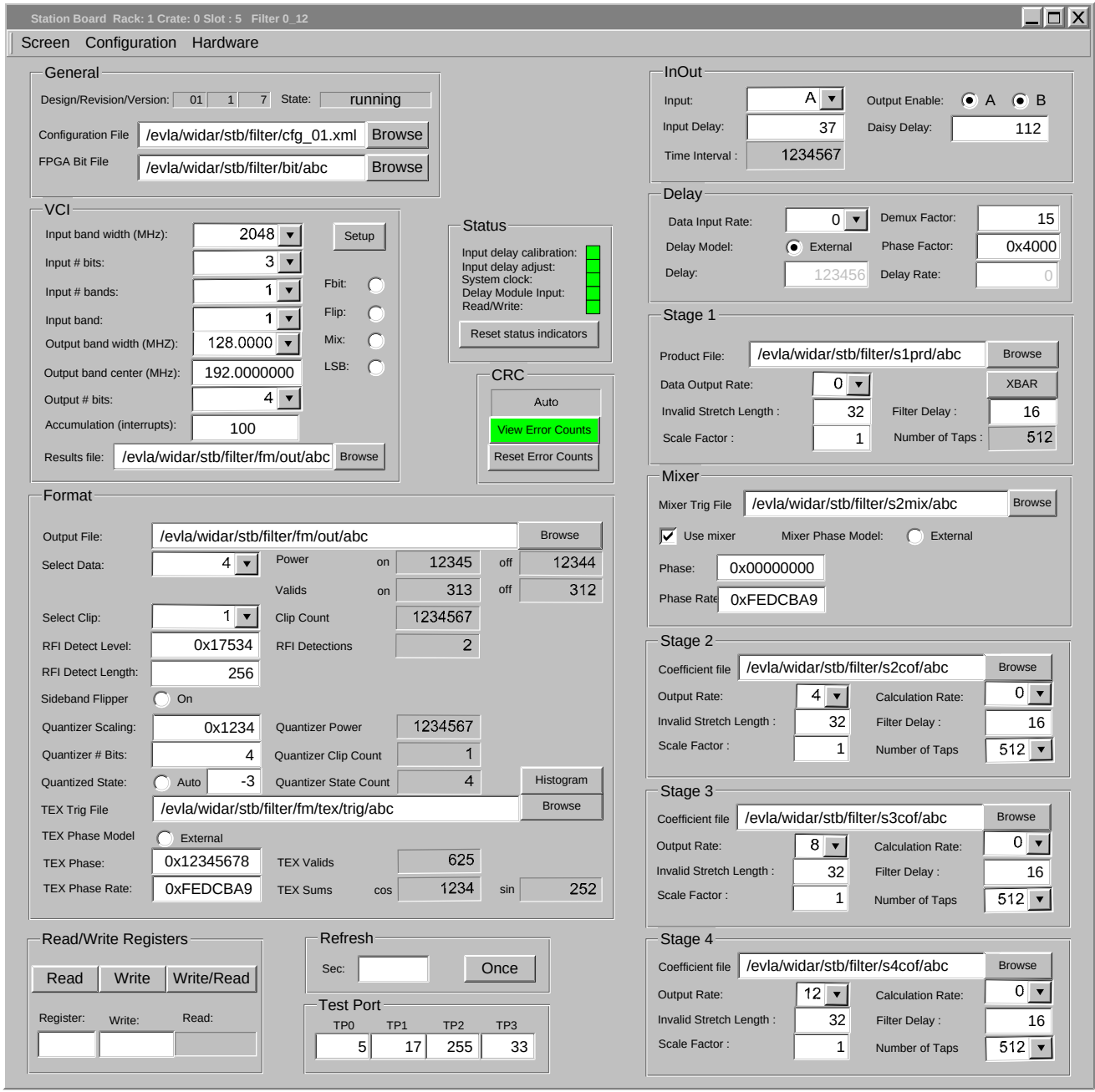
Filter Control GUI



Correlator Software People

- Sonja Vrcic (Penticton)
  - Coordinates overall design and specification.
  - Virtual Correlator Interface (VCI) definition.
  - Master Correlator Control Computer (MCCC) S/W.
- Bruce Rowen (Socorro)
  - Correlator hardware control S/W (CMIB).
- Kevin Ryan (Socorro)
  - GUI development and hardware control S/W.
- Martin Pokorny (Socorro)
  - Correlator Backend software.
- Michael Rupen, John Romney, Bryan Butler, Ken Sowinski, Barry Clark, Bill Sahr (Socorro)
  - Advisory capacity.

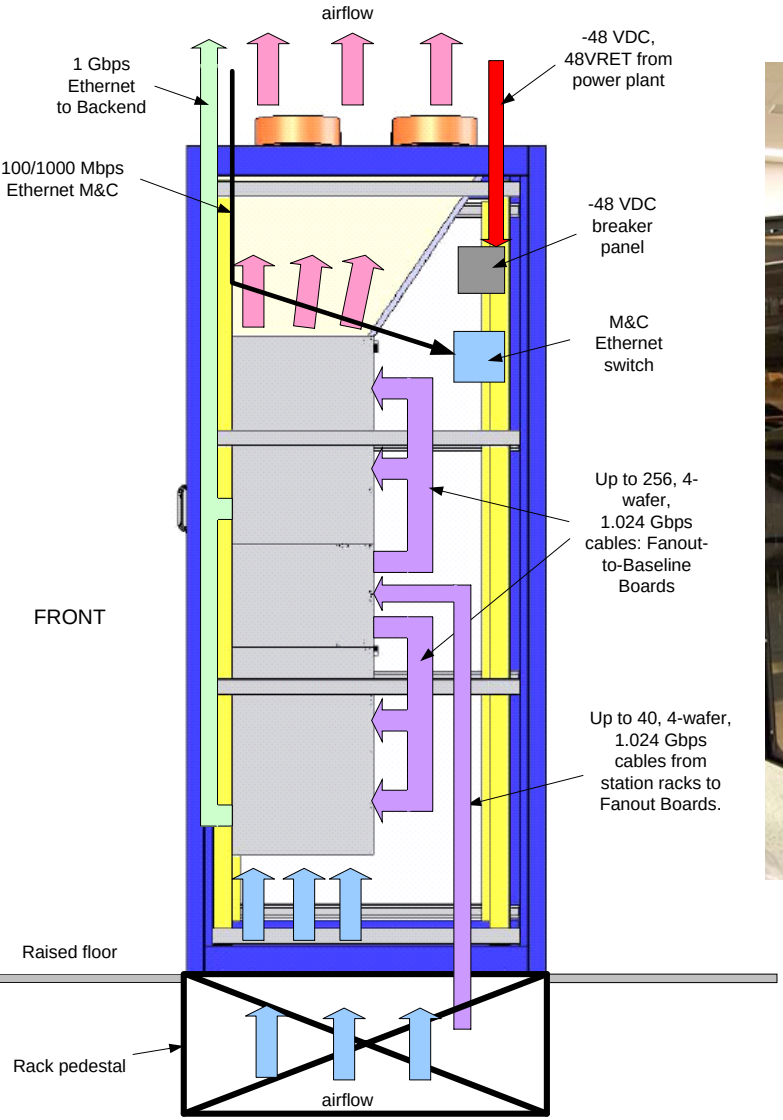
Correlator-related Software Issues

- Correlator output: ALMA Science Data Model (ASDM) must be qualified for EVLA use.
  - On the surface ASDM looks all right in the sense that additions can be made to meet EVLA requirements.
  - Is ALMA effort required and is it available?
  - This issue is to be addressed later in the series of presentations.
- Preliminary plans to add “blocks” in the Correlator Back End (CBE).
  - Additional Ethernet Switch and output Fast Data Formatter computer(s).
  - Formatting to ASDM spec’s will probably take place in the Fast Data Formatter.
  - Details to be worked out.
- Virtual Correlator Interface (VCI) Transport protocol is to be defined.
- Potential unknown throughput issues could arise.

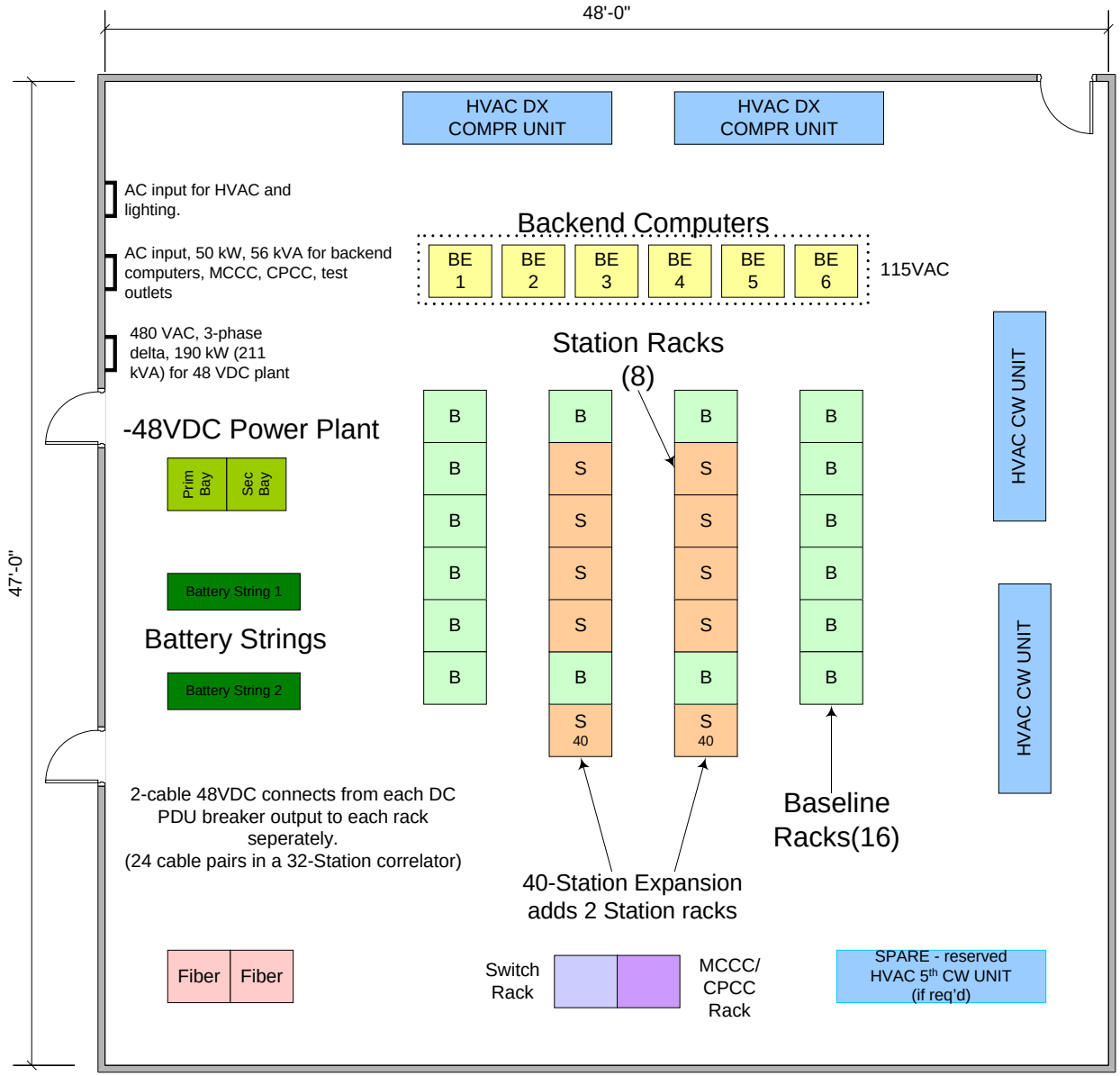
System Progress

- NRAO work on correlator room is progressing rapidly.
- Design of overall room layout is complete.
- Environmental specifications have been developed.
  - Air flow & temperature: ~1700 cfm per rack, 15 ºC.
  - ElectroStatic Discharge (ESD)
    - 90 nm devices used extensively (<1/1000 thickness of human hair)
    - Humidity specs.
    - Strict handling and servicing procedures.
  - Air quality
    - ISO 14644-1 class 8 + MERV 13 filter.
- Racks
  - "Thermal prototypes" have been built and tested.
  - "Mechanical prototypes" ditto.
  - Preliminary fabrication plan is being developed.
- Preliminary installation plan is being developed.
- Power plant specifications/RFP draft written for acquisition this fiscal year (ends Mar 31/07).

Correlator Rack Layout



Correlator Room Layout



ElectroStatic Discharge (ESD)

RESTRICTED ACCESS

ESD Protected Area
wear ESD coats and shoes

Overriding door interlock will sound ALARM

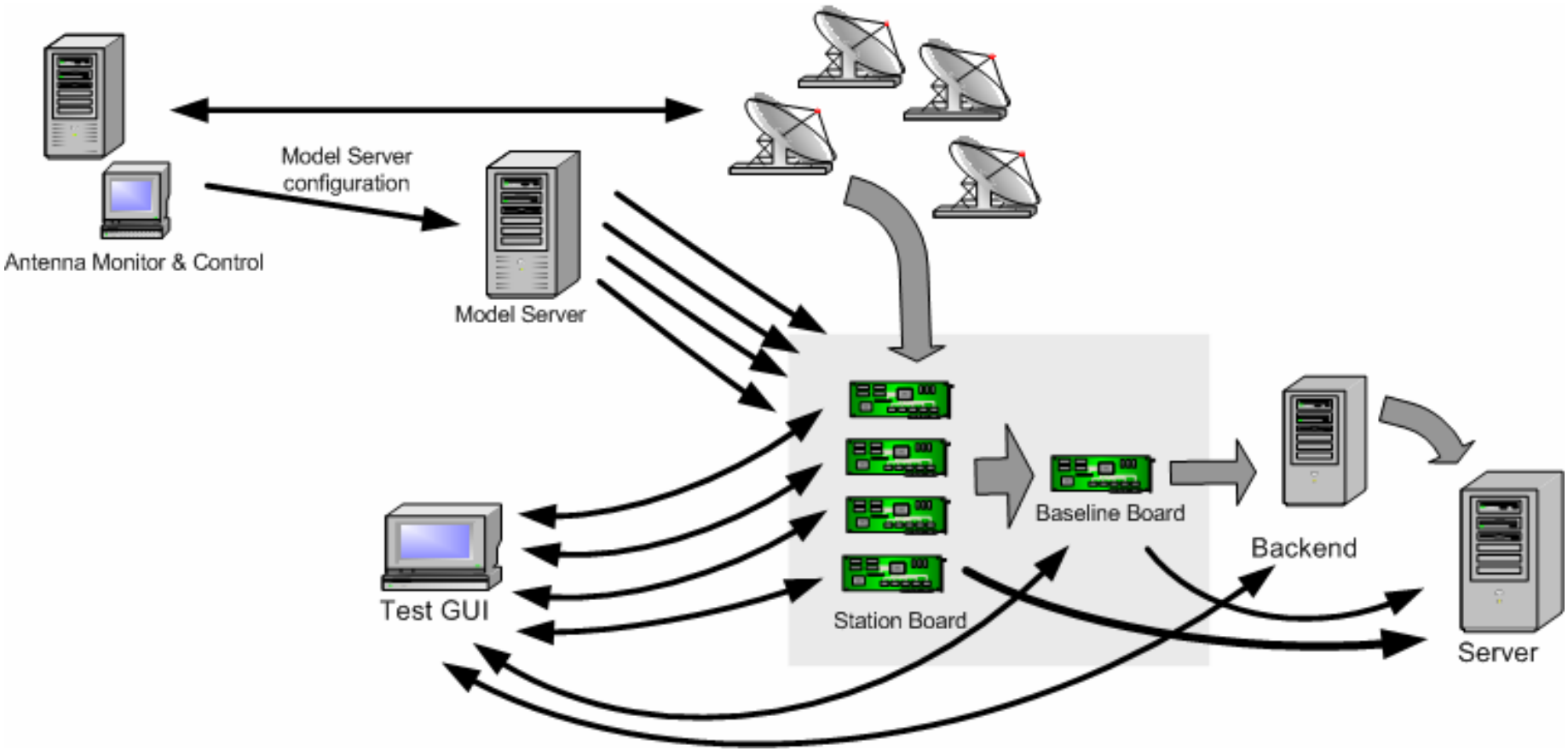
Correlator Testing

- Production correlator chip tests
  - Functional acceptance test by supplier using DRAO-supplied equipment.
    - At speed, but not over temperature range.
  - DRAO lab tests: special jig to be fabricated.
    - HALT/HASS tests being investigated (advanced version of "burn-in").
- Unit PCB hardware tests during production:
  - Fast functional tests performed at factory in DRAO-supplied equipment.
- Unit hardware tests after acceptance
  - HALT/HASS tests of circuit boards (or equivalent).
  - Extended functional tests.

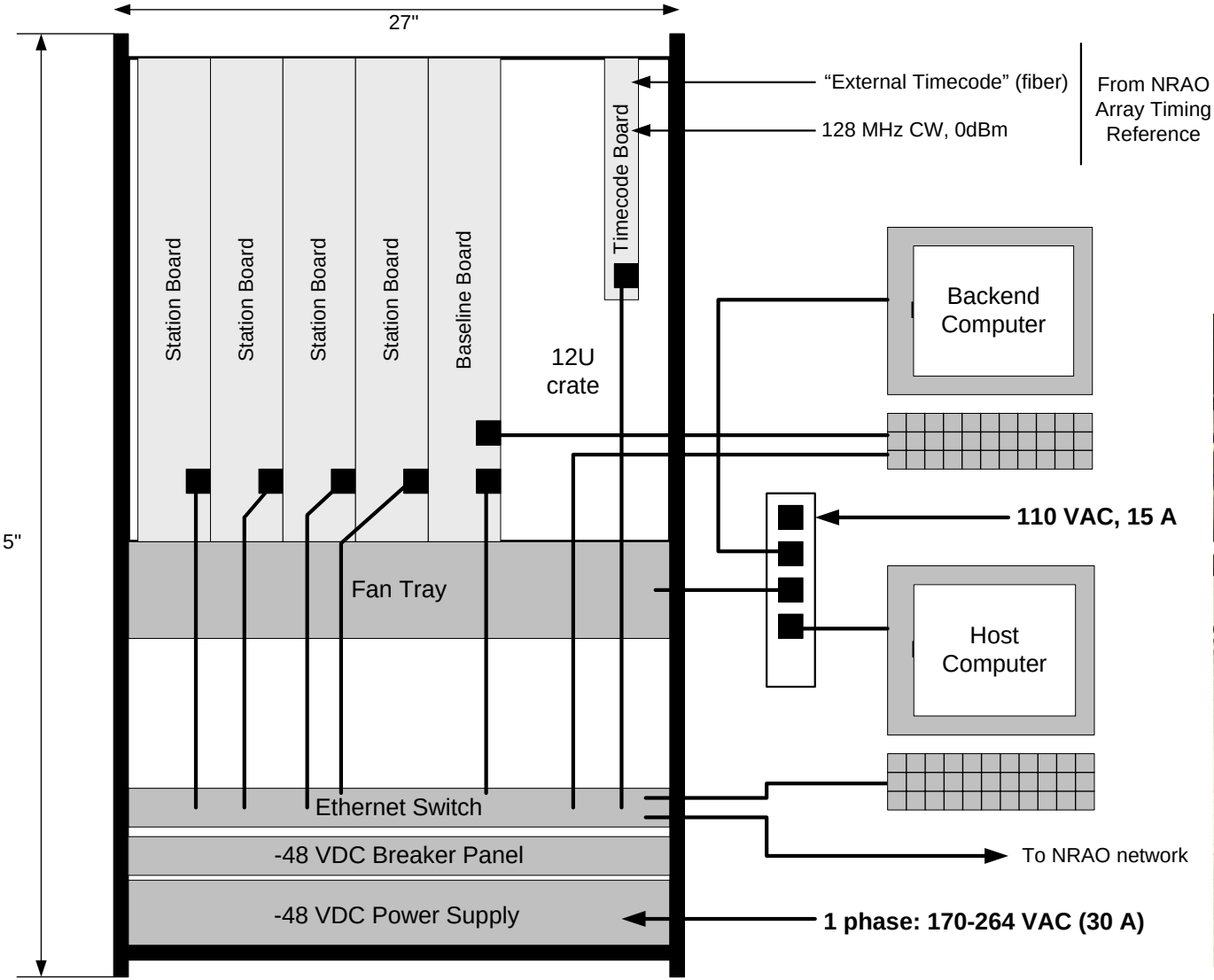
Correlator Testing (cont'd)

- System Tests
  - Prototype Stage
    - Extended testing/debug cycle in lab – all functions.
    - Many self-tests, simulated observations.
    - Should confer a high degree of reliability for On-the-Sky tests.
  - On-the-sky Tests
    - Final demonstration of prototype tests – designed to be quasi-independent of EVLA S/W.
    - Begin System Integration with EVLA software (continuing process).
    - Hardware left at VLA site.
  - Software Tests after On-the-Sky correlator delivered.
    - Continued testing with hardware that will remain at the VLA.
    - Understand interference (RFI) and the "clues" that the WIDAR system provides.

Test Configuration – Software View



On-the-Sky Test Setup



Installation Procedure

(Note: Dates from Apr/06 Long Term Schedule)

- 06-07: Install –48V DC power system.
- 06-07: Install underfloor cables.
- 08: Manufacture racks in Penticton.
- 08: Install overhead power distribution.
- 08: Install control computers, Ethernet switches, backend computers and other COTS equipment.
- 08-09: Install boards into racks in an order that maximizes scientific benefit.

Preliminary Installation Estimates

(Note: Dates from Apr/06 Long Term Schedule)

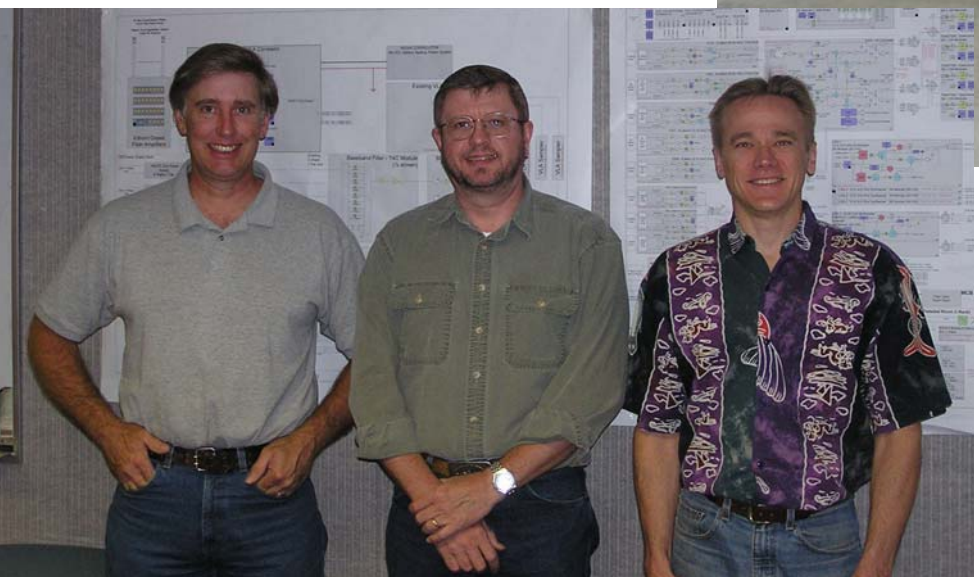
- Q4-06/Q1-07 – power supply (-48 V DC) .
  - Procurement, installation, training.
  - 40 person-days of NRAO effort.
- Q3/Q4-07 – signal cabling.
  - Installation of inter-rack high-speed cabling.
  - 512 pre-fab cables, 3 different lengths; 24 pre-fab power monitor & control cables.
  - 52 person-days of NRAO effort.
- Q4-07/Q1-08 – Racks
  - 24 racks, pre-fabricated, tested in Penticton.
  - 24 person days of NRAO effort.
- Q1-08 – power cabling.
  - Two cable runs: To distribution panel; distribution panel-to-racks.
  - 20 person-days of NRAO effort.

Preliminary Installation Estimates (cont'd)

- Q2-08 – control computers, M&C Ethernet
  - MCCC, CPCC, Ethernet switches, etc.
  - 120 VAC power required.
  - 8 person-days of NRAO effort.
- Q3-08 – Back-end computers and equipment.
  - Gbit Ethernet system.
  - 20 person-days of NRAO effort.
- Q3-08/Q3-09 – Board installation and test.
  - Occasional NRAO effort.
- Total Est. NRAO installation effort:
  - ≥ 8.2 Person-Months.

EVLA Correlator Group

DRAO-based.

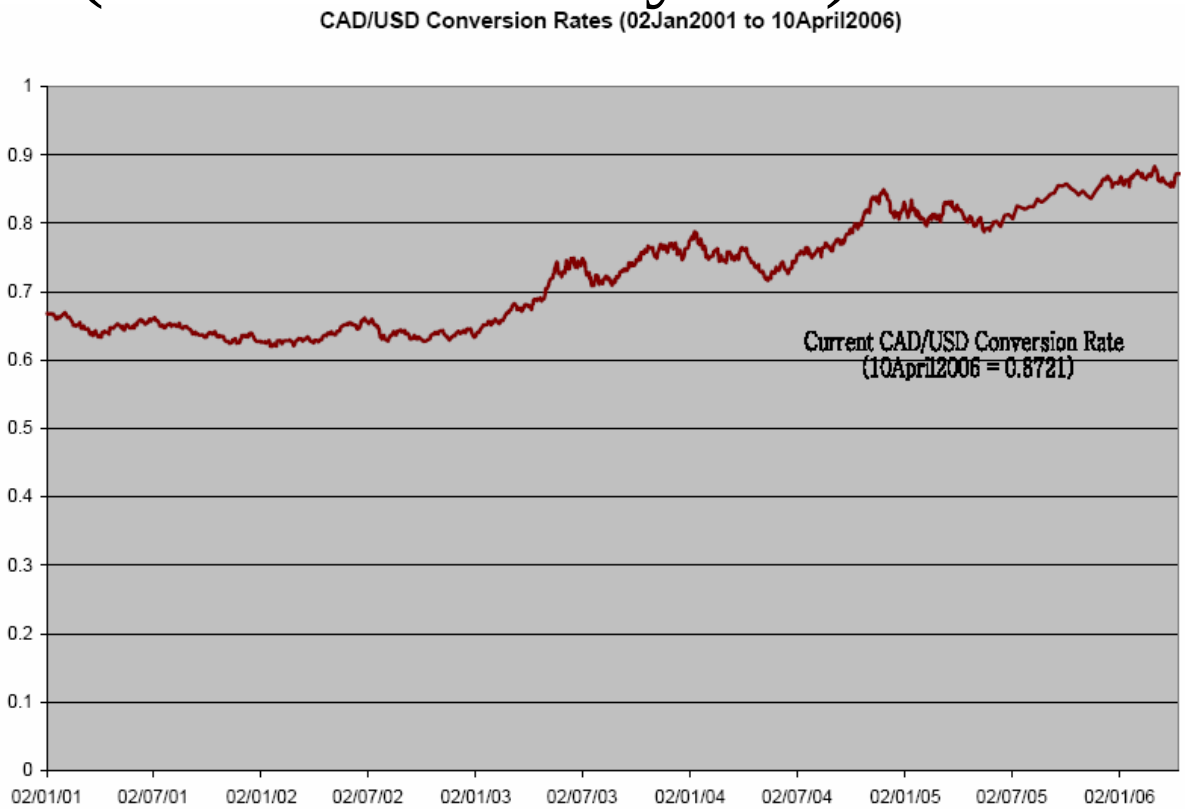


NRAO-based.

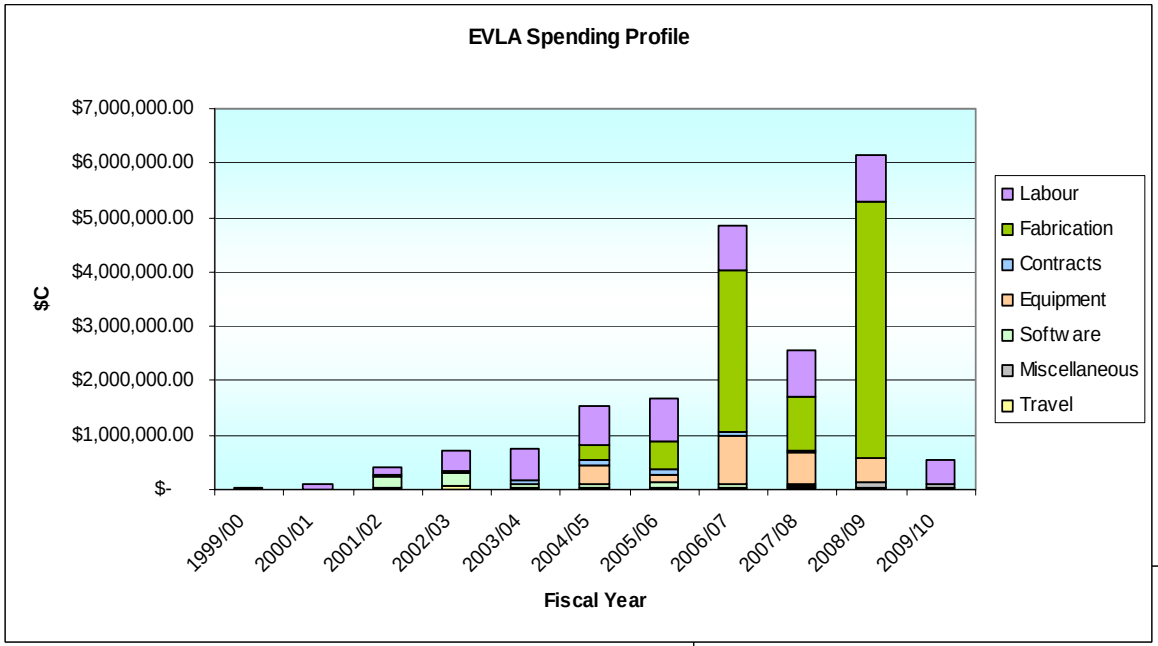
Funding in Canada – No Change

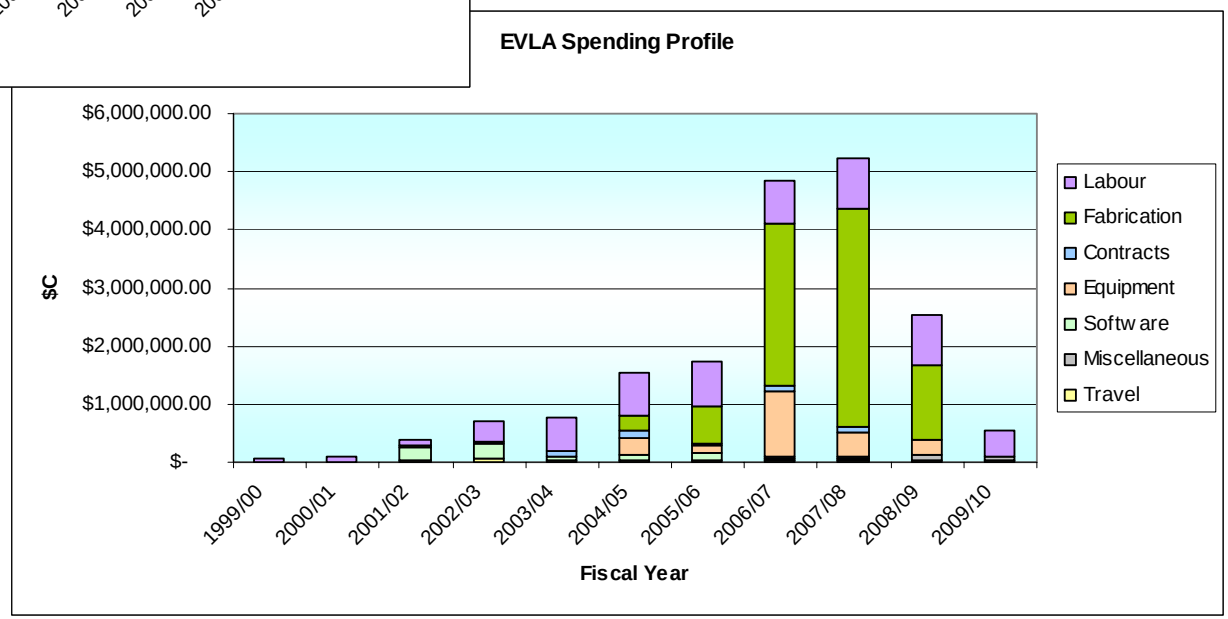
Aug/03 – Canadian Treasury Board approval of submitted budget ($C 20M over 5 years).

- Most spending in $US.
- But see risk factors.



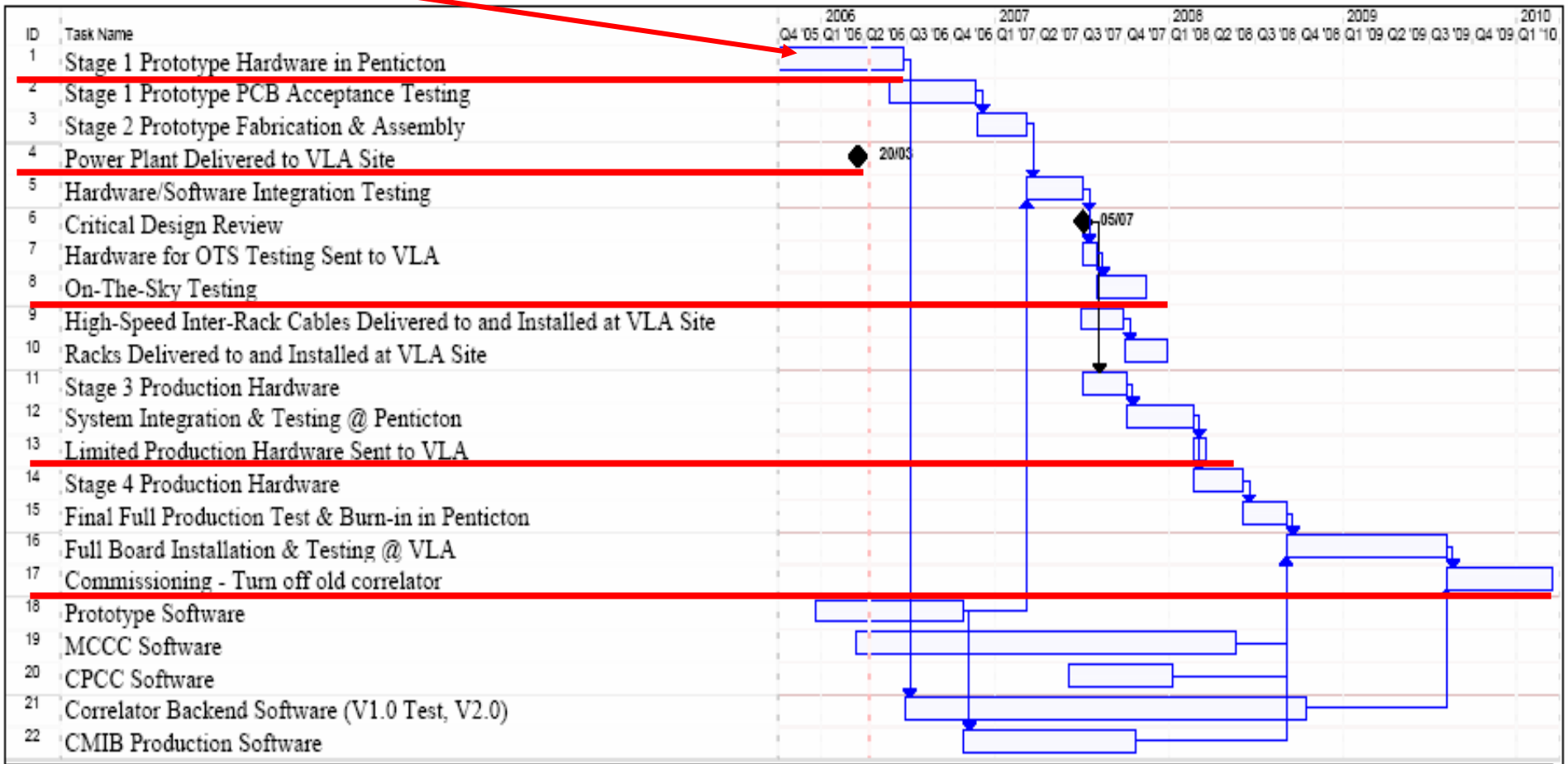
Correlator Projected Spending Profile





Correlator Summary Schedule

Very Uncertain Time Scale



*** This schedule assumes no re-spins will be necessary.*

*** This schedule is the current quasi-optimistic view of the project.*

*** Long Term Schedule Modifications (from the previous edition - 09Mar2006):*

------ *Task 1: Stage 1 Prototype Hardware in Penticton end date has been pushed out by four weeks to 23June2006 due to delay in release of Station Board Work Order.*

------ *Task 2: Stage 1 Prototype PCB Acceptance Testing now pushed out by two weeks due to delay in release of Baseline Board Work Order.*

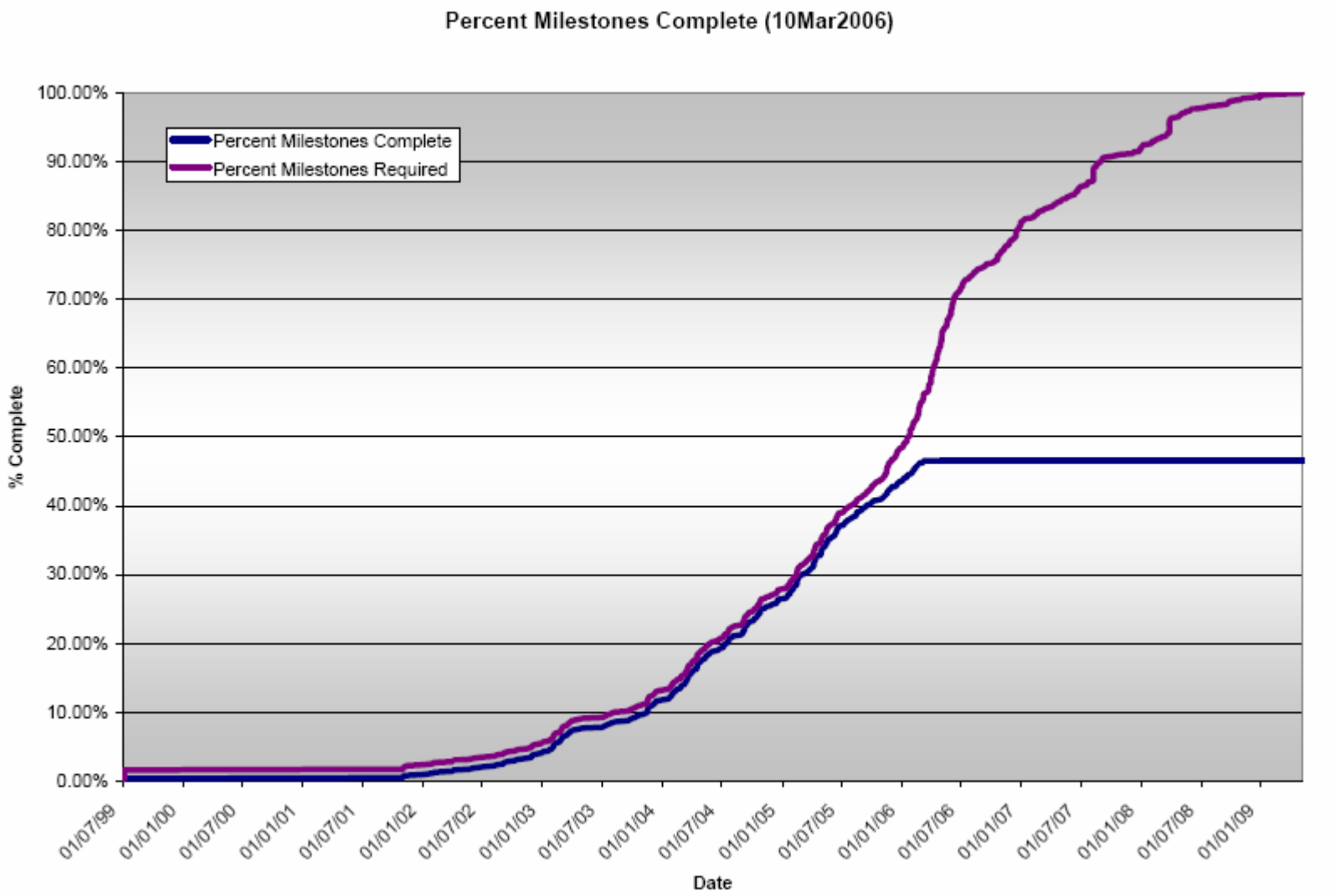
------ *Task 4: Power Plant Delivered to VLA Site has been added to schedule.*

------ *Task 9: High-Speed Inter-Rack Cables Delivered to and Installed at VLA Site has been added to schedule.*

------ *Task 10: Racks Delivered to and Installed at VLA Site has been added to schedule.*

Project: EVLA_LongTerm_12Apr2006_v1
Date: Wed 12/04/06

Milestone Progress



Project Management

- Schedule
  - Detailed schedule periodically updated.
  - Near-term (target) schedule updated weekly.
  - Long-term schedule discussed monthly, and cross-checked against detailed schedule.
- Budget
  - Projections updated with schedule.
- Bills of Materials (BOM's)
  - 1000's of components.
  - Maintenance required.

Correlator Documentation

- Master Document Tracking Spreadsheet Maintained at DRAO.
- 115 documents written so far, including “Memos”.
- Additional 23 documents with designations and titles are anticipated.

Principal Design Reviews

- Three Design Reviews:
  - Conceptual (CoDR – Nov, 2001)
    - Review architecture and overall design.
  - Preliminary (PDR – July, 2005)
    - Review detailed designs before prototypes.
  - Critical (CDR)
    - Review system before “limited production” stage.
    - Scheduled for Q2/Q3, 2007.

Non-Technical Program Risks

- Funding
  - Original allotment of funds was over five years.
  - NRC management was made aware in Aug/03 that this does not fit the project spending profile – they decided that internal cash management could deal with the problem.
  - Will have to apply for an extension, which in the present climate presents a risk.
  - Worst case is that project could hypothetically be halted in April 2008.
  - Active cash management at HIA, NRC level.
- Schedule slippage?
  - Due to a slow start (already happened at the beginning).
  - Concerns over procurement processes.
    - This risk is retired. Major procurement contracts are in place except for power supply.
  - Technical progress slower than the deliberately aggressive initial schedule.
  - "Re-spins" will present additional schedule risk.
- Inadequate contingency?
  - The contingency fractions are much smaller than most high-tech projects.
  - Cost risk will be reduced quickly once prototypes are tested.
  - Exchange-rate changes have been favourable to date.
- Inflation not being recognized in funding profile?
  - Inflation is a corrosive influence.

Technical Program Risks

- Technical risk is currently at a maximum
  - Much design effort and prototype expenditure has taken place.
  - Prototype hardware is being fabricated (or about to be fab'd), but not received/tested.
- But …
  - Considerable design effort expended to reduce technical risk.
    - Finely divided testing schemes for circuit boards – every path can be checked independently.
    - Correlator chip underwent an independent test and verification process, including a major simulation campaign after the "place-and-route" stage.
    - A separate Design for Manufacturability (DFM) analysis done for circuit boards – results in a major reduction in risk.
- Formal system reliability analysis has been done, and will be updated.
- Funds and design effort has been expended to minimize technical risk.
  - We are optimistic and confident that technical risk is reasonably low.

Descoping

- The correlator is difficult to split, once designed, and saving is inefficient.
- Have not reconsidered descoping options since the budget is currently “under control”.
- If the previously-mentioned non-technical risks become imminent concerns, then de-scoping options will have to be revisited.

Project Summary

- Are we meeting the required schedule?
  - We are sticking with the original delivery date, although there is now some squeezing of activities towards the end.
- Are we over budget at this stage?
  - Budget is slimly allocated, but we are not over budget.
- Are we planning to deliver on what we said we would do?
  - Yes, with minor improvements.
- What are the major risks at this stage?
  - Hypothetical funding difficulty in 2008.
  - Technical risks should be reduced this year as prototypes are tested.

End