EVLA Correlator

P. Dewdney
Dominion Radio Astrophysical Observatory
Herzberg Institute of Astrophysics

National Research Council Canada

NRC · CNRC

Outline

1. Funding
2. Review of Key Correlator Capabilities
3. Technical Progress
4. Project Progress
5. Review of Cost, Schedule and Risks

NRC · CNRC

Funding in Canada – No Change

- Aug/03 – Treasury Board approval of submitted budget ($C 20M over 5 years).
- $US/$C = 0.82-0.85 (40% increase over 2 yr).
  - Currently OK, but rapid changes are likely either way.
  - Only a small fraction of funding has been spent: if the $ ratio drops again, the project could be in funding difficulty.

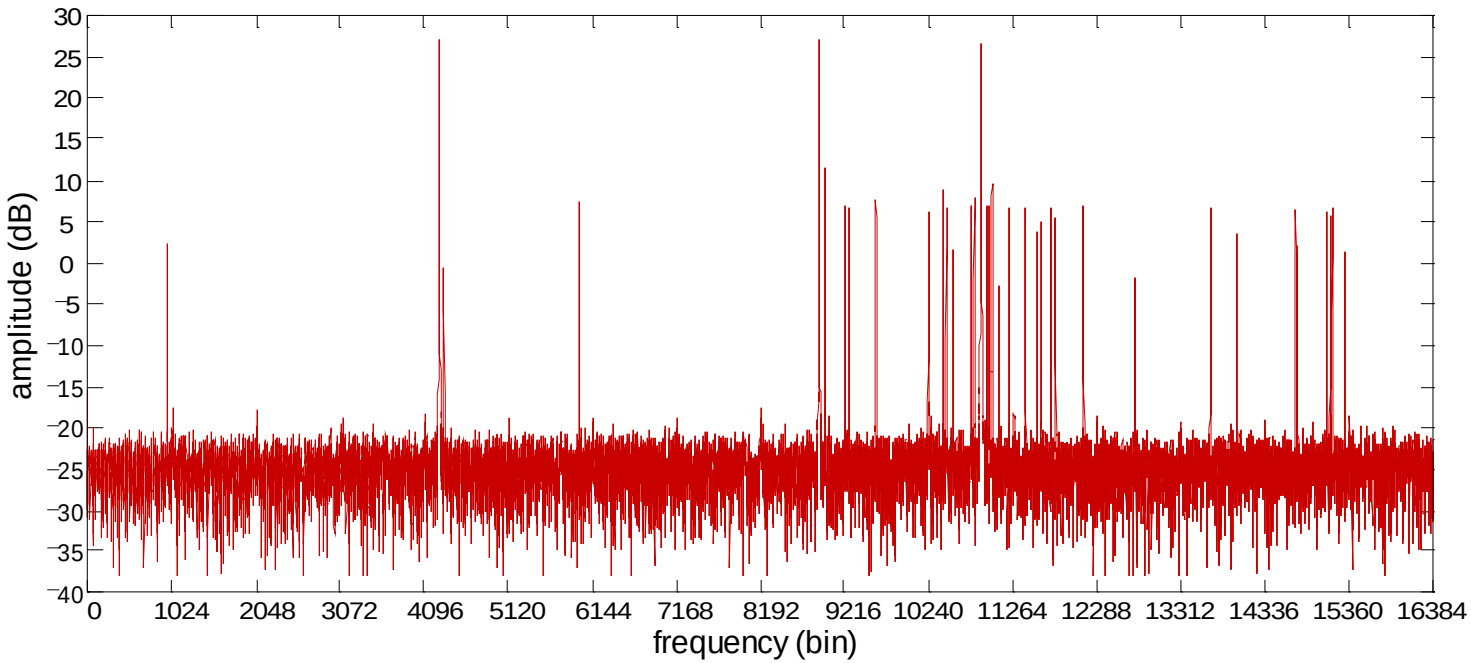
NRC · CNRC

Key Correlator Capabilities

Raw Bandwidth, Large No's of Channels

- **16 GHz** bandwidth per antenna in 2 GHz analog basebands. (8 x 2 GHz)
- **16384 spectral channels** at widest bandwidth over the 16 GHz.
- Targetable sub-band feature:
  - provides flexibility. Can trade off:
    - bandwidth for spectral resolution.
    - polarization modes for spectral resolution.
    - bandwidth for more antennas
    - bandwidth for delay centers ("beams") (phased VLA)

Example 16000 ch. Spectrum



NRC · CNRC

Key Capabilities

Flexible Configuration Trade-offs

- Reconfigurable, expandable architecture.
  - Can trade antennas for bandwidth.
- 32 stations input, expandable to 40.
  - EVLA Phase II will add ~8 antennas.
  - Local VLBA antennas will bring sum to 40.
  - physical infrastructure for expansion to 48.
- VLBA/VLBI capable.
  - Growth path to include tape-based or real-time VLBA antennas (“two correlators for the price of one”).

NRC · CNRC

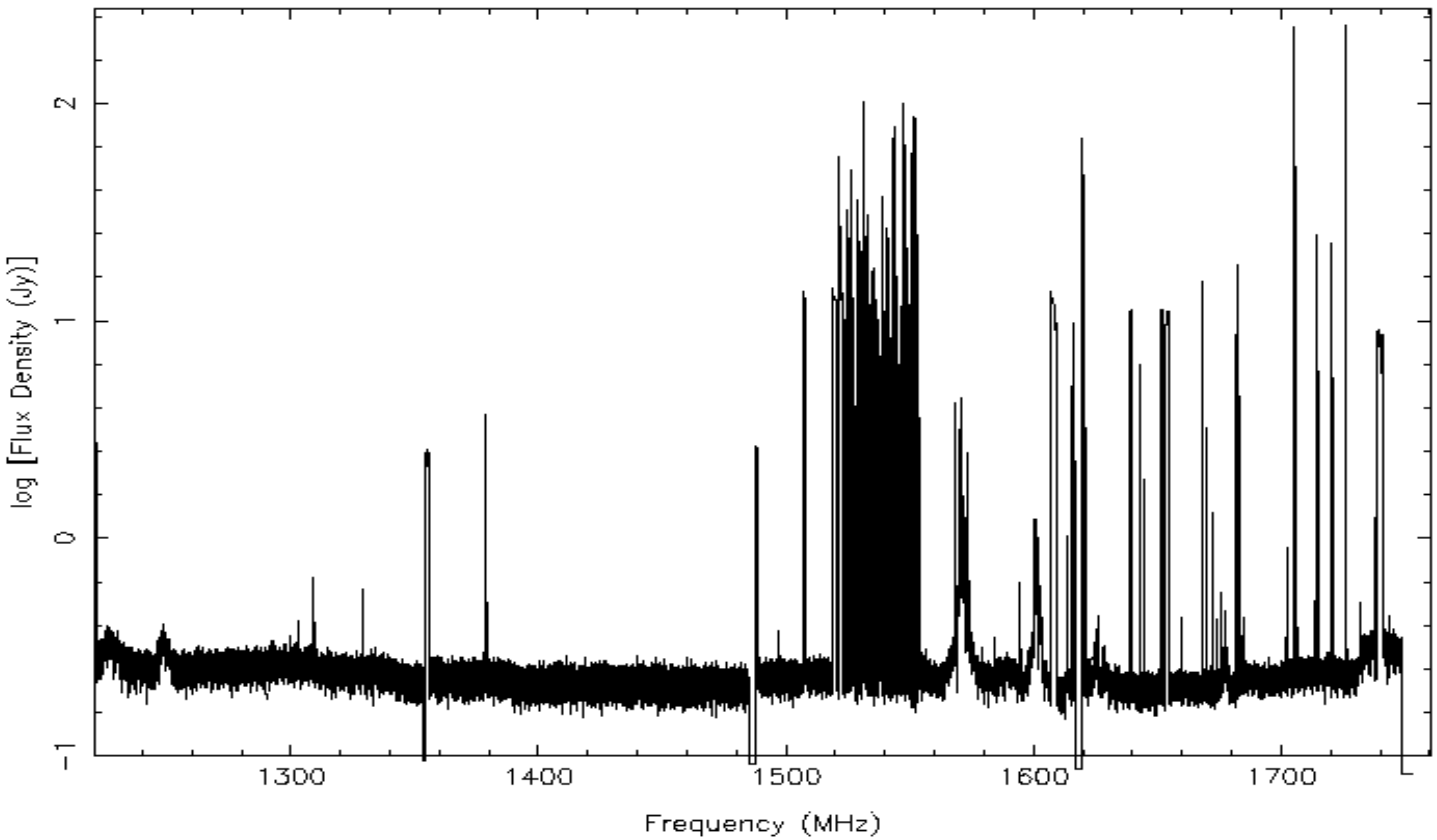
Key Capabilities

High Spectral Dynamic Range

- 4-bit/8-bit correlation
  - 4 bits are used internally, antennas deliver 3-bit data.
  - 8-bit mode can be used at lower frequencies where the trade for bandwidth is cost-free.
  - High spectral dynamic range for very bright lines & **interference robustness**.
- The ability to avoid narrow spectral regions which are not of interest, or have the potential to be especially damaging.

NRC · CNRC

Interference Spectrum (single ant.)



NRC · CNRC

Key Capabilities

Pulsar "Phase" Bins, Rapid Dumping

- Two banks of 1000 narrow phase bins per cross-correlation result for pulsar observations.
- Dump time resolution down to ~20 us.
- good frequency resolution.

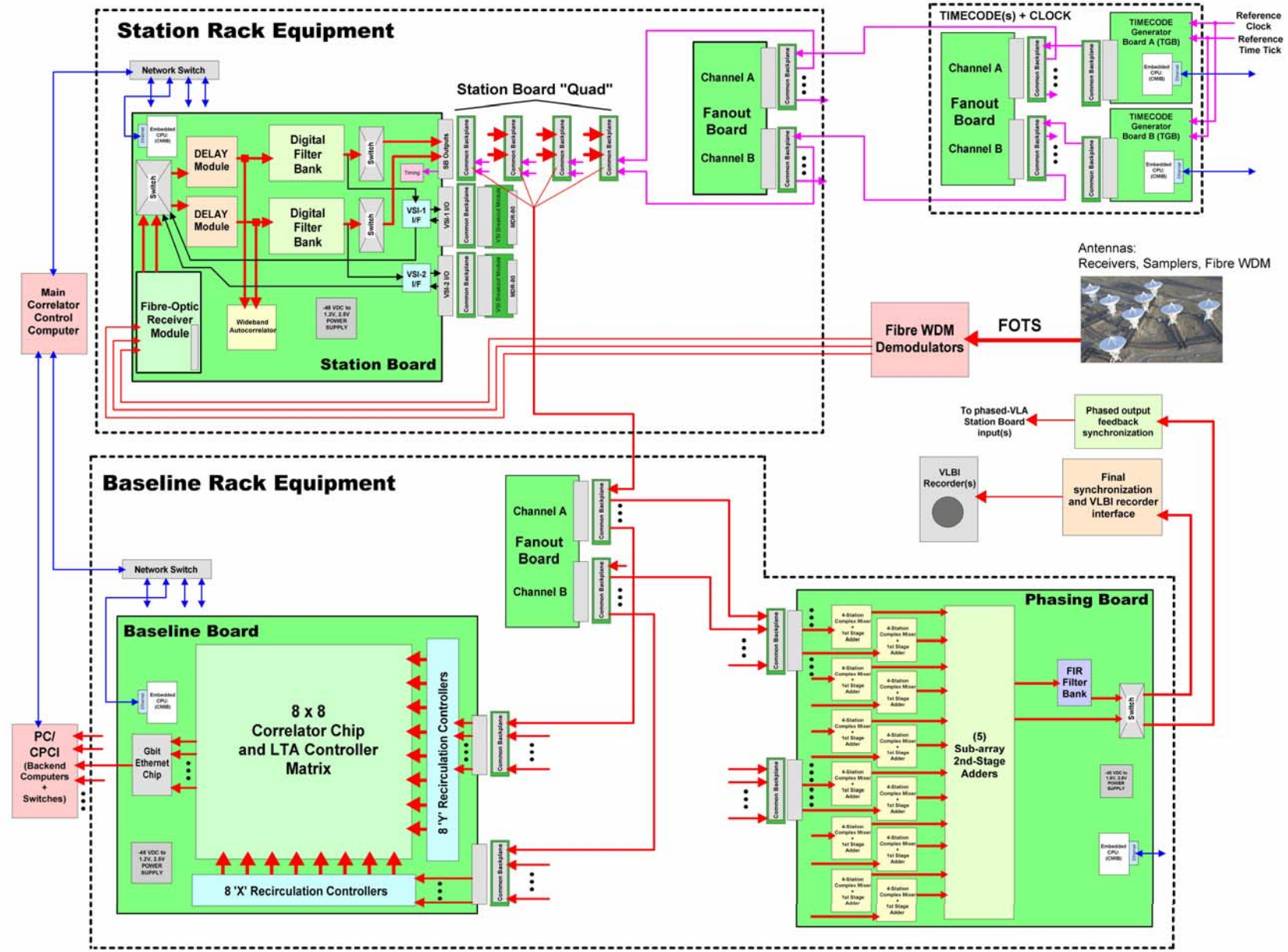
NRC · CNRC

Key Capabilities

"Single-dish" Capability, Sub-Arrays

- All digital **phased-VLA** sum (quasi-single dish mode) for VLBI and pulsar observing.
- Multiple sub-arrays.
  - E.g. Split array into two parts
  - use one part in phased-sum mode for real-time VLBI with VLBA and New Mexico antennas.
  - Use the other part in interferometry mode for another program.

EVLA Correlator System Diagram



NRC · CNRC

Station, Correlator & Phasing Boards

- Most of the design work is in a few key areas.
  - Station board
    - FIR chips & Delay module chips are the major items.
    - About 8 other designs which are much smaller.
    - Board, itself, not expected to be especially challenging.
  - Correlator board
    - Correlator chip & recirculation memory chip are the major items (75%).
    - Long-term Accumulator (LTA) much smaller design.
  - Phasing board
    - Deferred time but not reduced in priority.

NRC · CNRC

Additional Station Board Features

1. Radar Mode: Software output available with some buffering (see project book).
2. Individual sub-band delays available (32 μs at the highest data rate).
3. Standard VSI interfaces for VLBI
   - Saves optical switch in front of station boards for VLBI recorders.
   - Provides 2 input and 2 output interfaces, each 32 bits x 256 MHz clock rate (e.g. 4 Gsamples/s @ 2 bits per input).
4. Staged FIR filter with SSB digital mixer after 1st stage.
   - Permits arbitrary placement of narrower bands within a sub-band at the expense of reduced stitching performance.
   - Yet more choices for the observer . . .

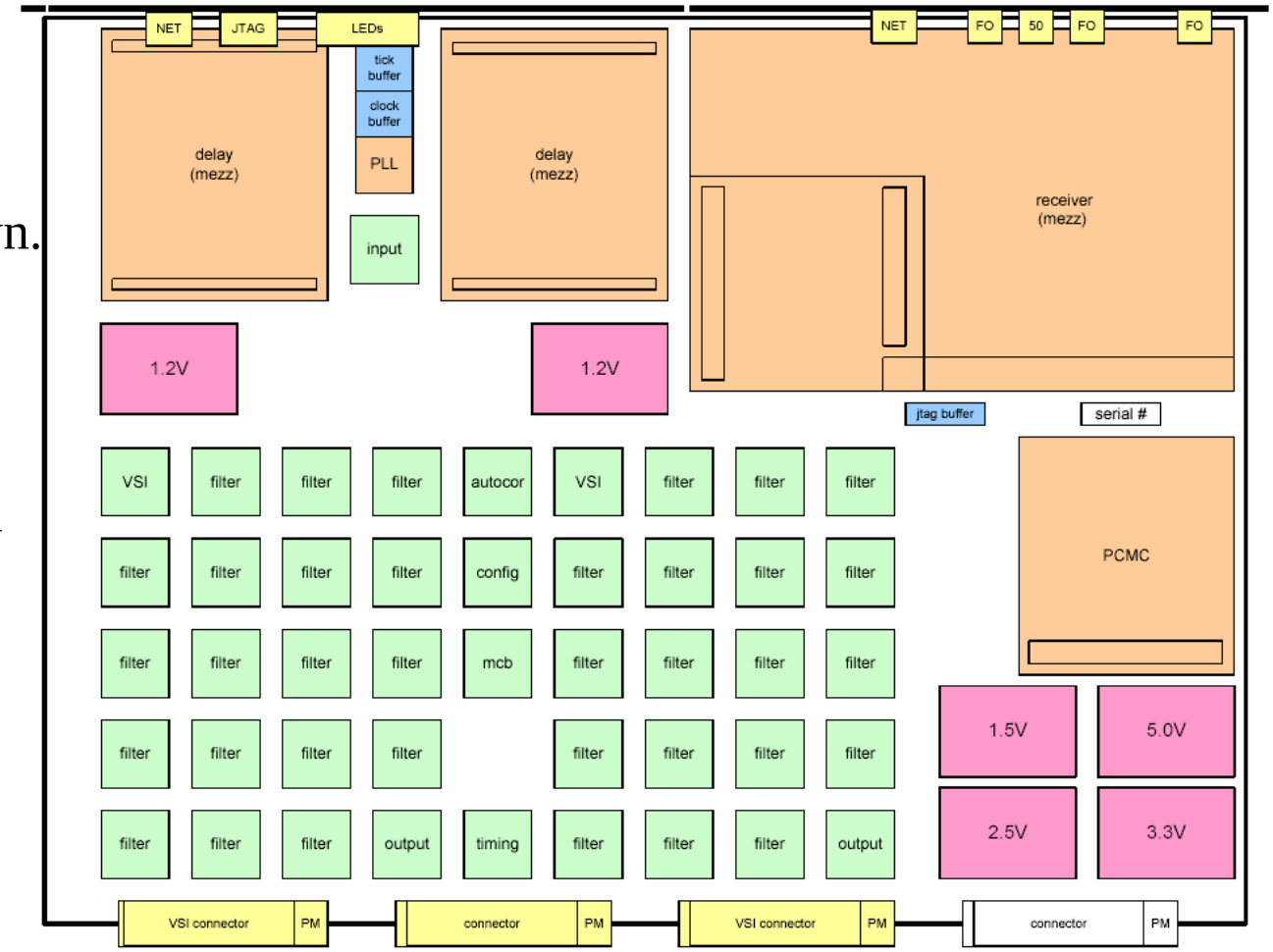
NRC · CNRC

Station Board Progress

1. FIR chip
   - Feasibility as FPGA has been in question for almost a year.
   - Design work for ASIC fall-back was started in parallel with continued FPGA work.
   - However, a reversal of direction has now occurred with the advent of a new Xilinx Vertex IV product.
   - Vertex IV implementation now assured with 6-7 W of power dissipation.
2. Delay Module
   - Complete but revisions may be needed to lower cost.
3. Overall Board Design
   - Schematic design almost complete.
   - Next step is “place and route” (done by outside contract).

Station Board Layout

- “Daughter” Board - brown.
- Power Supplies – pink.
- FPGA’s – Green
- Connectors – light brown and white



Size: ~510 x ~410 mm

NRC · CNRC

Correlator Board Progress

1. Correlator chip
   - Design complete, including optimization for either structured ASIC form, or full custom form.
   - Full Test & Verification Plan and extensive simulation testing via a “test bench”.
   - Two design study contracts have reduced risk of serious heat dissipation problems or rapid failure rates.
   - Firm cost estimates (at least ceilings) are established (considerably more expensive than first anticipated).
   - Reliability estimates provide guidance on feature size (130 nm ideally), in-service temperature (40-50C), and power supply voltage (1.02 V in core). MTBF minimum targets are 10^7 hours for a single chip. A reasonable goal is 10 x longer.
   - Procurement RFP has netted several proposals, which are now being evaluated by a group of engineers. Decision is expected to be in 1-2 weeks.
   - Correlator Chip CDR in late Jan/05.

NRC · CNRC

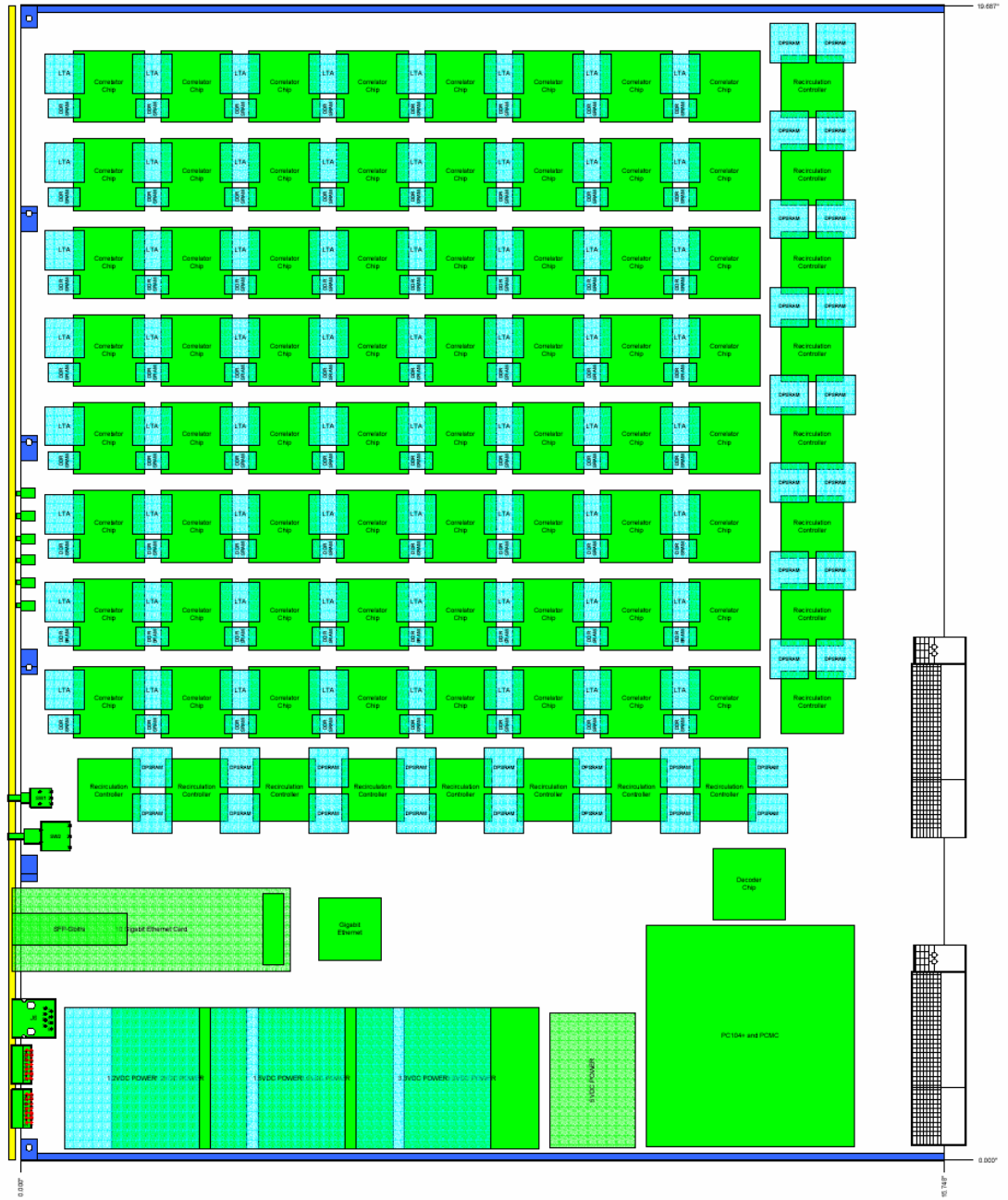
Correlator Board Progress (cont'd)

2. Other chip designs
   - All designs are complete

3. Correlator circuit board
   - Very crowded with signals (e.g. 90 wires from each recirculation controller to a row or column of corr. chips).
   - All signals are now "point-to-point". This is less risky than "busses", which were used in a previous rendition of the design.
   - Schematic design almost complete.

Correlator Board Layout

- Green chips – front side.
- Blue chips – back side.
- 8 x 8 array of correlator chips.
- LTA chips on the back side.
- Recirculation Controller.



NRC · CNRC

NRC · CNRC

Correlator Software People

- Sonja Vrcic (Penticton)
  - Coordinates overall design and specification.
  - Virtual Correlator Interface (VCI) definition.
  - Master Correlator Control Computer (MCCC) S/W.
- Bruce Rowan (Socorro)
  - Correlator hardware control S/W (CMIB)
- Tom Morgan (Socorro)
  - Correlator Backend software
- Ken Sowinski, Bill Sahr (Socorro)
  - Advisory capacity.

NRC · CNRC

Correlator Software Documentation

- Documentation: Vrcic, Rowan, Morgan (V, R, M)
  - Generating Baseline Board Configuration Based on the Configuration of Station Boards (Memo 18 - V)
  - Requirements and Specifications (RFS) – MCCC (V)
  - Protocol Spec. – Virtual Correlator Interface (VCI) (V)
  - Correlator S/W Architecture (V & R)
  - Correlator S/W Development Practices & Coding Conventions (V)
  - RFS – Timecode Generator CMIB Prototype S/W (R)
  - RFS – EVLA Correlator Backend (M)

NRC · CNRC

Memo 18: Correlator Control

- Purpose:
  - Analyze correlator hardware architecture,
  - Use the analysis to develop a rules-based approach for controlling the configuration of the hardware in the simplest way possible.
- Access to control S/W:
  - via commands sent across the VCI.
  - This part of the VCI will be the “face of the correlator” as seen by the EVLA M&C.
- Relies on well-known principles to maximize functionality & simplicity:
  - knowing the state of the system at all times
  - developing a command set that covers as many configurations as possible without resorting to a list of "arbitrary modes".
- Result:
  - system that can carry out all of the required correlator functions and can support several simultaneous "users".

Memo 18: Correlator Control

- The M&C:
  - specifies antennas to be used for a particular sub-array
  - the configuration of the station boards associated with subarray antennas.
  - also specifies the required correlator output products for the subarray.
  - can allocate and deallocate correlator resources indefinitely.
- The MCCC software:
  - provides consistency and resource checking to determine whether configuration commands can be implemented, and returns error messages appropriately.
  - derives Baseline Board configurations needed to provide the requested output (i.e. allocates Baseline Board resources to that subarray).
  - tracks the use of resources at all times, and can provide this information to the M&C at any time.
- The M&C:
  - can also directly specify the use of particular correlator resources, if available (envisaged mainly for testing).

NRC · CNRC

Correlator Documentation

- Master Document Tracking Spreadsheet Maintained at DRAO.
- 63 documents written so far, including “Memos”.
- Additional 45 documents with designations are anticipated.

NRC · CNRC

Project Management

- Work Breakdown Structure (WBS) complete.
- Schedule complete and being tracked.
- Budget is complete and being tracked.
- Bills of Materials (BOM's) for major subsystems are under good control.
- Integrated project tracking system (integrated WBS/Schedule/Cash flow) still being set up.

NRC · CNRC

Design Reviews

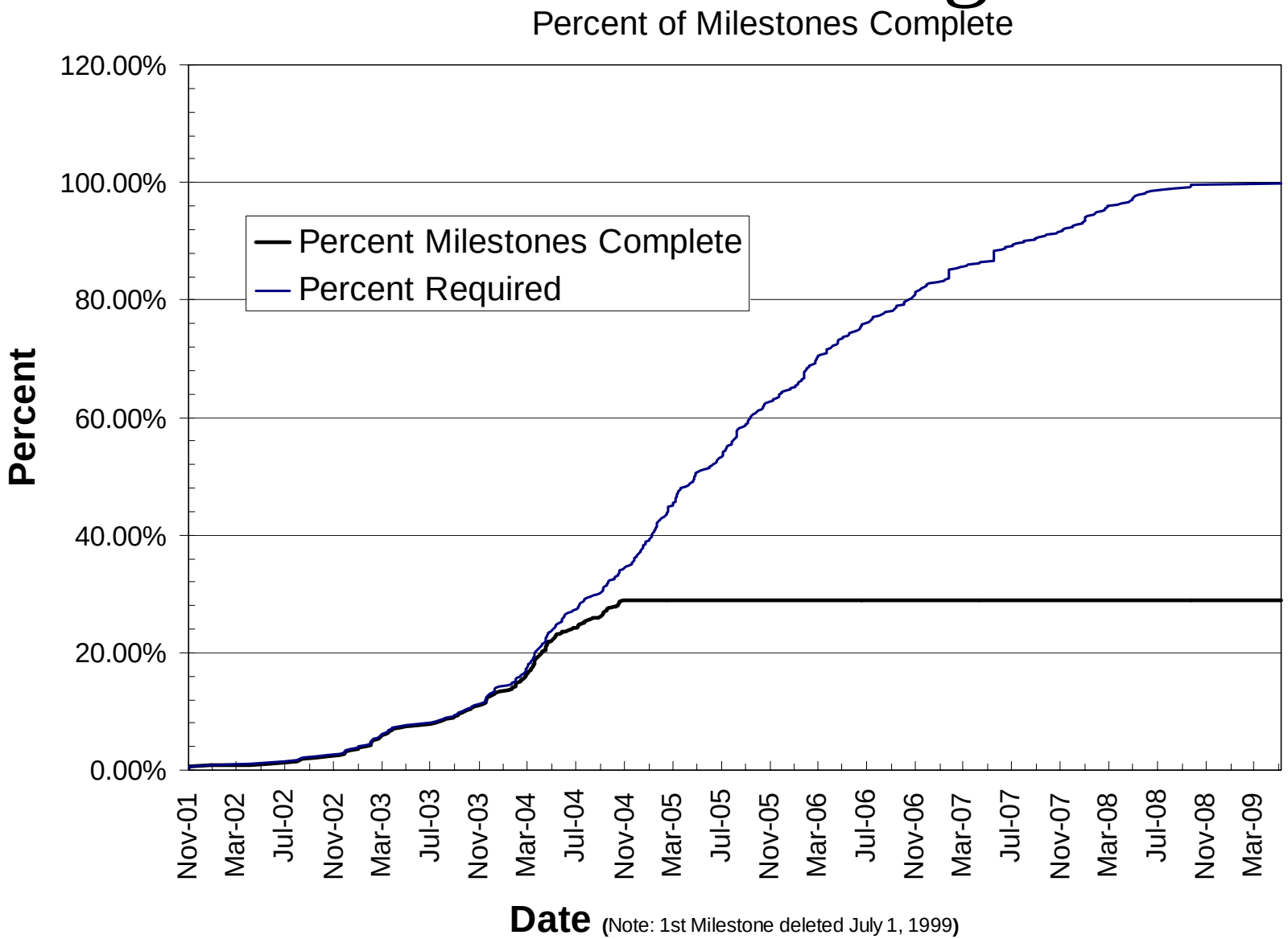
- Three Design Reviews planned:
  - Conceptual (CoDR - complete) - review architecture and overall design.
  - Preliminary (PDR) - review detailed designs before prototypes.
  - Critical (CDR) - review system before major production.

NRC · CNRC

Major Milestone Projection

WBS Number	Milestone Name	Milestone Date
2.2.6.2.10	Correlator Chip ASIC Critical Design Review Complete	28-Jan-2005
2.1.1.1.12.14	FIR Filter Chip Critical Design Review Complete	18-Feb-2005
2.1.6.3	**Preliminary Design Review Complete**	27-Jul-2005
2.2.2.8	Final System Design Review Complete	20-Apr-2006
4.2	System Test Plan Complete	6-Jul-2006
2.2.4.4	On-The-Sky Testing Complete	17-Aug-2006
2.2.5.3	**Critical Design Review Complete**	2-Oct-2006
2.3.2.12	Limited Production Run Complete	21-Feb-2007
3.3.8.12	MCCC Software Complete	3-Jul-2007
2.3.3.10	Full Production Run Complete	6-Sep-2007
3.3.7.24	Backend Software Complete	30-Nov-2007
4.10	Final System Acceptance Complete	2-Jan-2008
3.3.9.9	CPCC Software Complete	19-Feb-2008
5.8.10	Start Shared-Risk Observing	2-May-2008
5.9.8	Final Correlator Acceptance Complete	23-Sep-2008
6.1	Commissioning Begins	23-Sep-2008
6.5	Commissioning Complete	7-May-2009

Milestone Progress



Test & Verification Plan (Carlson)

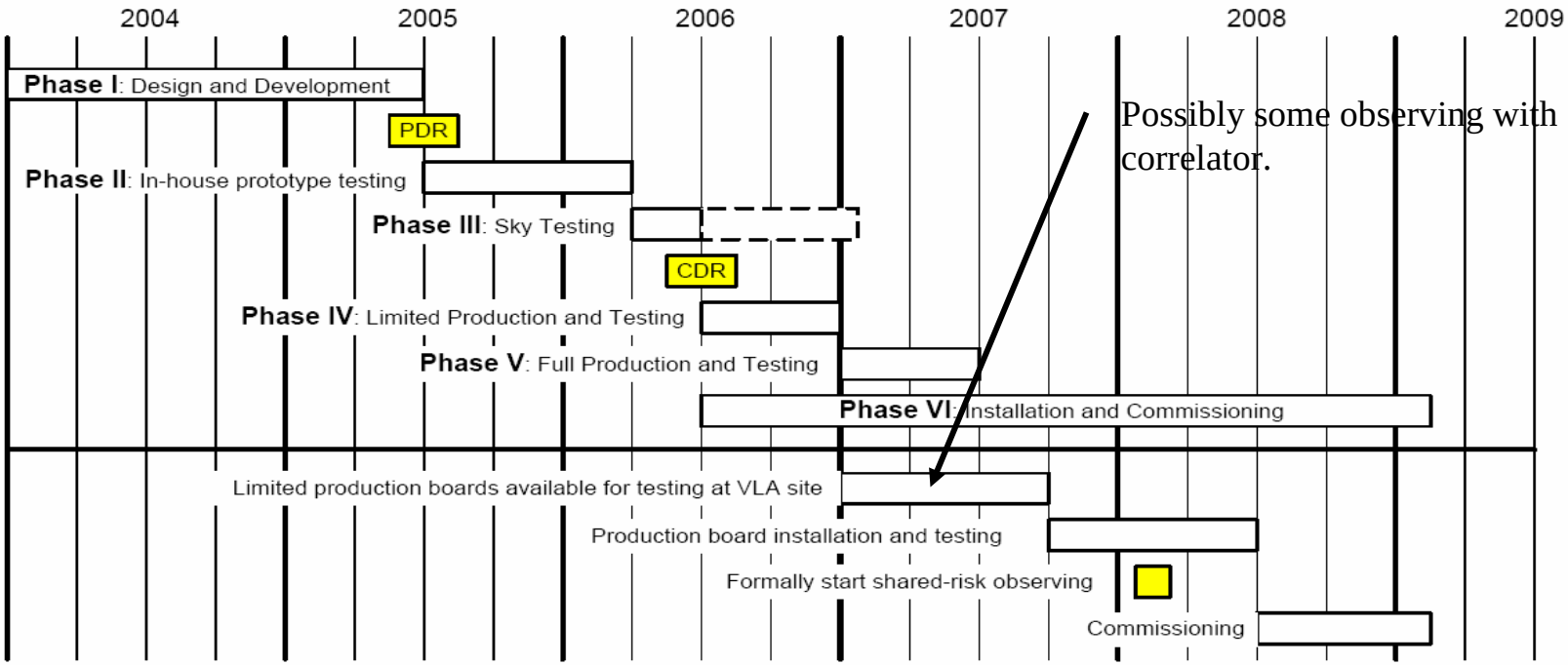
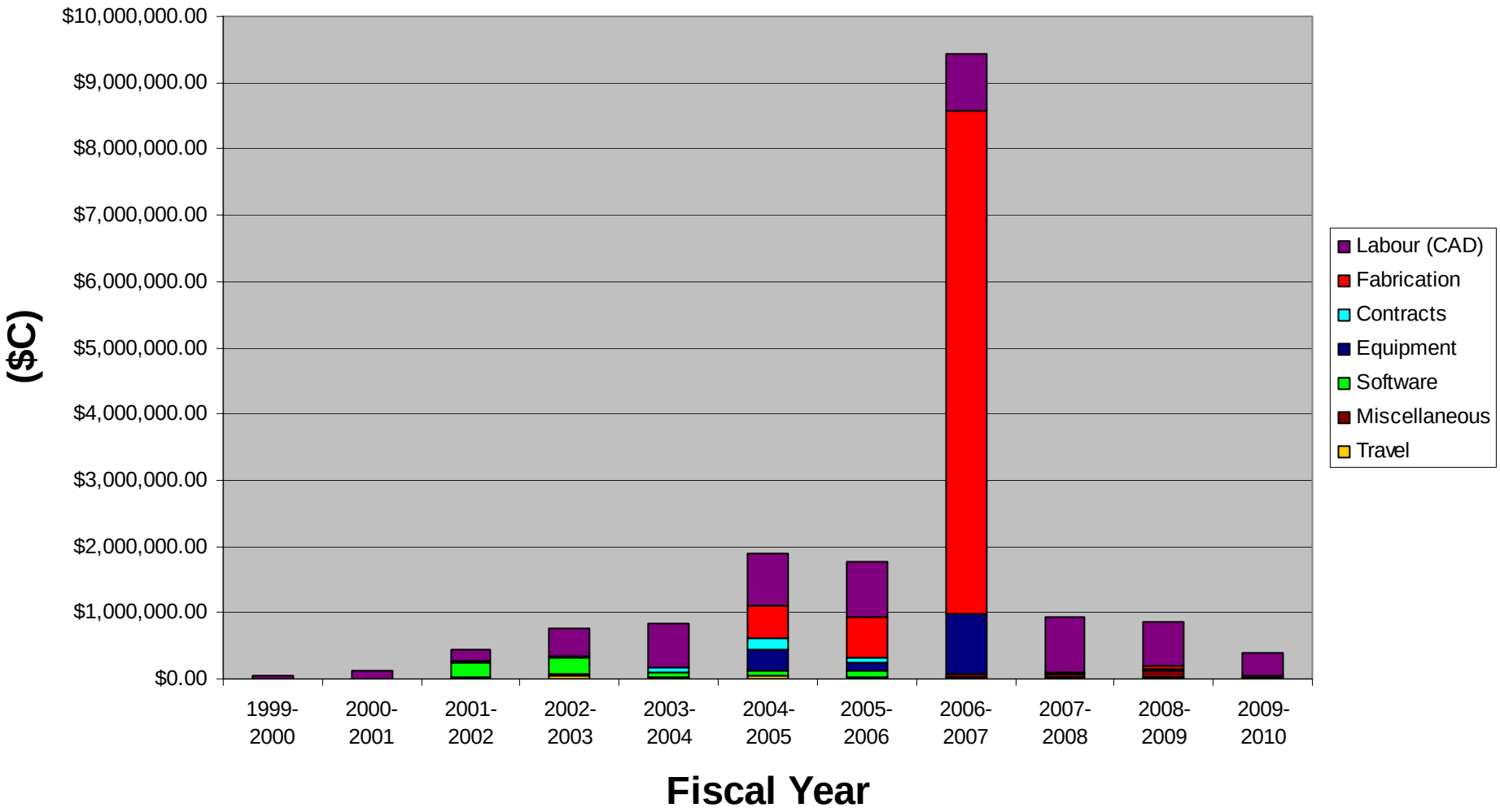


Figure 3-1 Simplified Gantt chart showing the phases of development, fabrication, and testing in the project. This schedule is developed from the current project schedule. Note that software development does not end with Phase I, but continues for most of the rest of the project.

Spending Profile (as of 08Oct2004)



NRC · CNRC

“Risk-based” Contingency Allocations

Contingency Table	%
Correlator Production Cost	17
Labour Cost	20
Non-Refundable Engineering Cost	30
Miscellaneous Project Cost	10

Non-Technical Program Risks

- Schedule slippage?
  - Due to a slow start (already happened).
  - Possible concern over procurement processes.
    - Attempts being made to reduce number of actual procurements, especially for circuit board fabrication.
- Inadequate contingency?
  - The contingency fractions are smaller than most high-tech projects.
  - Cost risk will be reduced as design matures.
  - Advantage of new technology developments (e.g. Vertex IV Xilinx chips have enabled FPGA's to be used for FIR chips).
  - Exchange rates changes can occur quickly.
- Inflation not being recognized in funding profile?
  - Industry stagnant - not a concern at present.

NRC · CNRC

Descoping

- Have not reconsidered descoping options since the last Advisory Board meeting.
- If the previously-mentioned program risks become imminent concerns, then de-scoping options will have to be revisited.

NRC · CNRC

Project Summary

- Are we meeting the required schedule?
  - We are somewhat behind the original schedule for shared-risk science. Overall the project remains on the original schedule.
- Are we over budget at this stage?
  - Budget is slimly allocated, but we are not over budget.
- Are we planning to deliver on what we said we would do?
  - Yes, with minor improvements.
- What are the major risks at this stage?
  - Procurement delays.