CompactPCI Technology

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CompactPCI uses ...

- PCI Electricals
  - 32/64 bit multiplexed address/data path
  - 33/66 MHz clock rate
  - Synchronous single transfer and block mode signalling
  - Developed by INTEL in 1992 as a chip level interconnect for motherboards
  - Extended for option cards in 1994, updated most recently in 1999 by PCI SIG

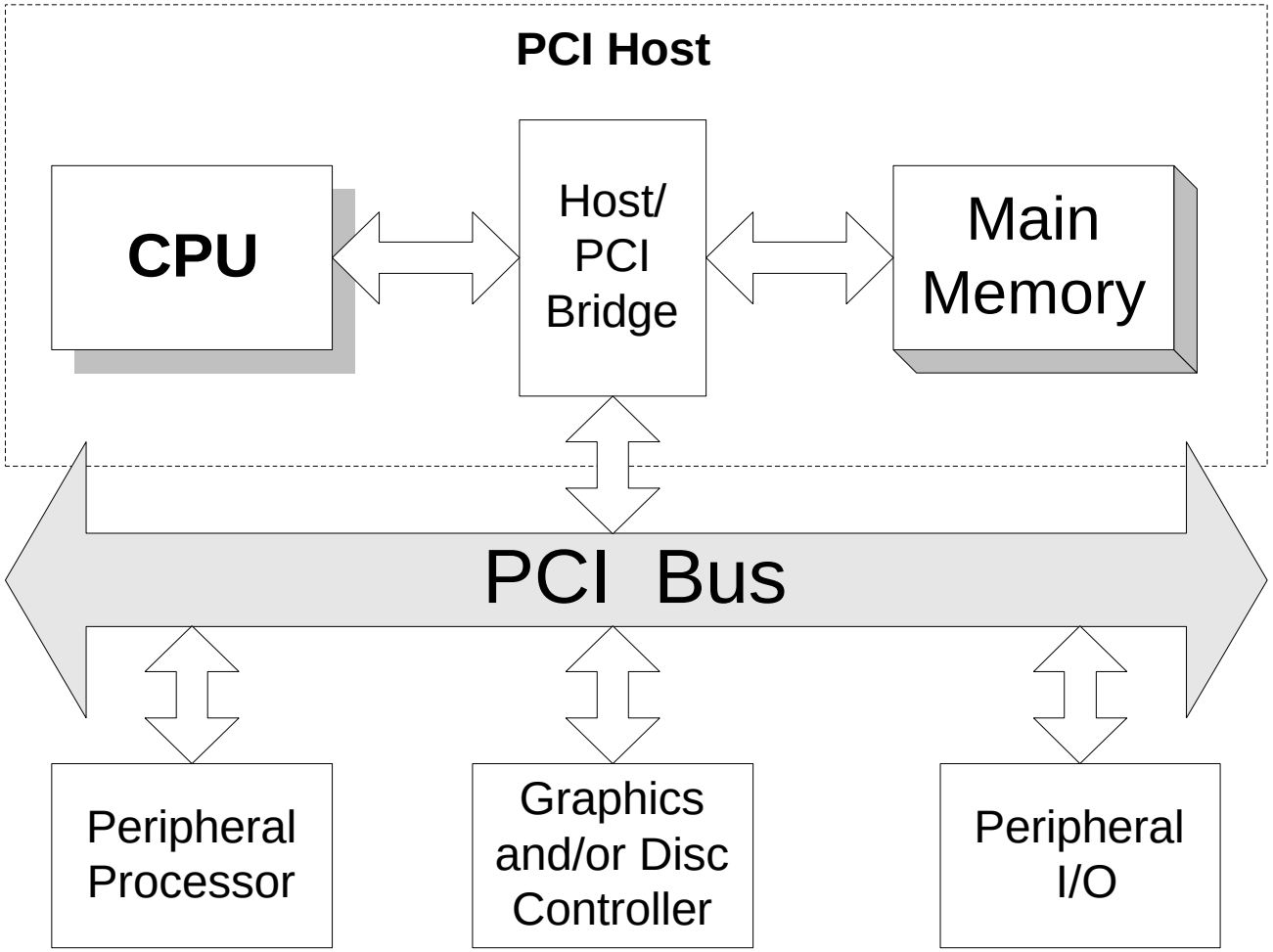
PCI Performance

- PCI bus Speeds
  - 133Mbytes/sec peak
    - 32bits, 5.0V, 33MHz bus clock
  - 266Mbytes/sec
    - 64bits, 33MHz bus clock
  - Theoretical Maximum of 532Mbytes/sec
    - 64bits, 66MHz, 3.3V
  - Extensible to 1066 Mbytes/sec
    - PCI-X, 64 bits, 133MHz

CompactPCI leverages ...

- "Standard" off-the-shelf PCI bus:
  - Processor core logic specific to processor architecture
  - Chip level peripherals stable across architectures and generations
  - Software and development tools in common with desktop and server systems

PCI System Architecture



Desktop PCI Slot Count

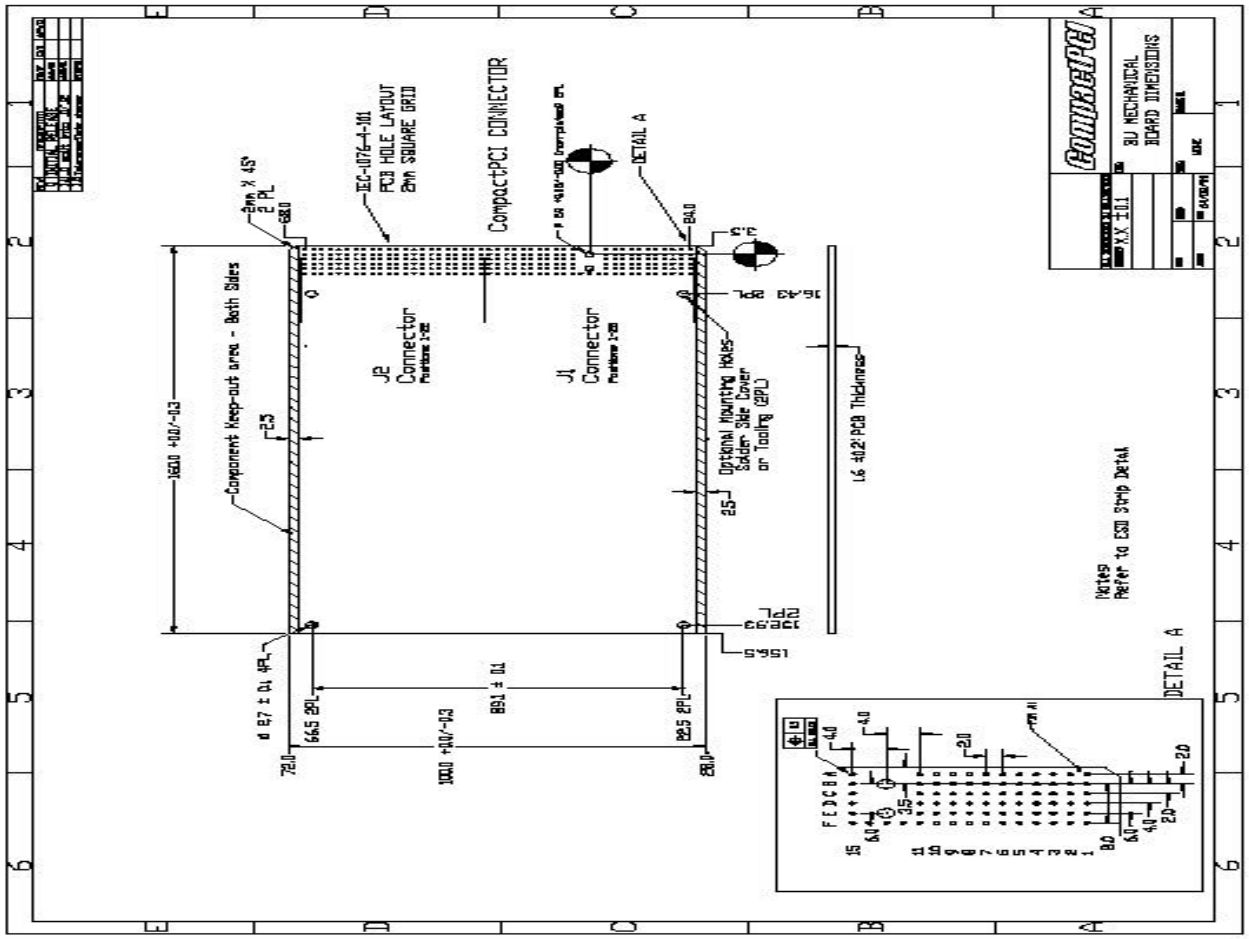
- PCI spec allows 10 loads:
  - A PCI chip is a load
  - Desktop connectors represent a load
- Desktop PCI: chip is 1 load, connector is 1 load = 2 loads per plug-in card.
- CPU support chipset and GPIO chip on motherboard = 2 loads
- Therefore, 4 slots/system maximum in desktop PC PCI without PCI to PCI bridging

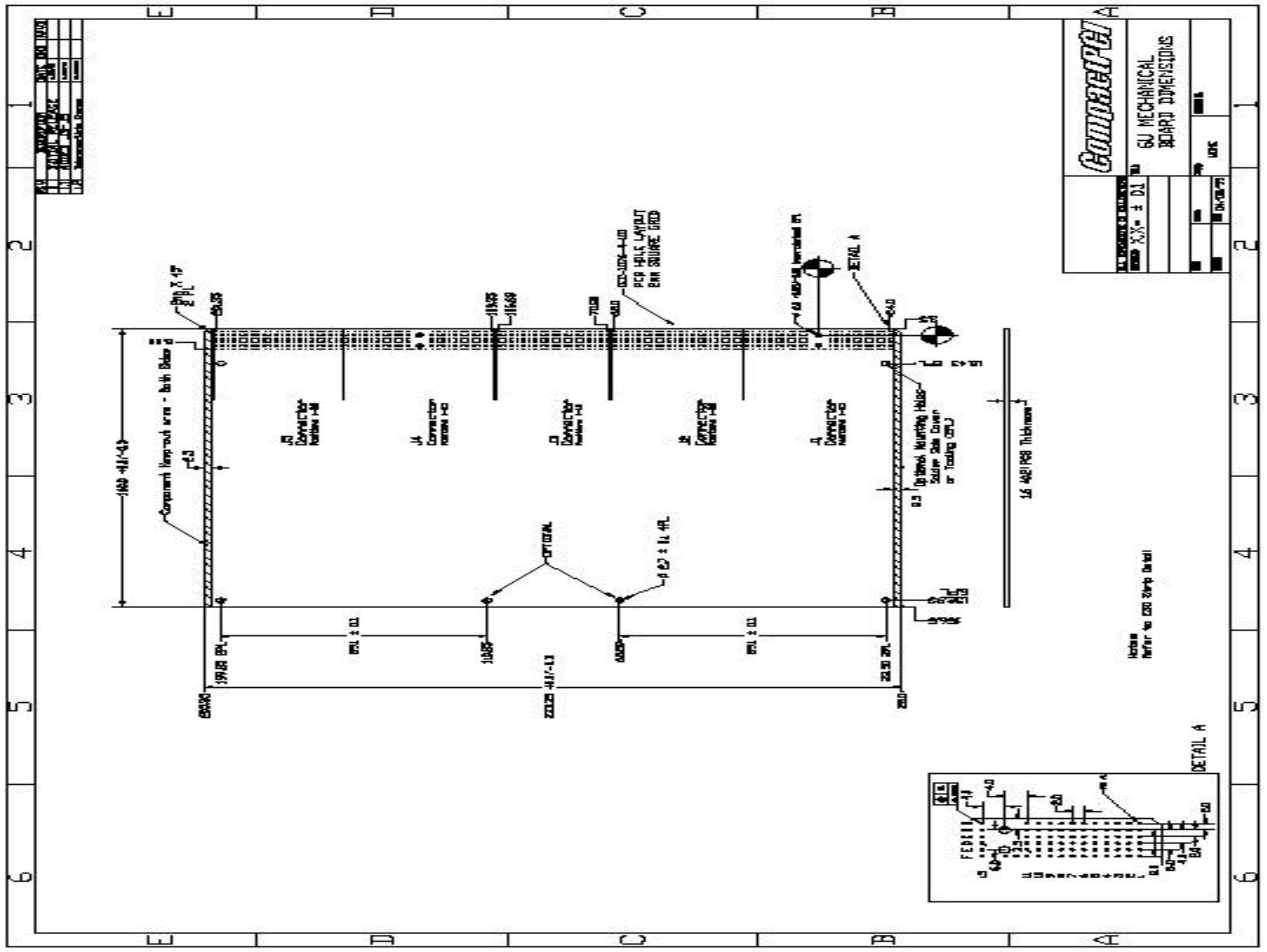
CompactPCI Slot Count

- ***CompactPCI***:
  - chip is one load
  - connector is approx. 1/8 load (controlled impedance, minimal reflections)
- Therefore, ***CompactPCI*** can have 8 slots
- Extensively simulated, tested
- This can be easily expanded with bridge chips (7 more slots/chip)

CompactPCI uses ...

- Eurocard Mechanicals
  - IEEE 1101.10
    - Improved Injector/Ejector
    - Better Grounding for ESD protection
    - Extensive shielding meets CE requirements
    - Alignment pins, keys, insert/eject handles
  - IEEE 1101.11 Allowed (Rear Panel I/O)
    - Standard method of providing rear panel I/O
    - 80mm card depth, mirrors front of chassis 3U/6U Modules


CompactPCI CONNECTOR
IEC-1076-4-101
PCB HOLE LAYOUT
2mm SQUARE GRID
DETAIL A
J2
Connector
J1
Connector
Component Keep-out area - Both Sides
Optional Mounting Holes
Solder Side Cover
or Tooling (2PL)
1.6 ±0.2 PCB Thickness
DETAIL A
Notes
Refer to ESD Strip Detail



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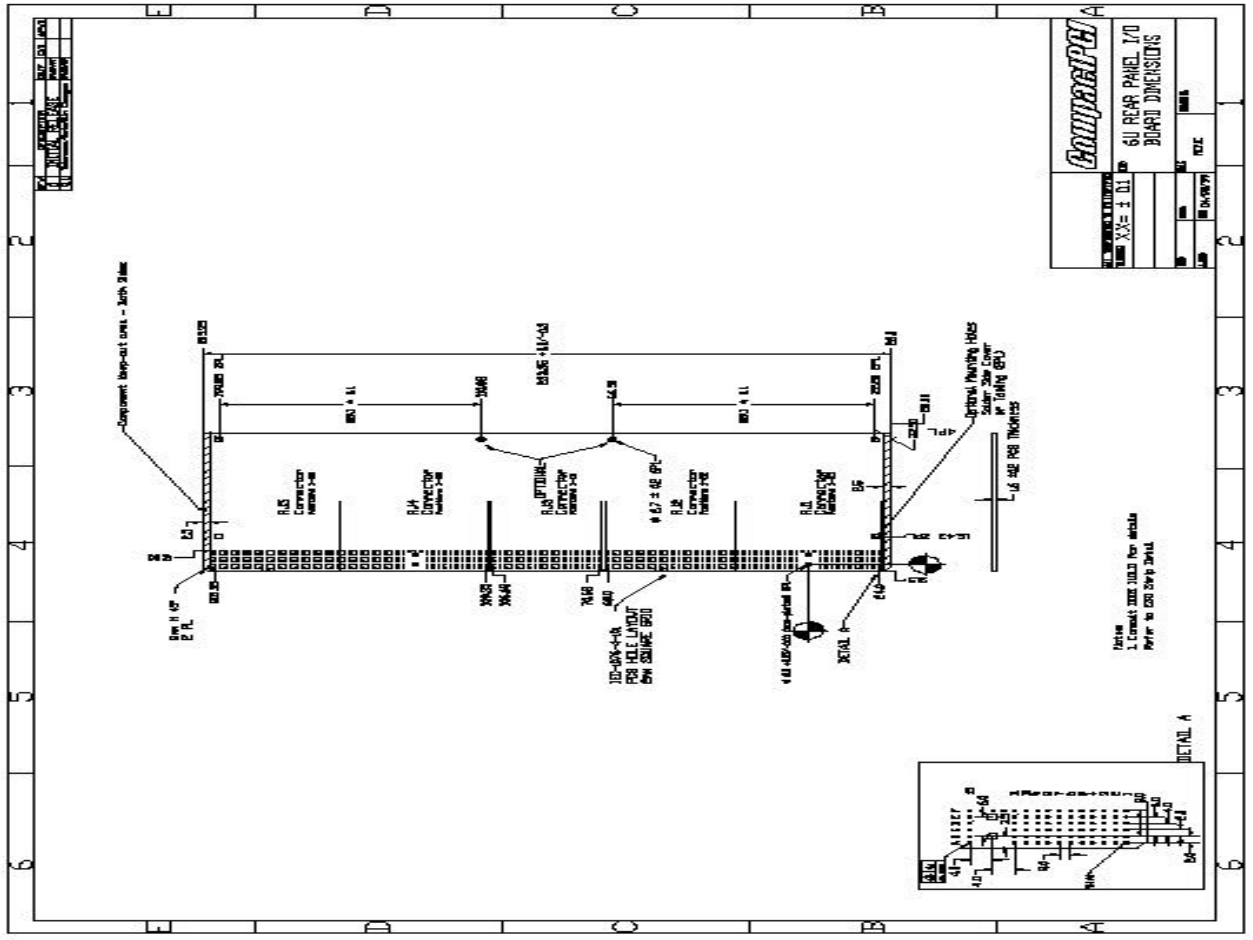

6U REAR PANEL I/O
BOARD DIMENSIONS

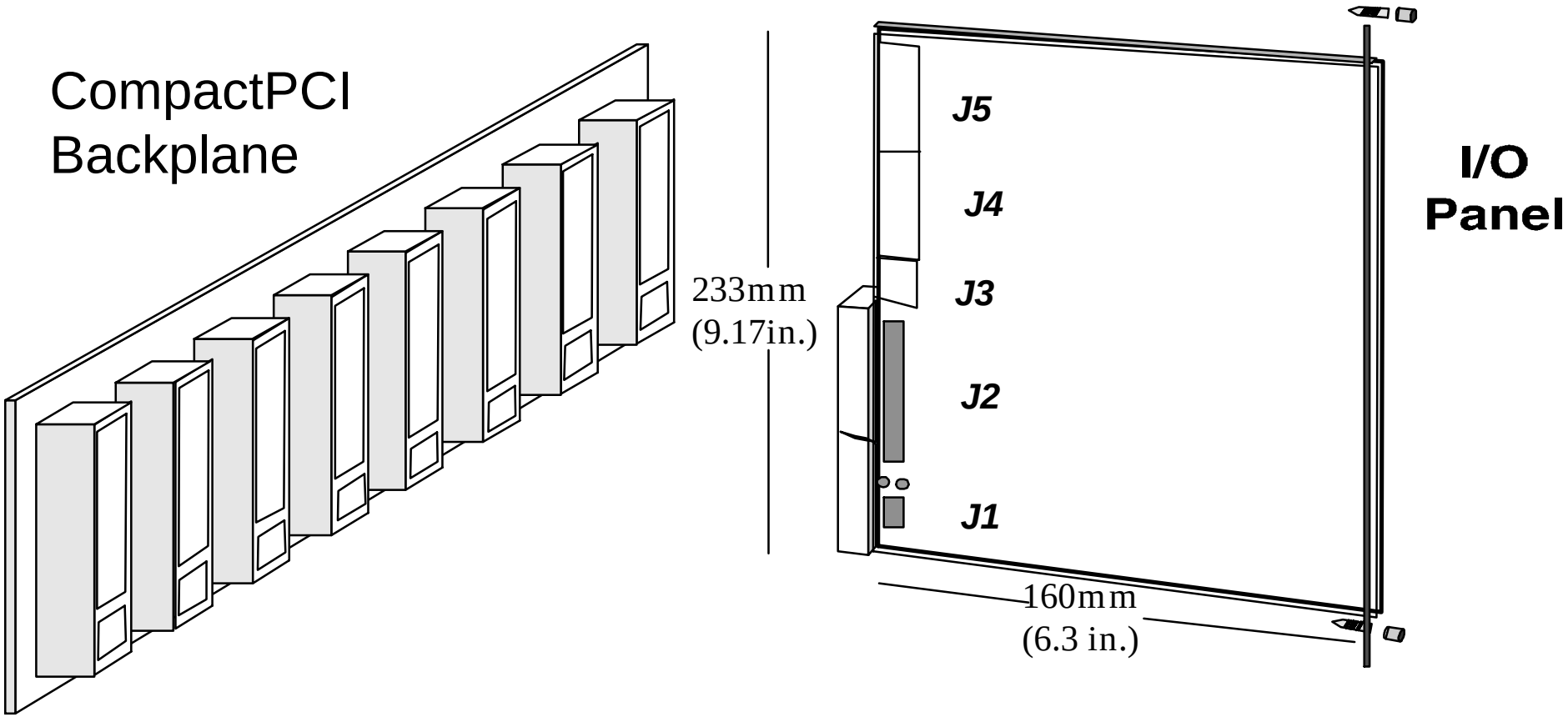
CompactPCI uses ...

- 2 mm pin-and-socket type
  - socket half on plug-in cards
  - Pin half on backplane
- Originally developed by Siemens for telecom applications
- Meets IEC-917 and IEC 1076-4-101 standards

CompactPCI connector

- IEC 61076-4-101 connector utilization
  - J1/P1 for 32 bit PCI (110 pins)
  - J2/P2 for 64 bit extensions (110 pins)
  - J3/P3 for rear IO (95 pins)
  - J4/P4 for H.110 CT bus or rear IO (110 pins)
  - J5/P5 for general purpose or telecom IO (110 pins)

CompactPCI Components



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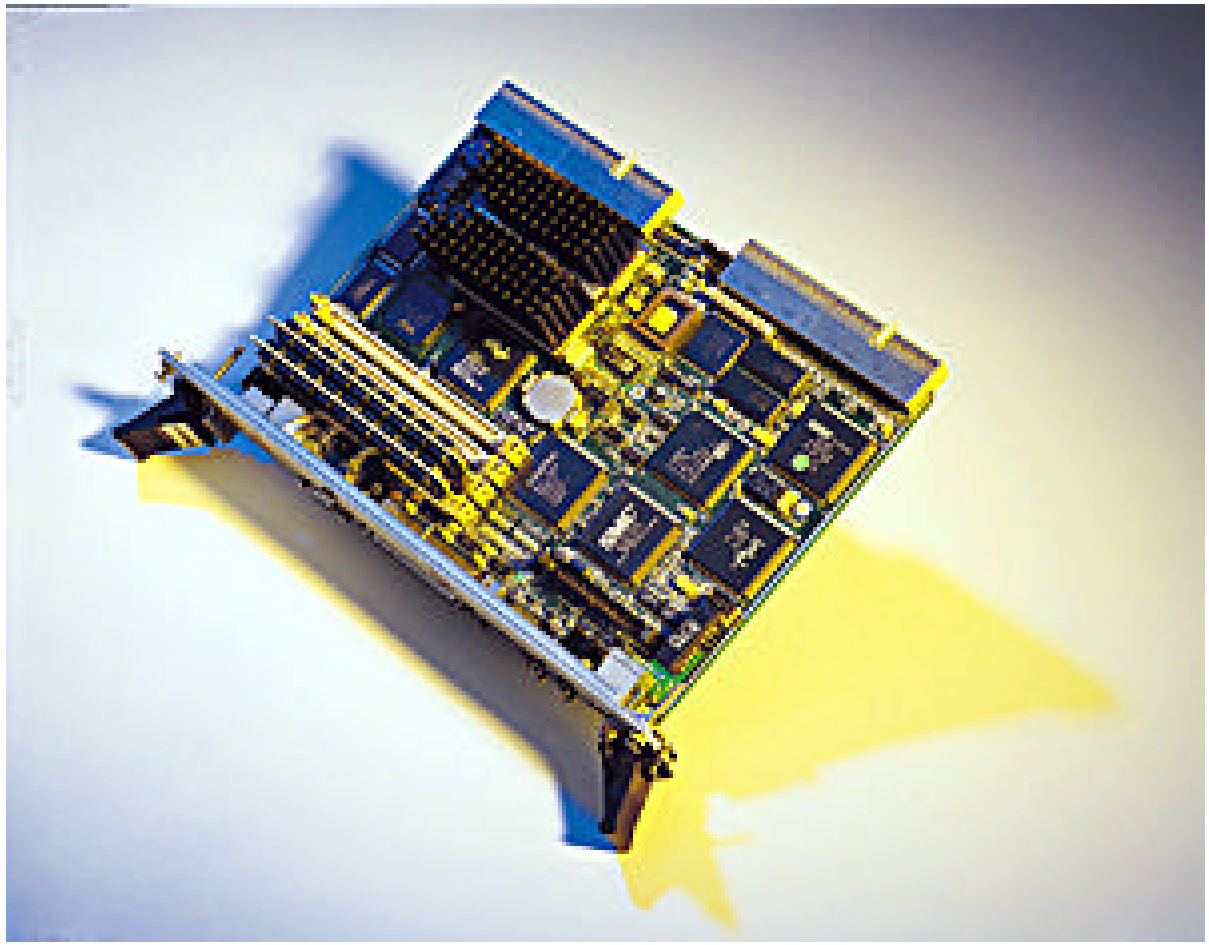
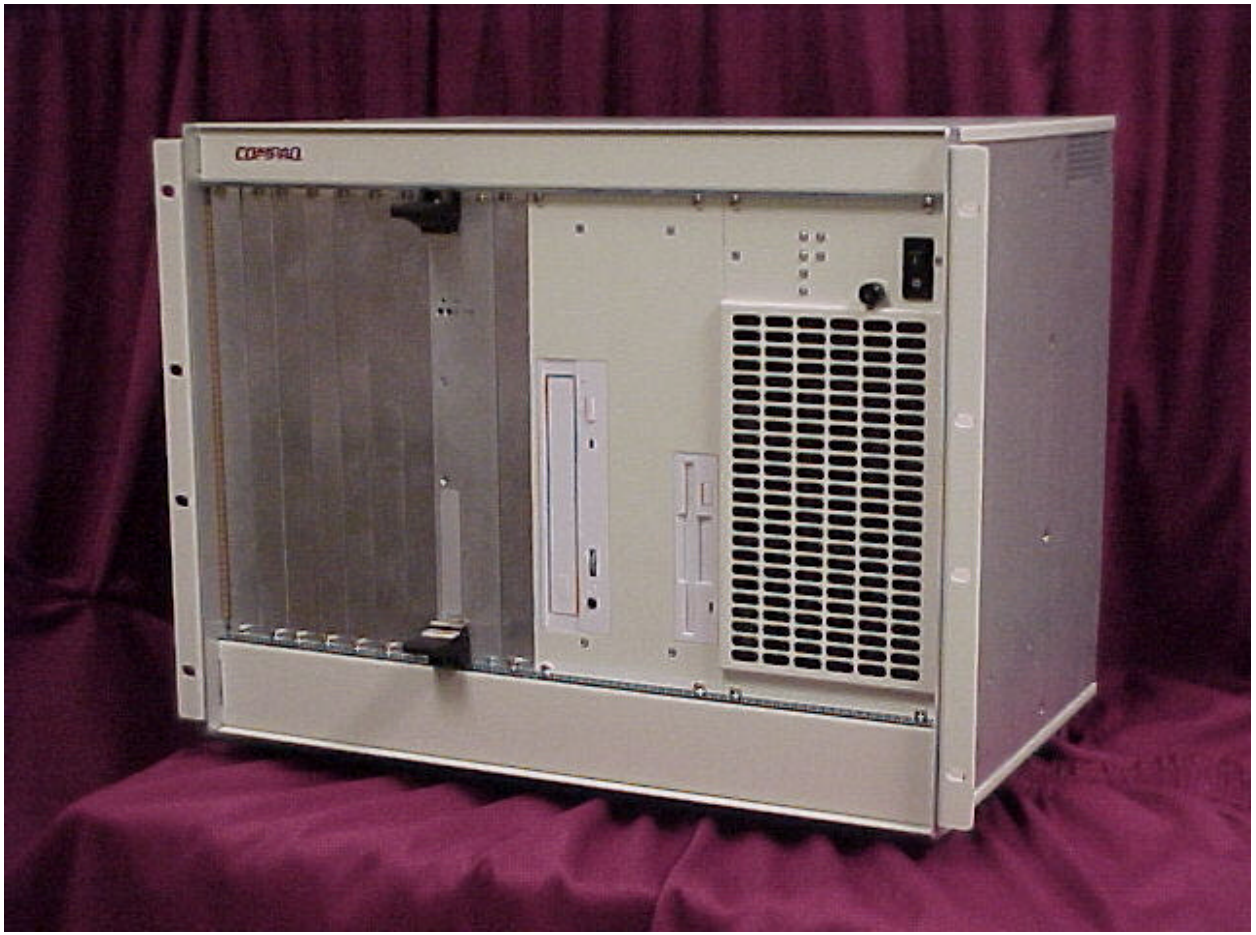
CompactPCI SBC



CompactPCI System



CompactPCI leverages ...

- General purpose desktop and server architectures
  - Intel processors and chipsets
  - Alpha processors and chipsets
  - Chip level PCI devices
- General purpose operating systems
  - Windows
  - UNIX

CompactPCI also supports ...

- Embedded processor architectures
  - MC68K
  - PPC
  - StrongARM
- Embedded OS's
  - VxWorks (also for Intel and Alpha)
  - pSOS
  - LynxOS

CompactPCI today

- Specifications developed under jurisdiction of PCI Industrial Computer Manufacturers' Group, PICMG, an industry consortium of over 400 members
- PICMG 2.0 Rev 2.1 CompactPCI Core Spec
  - PICMG 2.1 Rev 1.0 Hot Swap
  - PICMG 2.5 Rev 1.0 Computer Telephony
  - PICMG 2.2 Rev 1.0 VME64 Extensions

CompactPCI evolution

- PICMG 2.0 Rev 3.0
  - Update incorporating Hot Swap and CT Extensions, 66 MHz operation
- Keying
- Bridging
- Dual CompactPCI System Slot
- Instrumentation Extensions
- System Management
- Hot Swap Modular Power

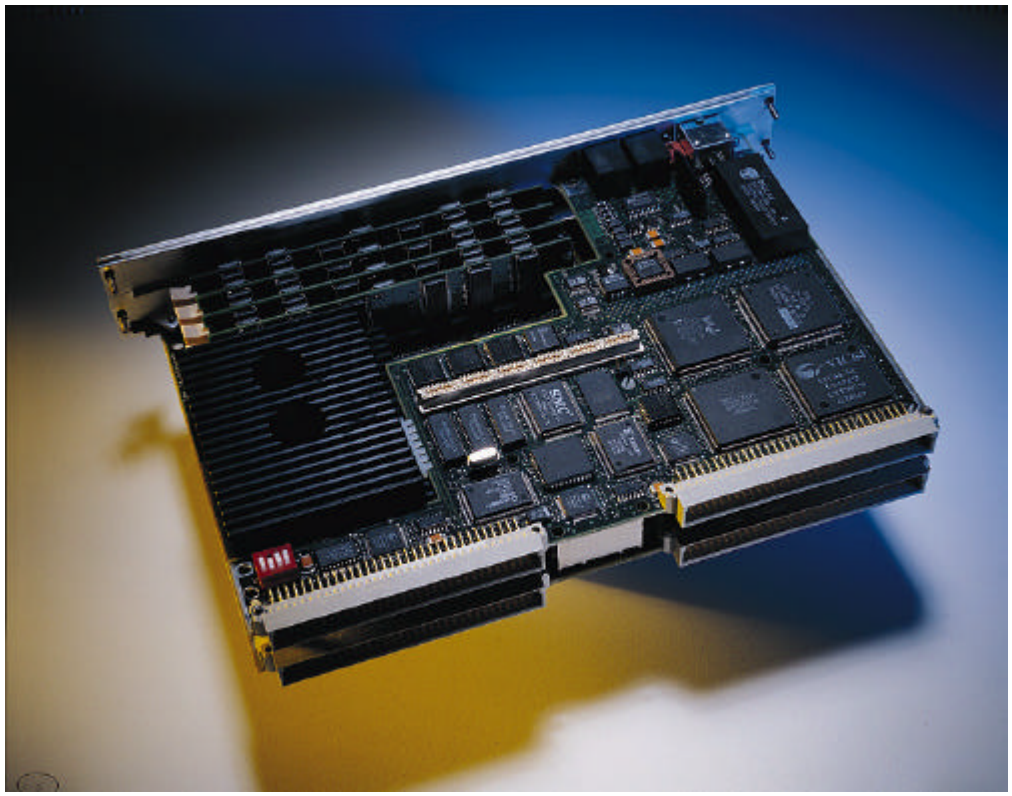
CompactPCI evolution

- Conduction Cooled CompactPCI
- System Slot Hot Swap
- Multicomputing
- IO Enhancements
  - PCI-X
  - NGIO
  - FutureIO

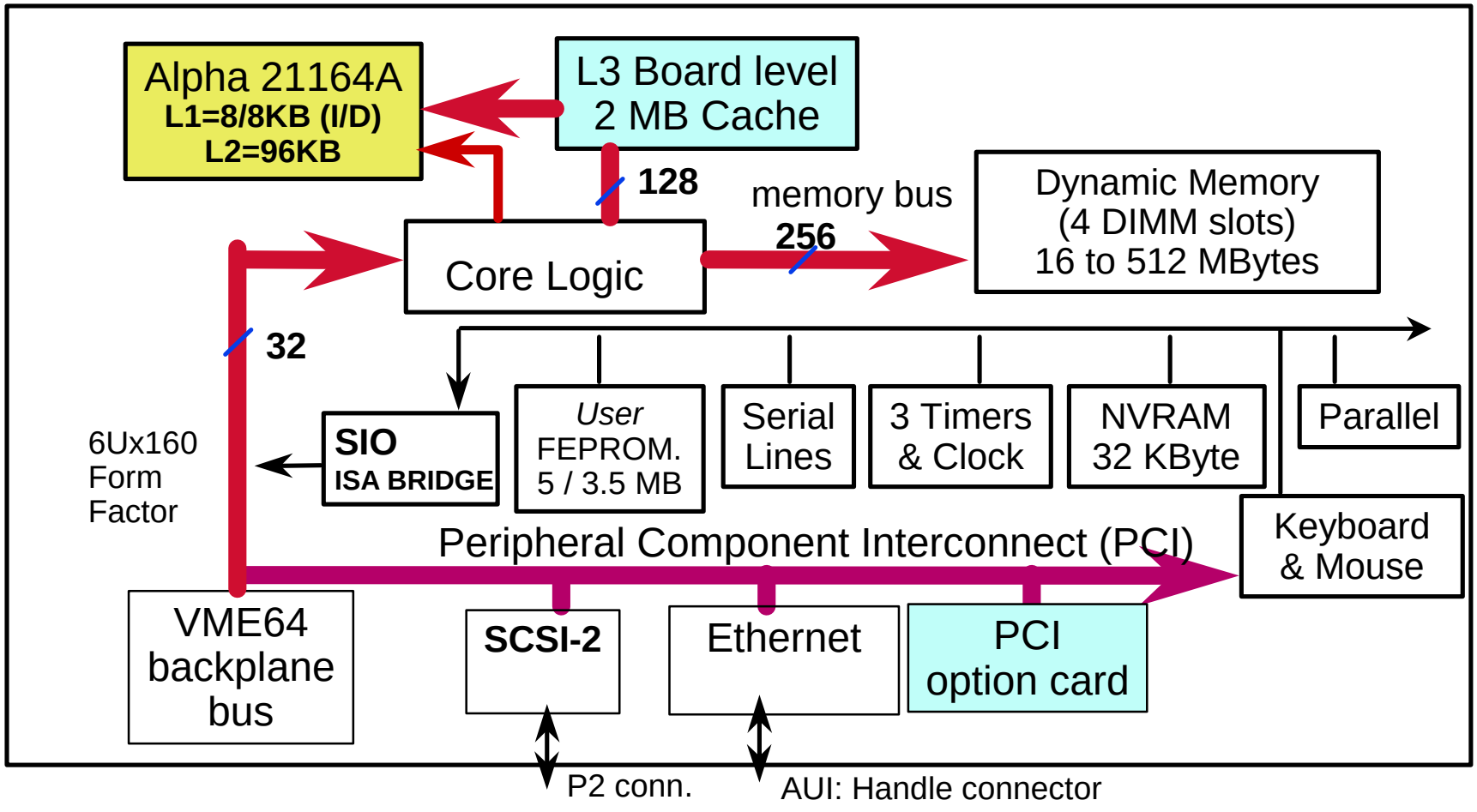
CompactPCI and VME64x

- CompactPCI and VME share common mechanicals
- VME64x signals have been mapped to CompactPCI J4 and J5
- Hybrid CompactPCI/VME systems have been built
- VME SBCs typically use PCI as a local bus
- PCI/VME bridge silicon available

VME SBC



VME SBC


Alpha 21164A
L1=8/8KB (I/D)
L2=96KB
L3 Board level
2 MB Cache
128
memory bus
256
Dynamic Memory
(4 DIMM slots)
16 to 512 MBytes
Core Logic
32
6Ux160
Form
Factor
SIO
ISA BRIDGE
User
FEPROM.
5 / 3.5 MB
Serial
Lines
3 Timers
& Clock
NVRAM
32 KByte
Parallel
Keyboard
& Mouse
Peripheral Component Interconnect (PCI)
VME64
backplane
bus
SCSI-2
Ethernet
PCI
option card
P2 conn.
AUI: Handle connector

CompactPCI and VME

	CompactPCI	**VME**	**VME64x**
Peak data rate	133 MB/s (PCI32 @ 33MHz) 266 MB/s (PCI64 @ 33MHz) 532 MB/s (PCI64 @ 66MHz)	40 MB/s	80MB/s D64 160MB/s 2eVME 320MB/s 2eSST
Cards/System w/o Bridging	8	21	21
Bus logic	CMOS	TTL	ETL
3.3 v migration	Yes	No	Yes

VME Advantages vs CompactPCI

- Multicomputing
  - Distributed interrupt handling
- Wide variety of processor architectures
  - General purpose
  - DSPs
- Wide variety of auxiliary interconnects
  - RACEway
  - SKYchannel
  - Myrinet

CompactPCI Advantages vs VME

- Leverages hardware and software investment for mainstream desktops and server market
- Intelligent IO
- Flexible configuration of system peripherals on local bus
- Greater aggregate BW to memory than competing VME protocol enhancements
- Tighter coupling to memory bus than VME

Longevity

- Will there ever be another VME?
  - Longevity
  - Evolution
  - Backward compatibility
- Probably not, but there is an alternative
  - Choose a robust HW platform that will track emerging desktop/server technology trends
  - Insert technology as it matures

Internet pointers

- http://www.digital.com/oem/
  - CompactPCI
  - PCI/ISA
  - VME
  - RTOS
- http://www.picmg.org/
  - Membership information
  - Specification Directory
  - Product Directory

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