- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

#### description

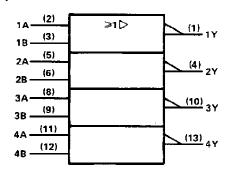
These devices contain four independent 2-input-NOR line drivers. They perform the Boolean function  $Y = \overline{A} + \overline{B}$  or  $Y = \overline{A} \cdot \overline{B}$ . The SN54128 is designed to drive 75 ohm lines. The SN74128 is designed to drive 50 ohm lines.

The SN54128 is characterized for operation over the full military temperature range of  $-55\,^{\circ}\text{C}$  to 125 $^{\circ}\text{C}$ . The SN74128 is characterized for operation from 0 $^{\circ}\text{C}$  to 70 $^{\circ}\text{C}$ .

#### logic diagram (each driver)



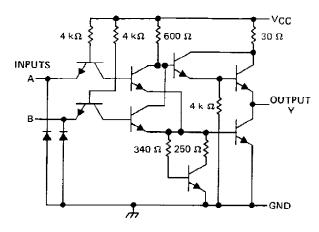
#### logic symbol†



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### SN54128 . . . J OR W PACKAGE **SN74128...N PACKAGE** (TOP VIEW) 1ҮД1 / 14口 Vcc 13 4Y 1A 🛮 2 18 □3 12 4B 2Y **□**4 11 4A 2A 🗆 5 10 3Y 28 □ 6 9 3B GND ☐ 7 8 3A

#### schematic (each driver)



Resistor values shown are nominal,

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range:	SN54'	- 55°C to 125°C
	SN74'	0°C to 70°C
Storage temperature range	· · · · · · · · · · · · · · · · · · ·	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### SN54128, SN74128 LINE DRIVERS

#### recommended operating conditions

		L	SN5412	В	SN74128			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4,5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2		-	2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 29			- 42.4	mA
loL	Low-level output current			48			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN TYP\$ MA	X UNIT
ViK	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.	5 V
	$V_{CC} = MIN$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -2.4 \text{ mA}$	2.4 3.4	
$v_{OH}$	$V_{CC} = MIN$ , $V_{IL} = 0.4 \text{ V}$ , $I_{OH} = -13.2 \text{ mA}$	2.4	→ v
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.4 V, I <sub>OH</sub> = MAX	2	_
VOL	V <sub>CC</sub> = MIN, V <sub>1H</sub> = 2 V, i <sub>OL</sub> = 48 mA	0.26 0.	4 V
11	VCC = MAX. V1 = 5.5 V		1 mA
ItH	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V	4	ДД С
lie_	V <sub>CC</sub> = MAX, V <sub>1</sub> = 0.4 V	-1.	3 mA
los§	VCC = MAX	- 70 - 18 <sup>1</sup>	Am C
<sup>I</sup> ссн	V <sub>CC</sub> = MAX	12 2	I mA
CCL	V <sub>CC</sub> = MAX	33 5	7 mA

t For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	MIN	TYP	MAX	UNIT		
tPLH			D -1225			6	9	ns	
<sup>₹</sup> PHL	A or B	V	R <sub>L</sub> = 133 Ω,	C <sub>L</sub> ≈ 50 pF		8	12	∩s	
₹PLH .		7 ~0.8	,	$R_1 = 133 \Omega$ ,	0 150 - 5		10	15	ns
<sup>t</sup> PHL			11[ - 133 28,	C <sub>L</sub> = 150 pF		12	18	П5	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

 $<sup>\</sup>pm$  All typical values are at VCC = 5 V, TA = 25°C.  $\S$  Not more than one output should be shorted at a time.



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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9861101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9861101QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-9861101QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-9861101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9861101QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54128J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54128J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74128D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74128N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74128N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74128N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74128NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74128NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74128NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74128NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54128FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54128FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54128J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54128J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54128W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54128W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type



#### PACKAGE OPTION ADDENDUM

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<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

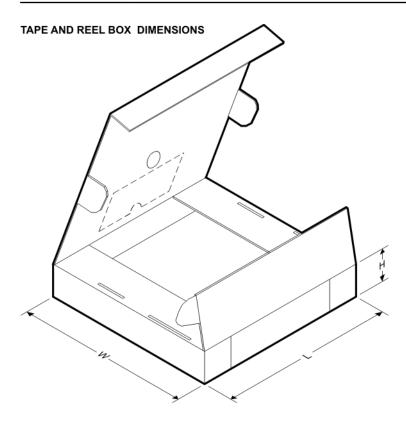
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74128NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74128NSR	SO	NS	14	2000	346.0	346.0	33.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



# FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE

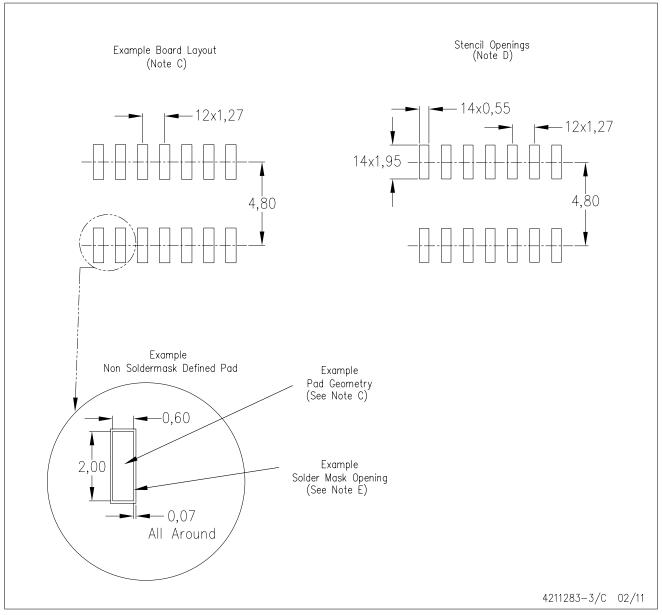


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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