



WIDAR in Pictures

Kevin Ryan



170,000 watts of power, 120 tons of cooling

for

17,308,672 control/monitor bits

in

1,473,536 registers

in

24,832 FPGAs

in

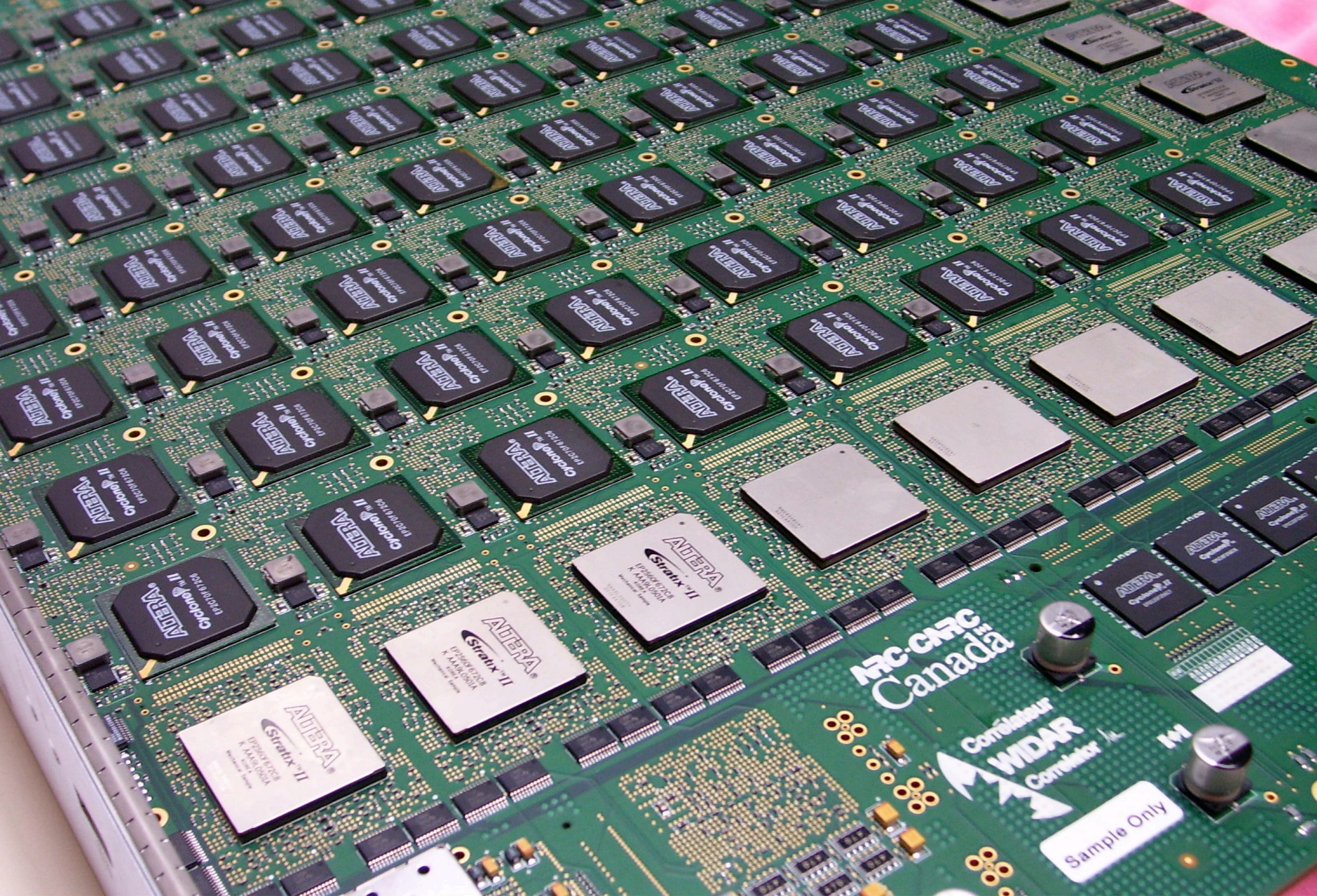
256 boards

in

16 racks

in

1 room

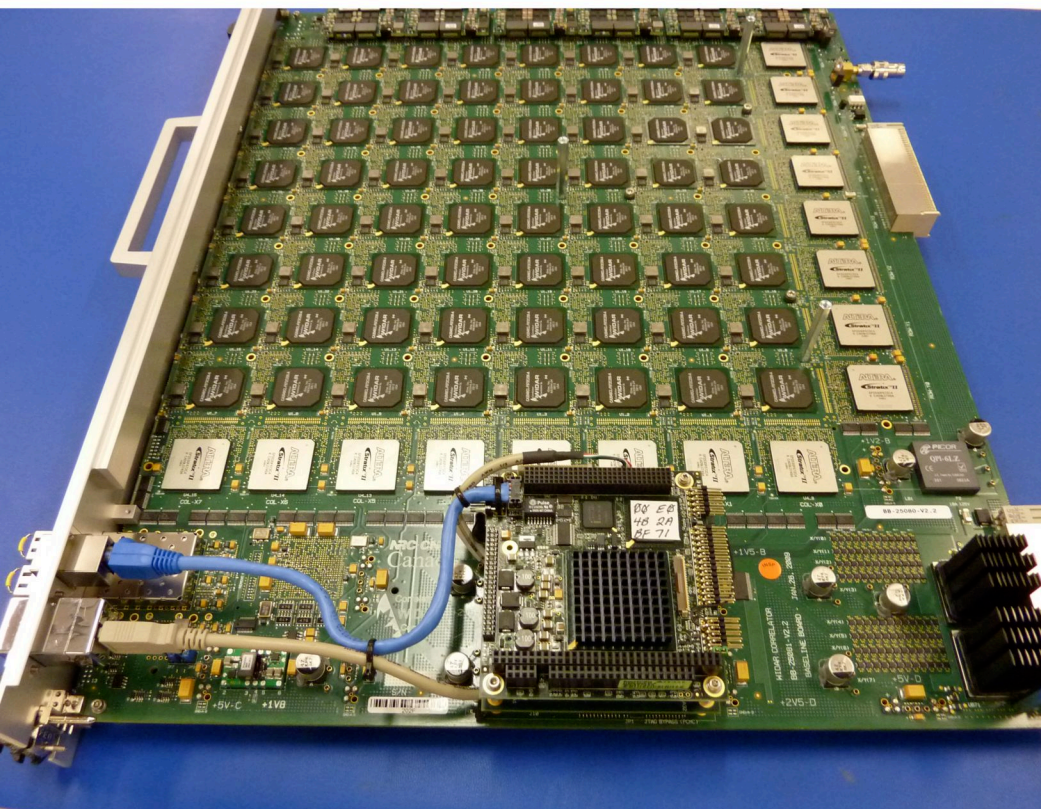
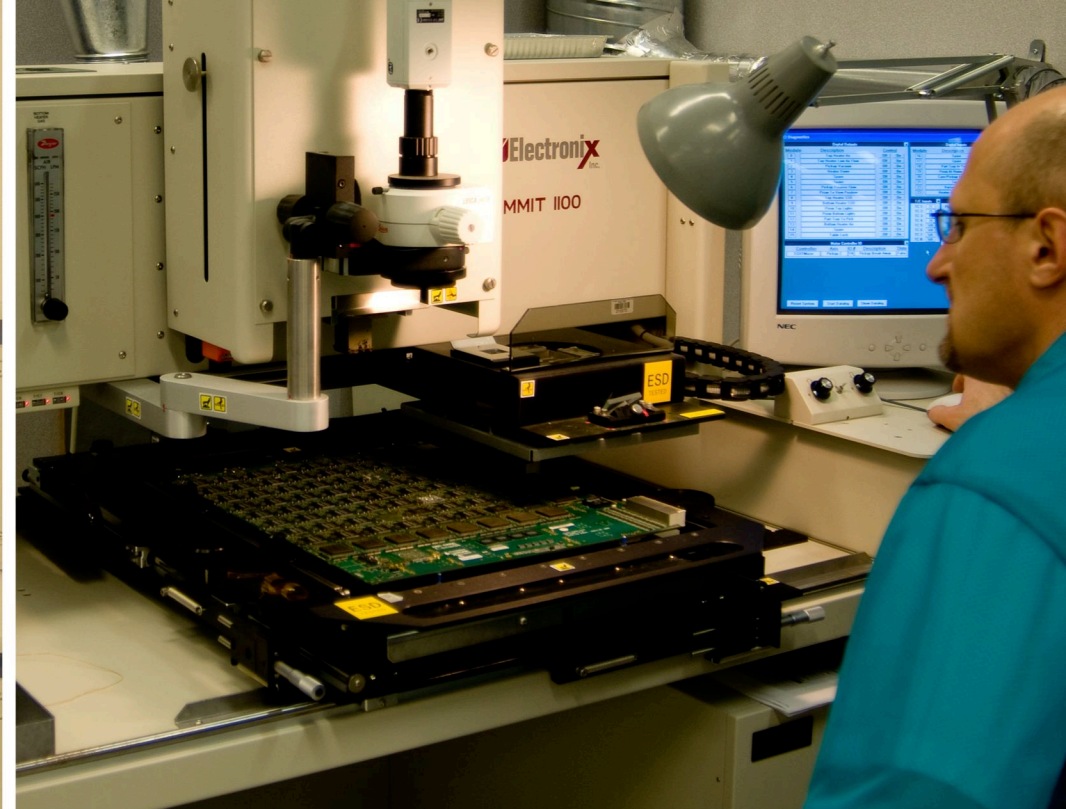
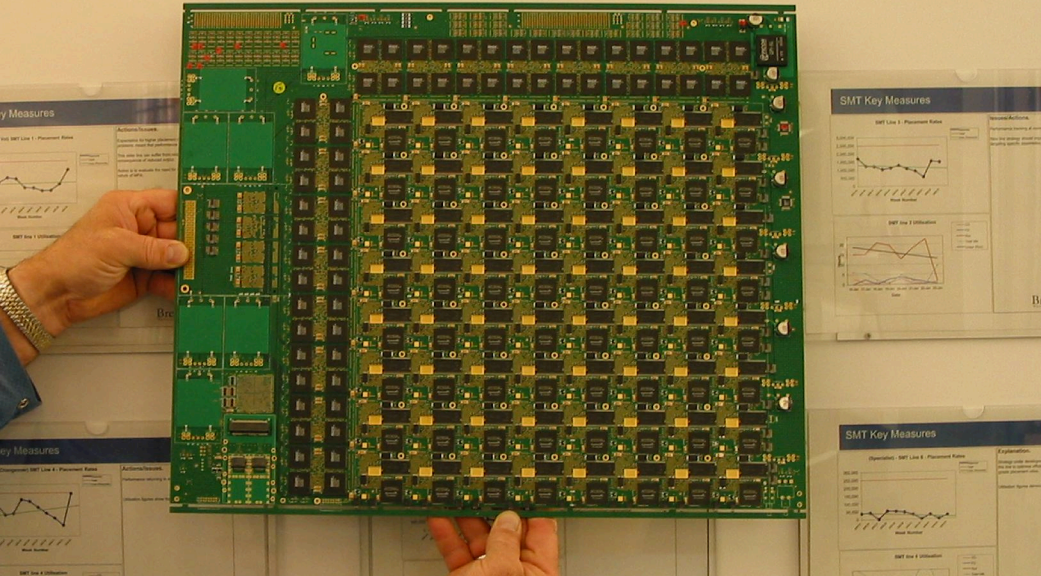


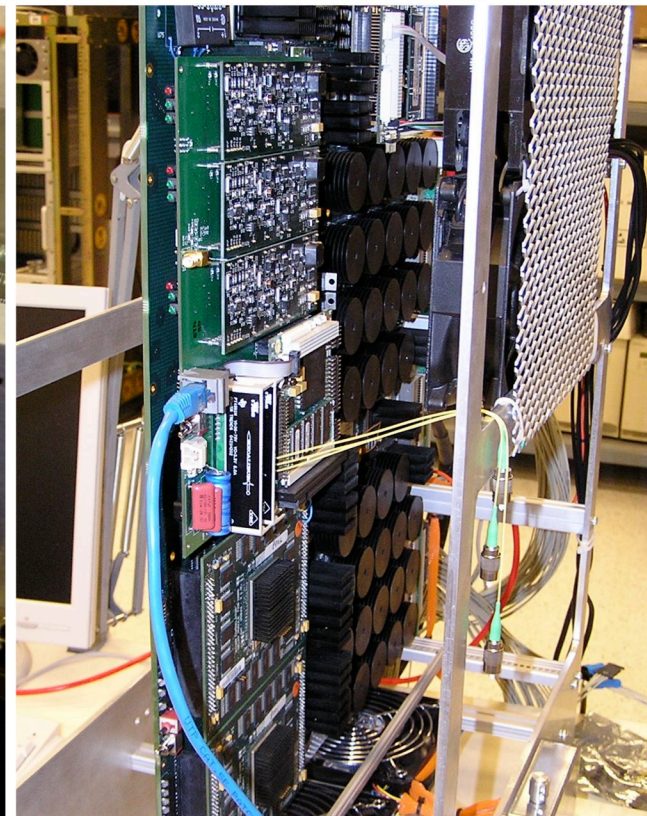
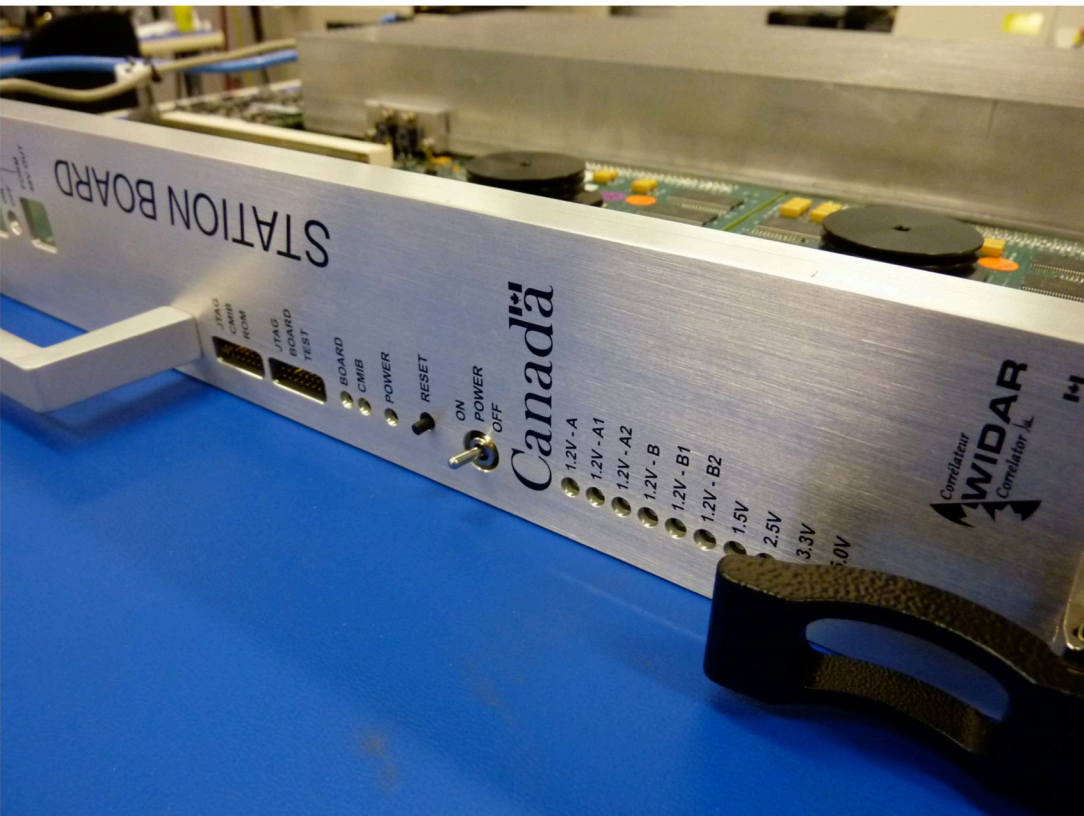
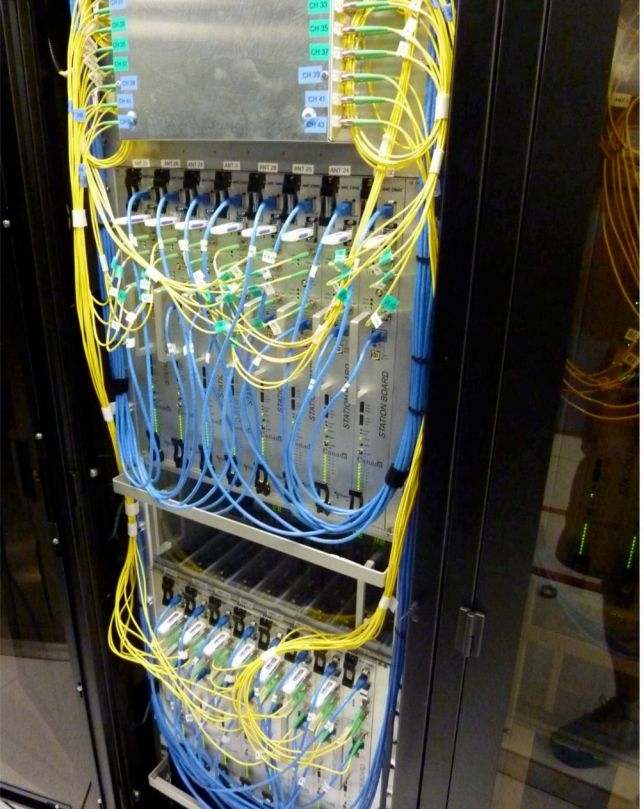
Baseline Board

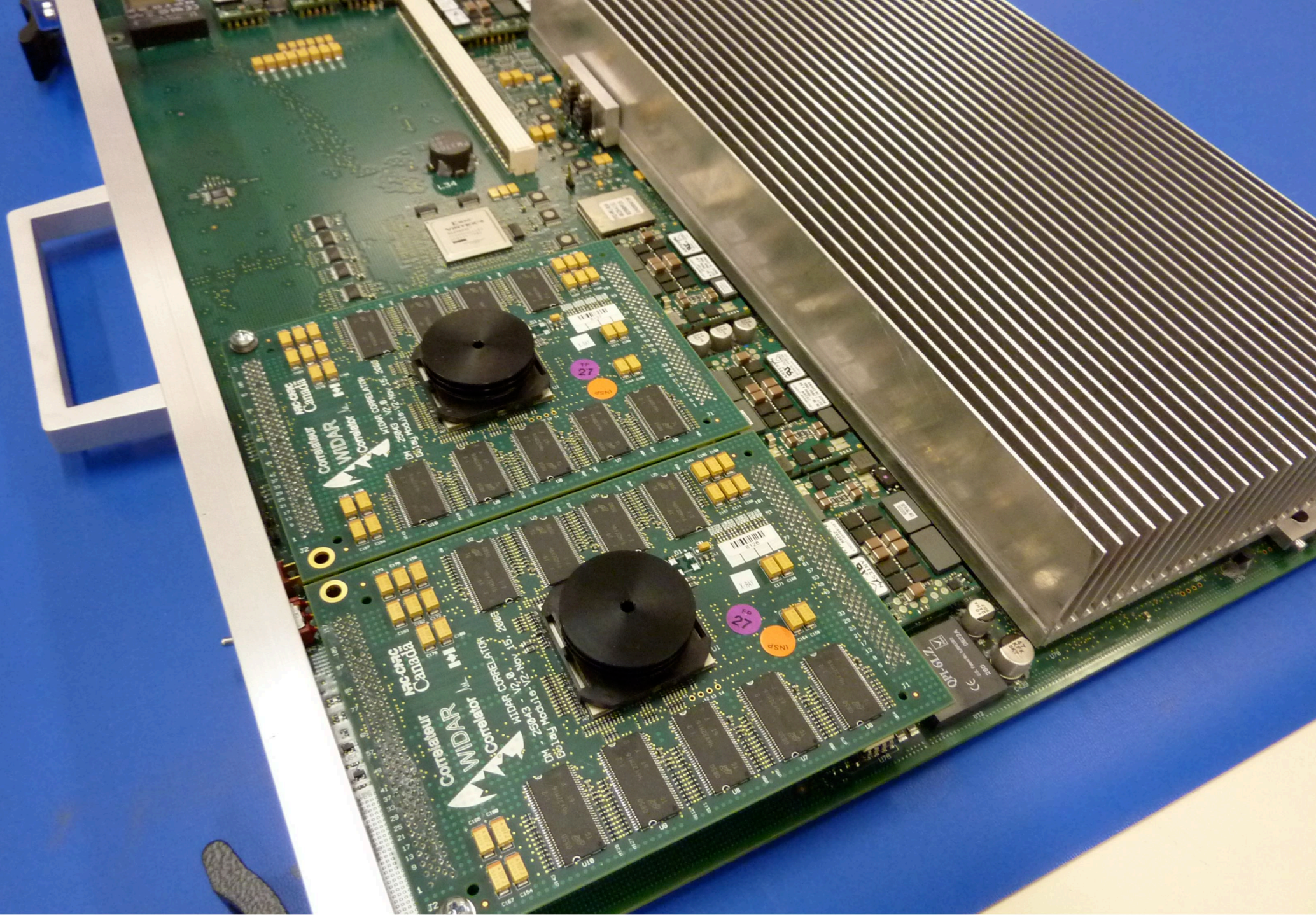
28-layers • 2km of traces • 11,000 components • 100,000 solder joints x 128

BreconRidge

Manufacturing Solutions

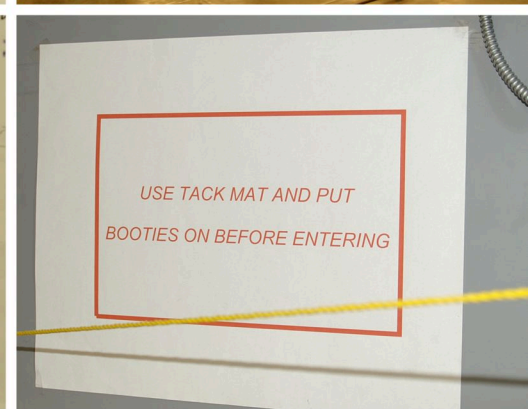
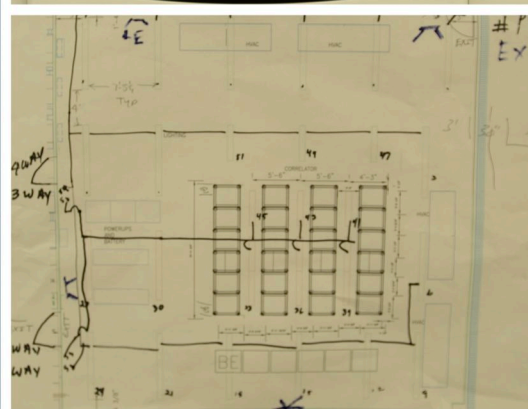






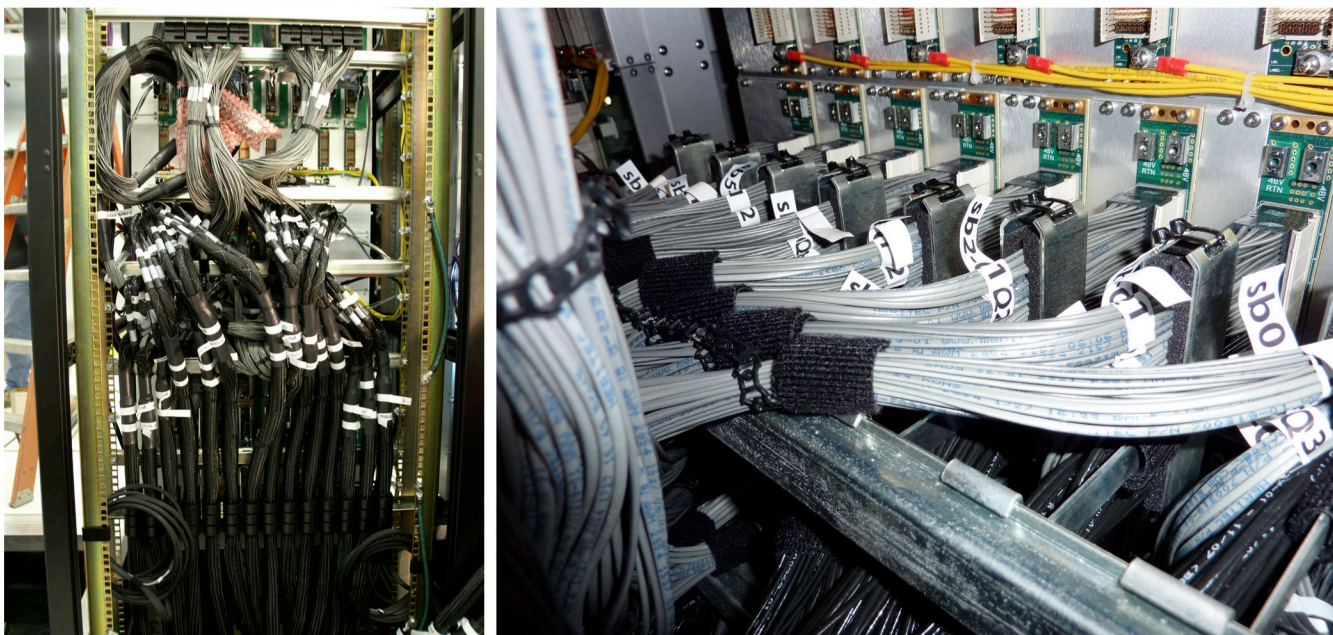
Station Board

28 layers • 1km of traces • 8,000 components • 50,000 solder points x 128





One room



- 65,536 connections • 16,384 lines • 50km of cables under the floor

S002

S003

S004

-48V DC
Breaker Panel

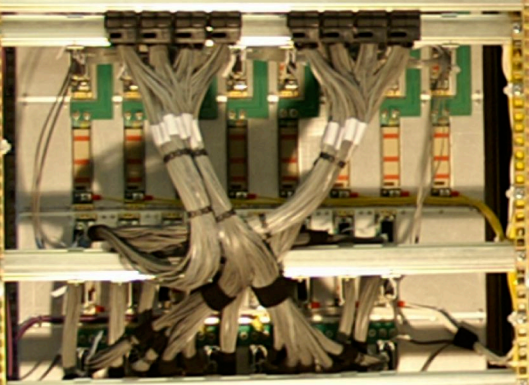
-48V DC
Breaker Panel

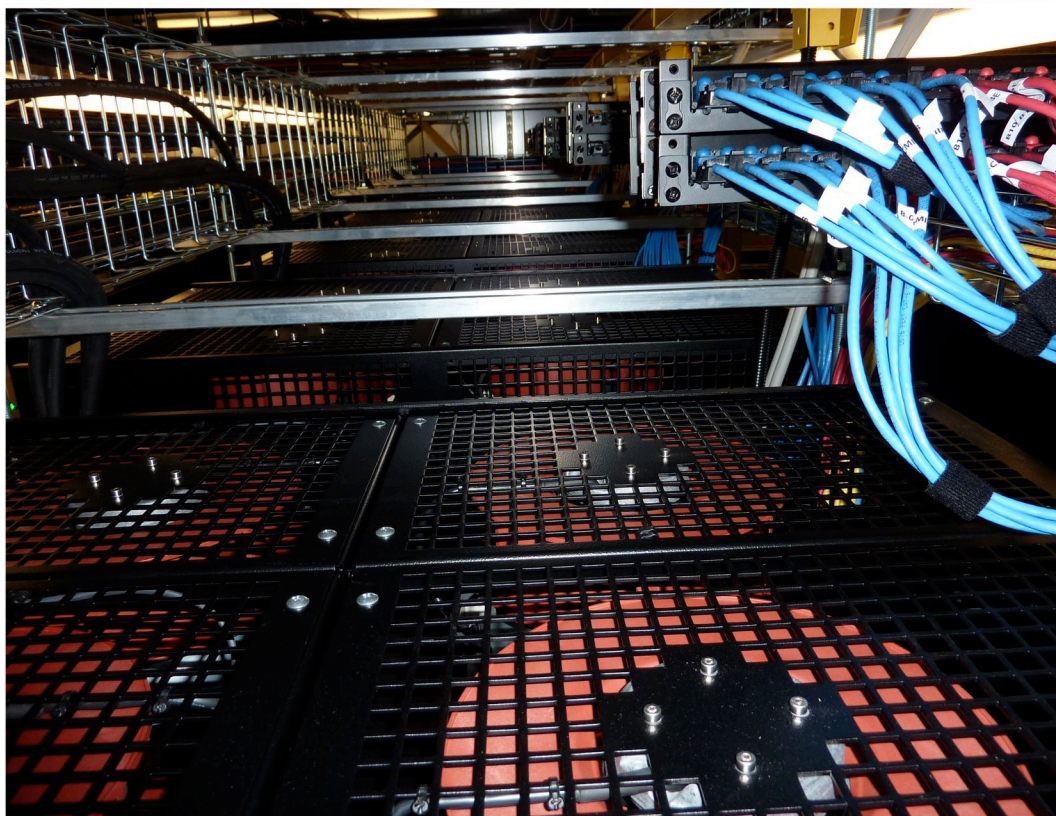
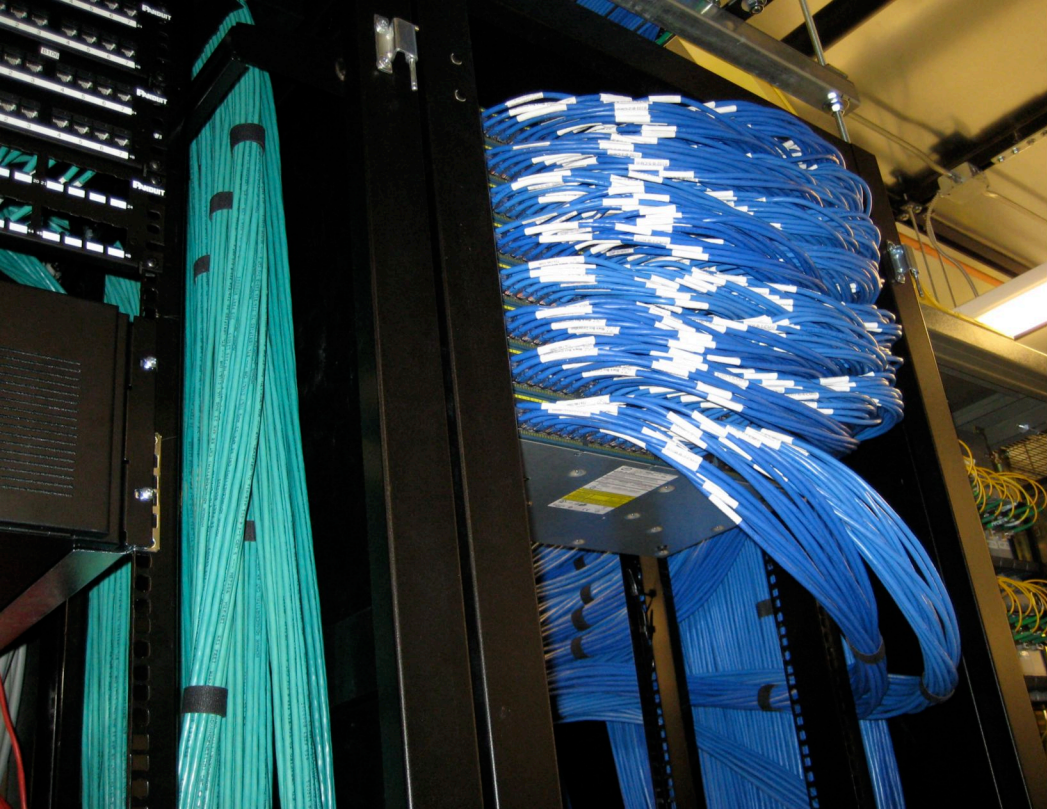
-48V DC
Breaker Panel

WIDAR

WIDAR

WIDAR





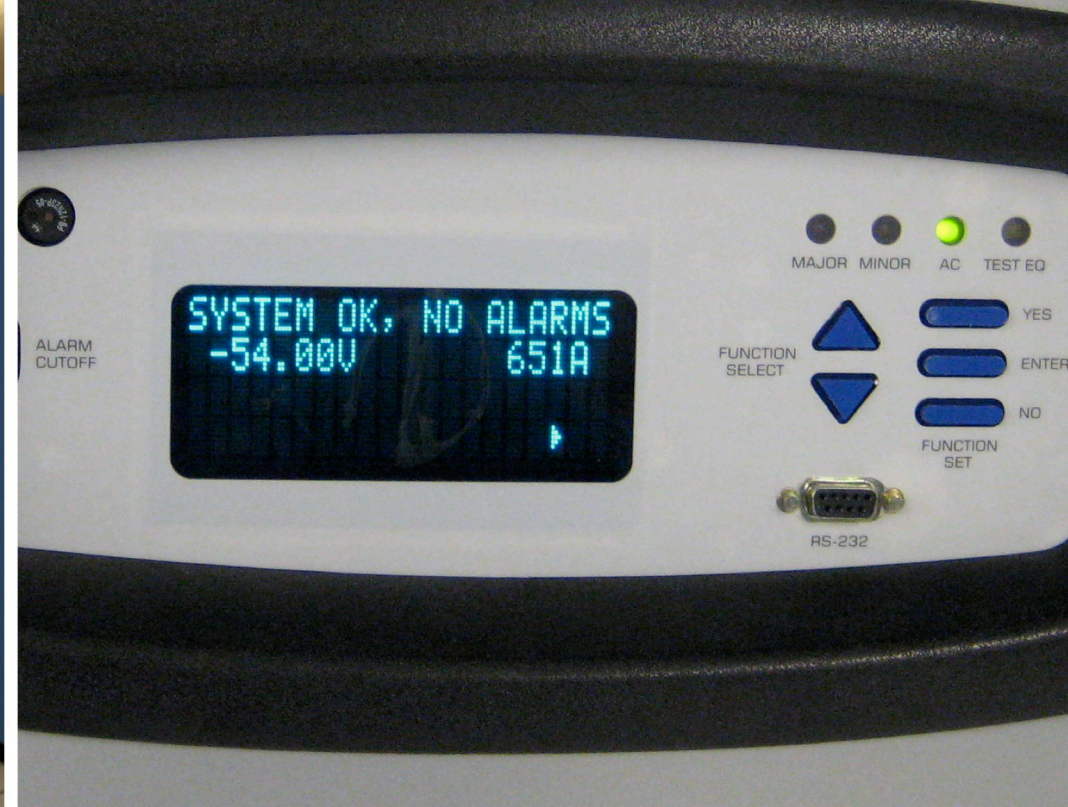


B103

S004

S003

S002





Power, cooling, protection



WIDAR Correlator Power & Temperature -- 20100708-0906

HVAC CW1 HVAC CW2

Fan within RPM range
Max Temp, Crate-Slot
Min Temp, Crate-Slot

Stage-3 2nd Smoke Detector
Stage-2 1st Smoke Detector
Stage-1 Supervisory
Smoke Detector

Individual Board Status
Max Temp °C
45 - 50
40 - 45
< 40

Power Supplies
FPGAs Programmed
Timecode Status latch

Reboot Load FPGAs Deprogram FPGAs Power UP Power DOWN

2C
Set Fan Speed S001

Rack To Monitor Rack(s) to Control

Top 0 1 2 3 4 5 6 7 8 9
6U Bottom Spare SSR-1 SSR-2 (Mon = SPR 0-5) (Cmd = SSR1/SSR2/SPR 0-3)

Control Enabled Screen Refresh 2 sec Refresh Squelch Popups

ServerComm cpcc1.evla.nrao.edu View

Clear Msgs

*** Stage 3 Smoke Detection ***
-- Commencing power off of Correlator Boards.



Scary testing

Screen Board

Power Supplies

All Power	48Vdc	-53.7	15	23
(latched)	3.3v	3.31	14	17
	2.5v	2.47		
	1.8v			
	1.5v	1.48		
	1.2v	1.19		

Board Temps °C

Y7: 15 23
Y6: 14 17
Y5: 14 17
Y4: 14 17
Y3: 14 17
Y2: 14 17
Y1: 14 17
Y0: 14 17

MCB Register Access

Register: 0x0000
Write + Read
Write Read

Screen Refresh: 1 sec Refresh Squelch Popups

Server/Comm: b101-t-1 View

In From Station Board
Phased Output
Out to CBE

Screen Board Control FPGA GUI ErrorCounts Logging Misc

Name/IP: s001-t-1
State: **running** Serial #: 0x0010
Version: 20120223-1119

Configuration: Act.Time: 2012-03-09T00:14:35.900
12A-032.b9053541.eb9242367.55995.02085108796.10

Status & Control

Interrupt Source: timingFPGA
CMB Interrupt Enabled
PCI Interrupt Enabled
External Delay Models

DPO Ant/St:2 BB:0

DP1 Ant/St:2 BB:1

up: 8d 3h 04m

up: 8d 4h 34m

03/08 11:00 kryan - disconnected.
03/08 11:34 vrcis - disconnected.
03/08 12:03 vrcis - connected.
03/08 12:05 vrcis - disconnected.
03/08 12:13 vrcis - connected.
03/08 14:46 browen - connected.
03/08 18:04 kryan - connected.
03/08 18:04 kryan - Clear all Errors

http://b101-b-2:8080/

Correlator Board CMB

baselineBoard: b101-b-2, bb2037, 10.80.211.144, 10.80.211.202

Board Status		
	Temperatures	Voltages
Op State	working	heatsink_T: 19.3 C
Error Code	0	board_UL: 15.3 C
Power		board_UR: 22.9 C
FPGA		nom_48_0v: -52.64 V
Signals		nom_5_0v: 4.88 V
		nom_3_3v: 3.25 V
		nom_2_5v: 2.43 V
		board_LL: 13.7 C
		nom_1_5v: 1.45 V
		board_LR: 12.5 C
		nom_1_2v: 1.17 V

[System Page](#) [GUI](#)

WIDAR Correlator Room -- 20101027-1410

HVAC CW1 HVAC CW2

Board Temperatures

Stage-3 2nd Smoke Detector
Stage-2 1st Smoke Detector
Stage-1 Supervisory
Smoke Detector Silent

TC-A

1 U-RXP pri clk
1 U-RXP sec clk
1 L-RXP pri clk
1 L-RXP sec clk

TC-B

1 L-RXP sec clk

Sensor Location: LED BB SB °C

1	Max	Max	20
2	HT	HT	24
3	UR	R	28
4	UL	B	32
			36
			40
			44
			48
			52

Set Fan Speed: **S002**

Rack To Monitor: 0 1 2 3 4 5 6 7 8 9
GU:
Bottom:
Spare:
Cmd: SSR-1 SSR-2
Mon: Fire1* Fire2* Fire3* * = Active-Low

Screen Refresh: 2 sec Refresh Squelch Popups

Server/Comm: cpcc1.evla.nrao.edu View

2012.02.23 18:42.08 - cpcc2: WIDAR Power Plant Alert : A/C Power Restored.
Deprogram and Power-down timers cancelled; System operational state should not have been aff
2012.03.08 09:29.09 - cpcc1: WIDAR Power Plant Alert : Loss of A/C Power detected.
Timers started to initiate FPGA deprogram in 300 seconds and board power-down in 900 seconds
2012.03.08 09:29.09 - cpcc2: WIDAR Power Plant Alert : Loss of A/C Power detected.
Timers started to initiate FPGA deprogram in 300 seconds and board power-down in 900 seconds
2012.03.08 09:29.26 - cpcc1: WIDAR Power Plant Alert : A/C Power Restored.
Deprogram and Power-down timers cancelled; System operational state should not have been aff
2012.03.08 09:29.26 - cpcc2: WIDAR Power Plant Alert : A/C Power Restored.
Deprogram and Power-down timers cancelled; System operational state should not have been aff

High-Tech 'Heart' of New-Generation Radio Telescope Passes First Test

The [Expanded Very Large Array \(EVLA\)](#), part of the National Radio Astronomy Observatory (NRAO), took a giant step toward completion on August 7 with successful testing of advanced digital hardware designed to combine signals from its upgraded radio-telescope antennas to produce high resolution images of celestial objects.

By upgrading the 1970s-era electronics of its original Very Large Array (VLA), NRAO is creating a major new radio telescope that is ten times more sensitive than before. Using the EVLA, astronomers will observe fainter and more-distant objects than previously possible and use vastly improved analysis tools to decipher their physics.

The heart of the new electronics that makes this transformation possible is a high-performance, special-purpose supercomputer, called the WIDAR Correlator. It has been designed and is being built by the National Research Council of Canada at the Dominion Radio Astrophysical Observatory (DRAO) of the Herzberg Institute for Astrophysics, and serves as Canada's contribution to the EVLA project.

The design of the correlator incorporates an NRC-patented new digital electronic architecture. The successful test, at the VLA site 50 miles west of Socorro, New Mexico, used prototype correlator electronics to combine the signals from two upgraded VLA antennas to turn them into a single, high-resolution telescope system, called an interferometer. The technical term for this achievement is called "first fringes."

Each upgraded EVLA antenna produces 100 times more data than an original VLA antenna. When all 27 antennas are upgraded, they will pump data into the WIDAR correlator at a rate equal to 48 million digital telephone calls. To process this torrent of data, the correlator will make 10 million billion calculations per second.

Powerful, multi-antenna imaging radio-telescope systems use pairs of antennas as their basic building blocks. Each of the VLA's 27 giant dish antennas is combined electronically with every other antenna to form a multitude of pairs. Each pair contributes unique information that is used to build a highly-detailed image of some astronomical object. The successful two-antenna test thus verifies the design of the new correlator.

"This achievement marks the first time that the complete chain of electronics for the EVLA has worked together, and represents a huge milestone in the project. Our congratulations go to our Canadian colleagues and to the NRAO staff members participating in this project. This is a job well done," said Fred Lo, Director of the National Radio Astronomy Observatory.

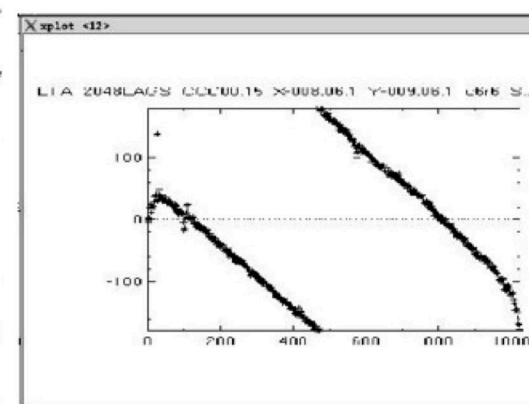
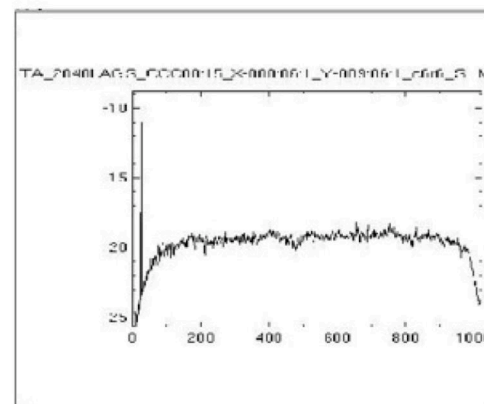
The VLA Expansion, a ten-year project approved in 2001, is funded by \$55 million from the United States National Science Foundation (NSF) and \$1.75 million from the Mexican government. The Canadian correlator represents a contribution of about \$17 million to the project.

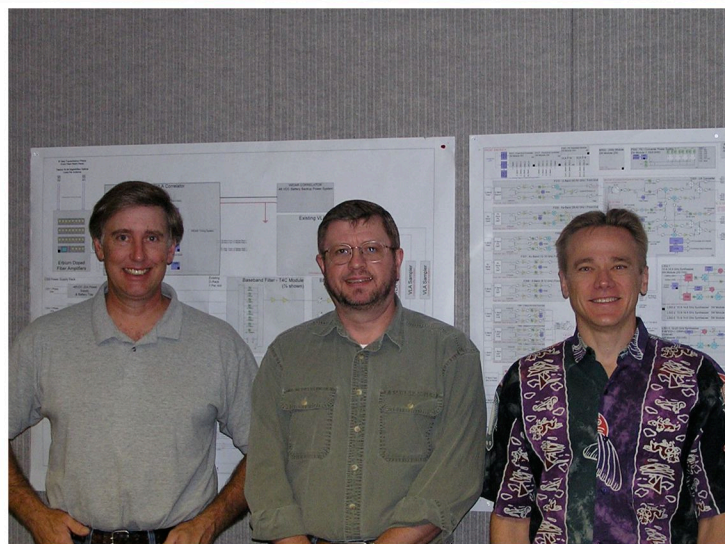
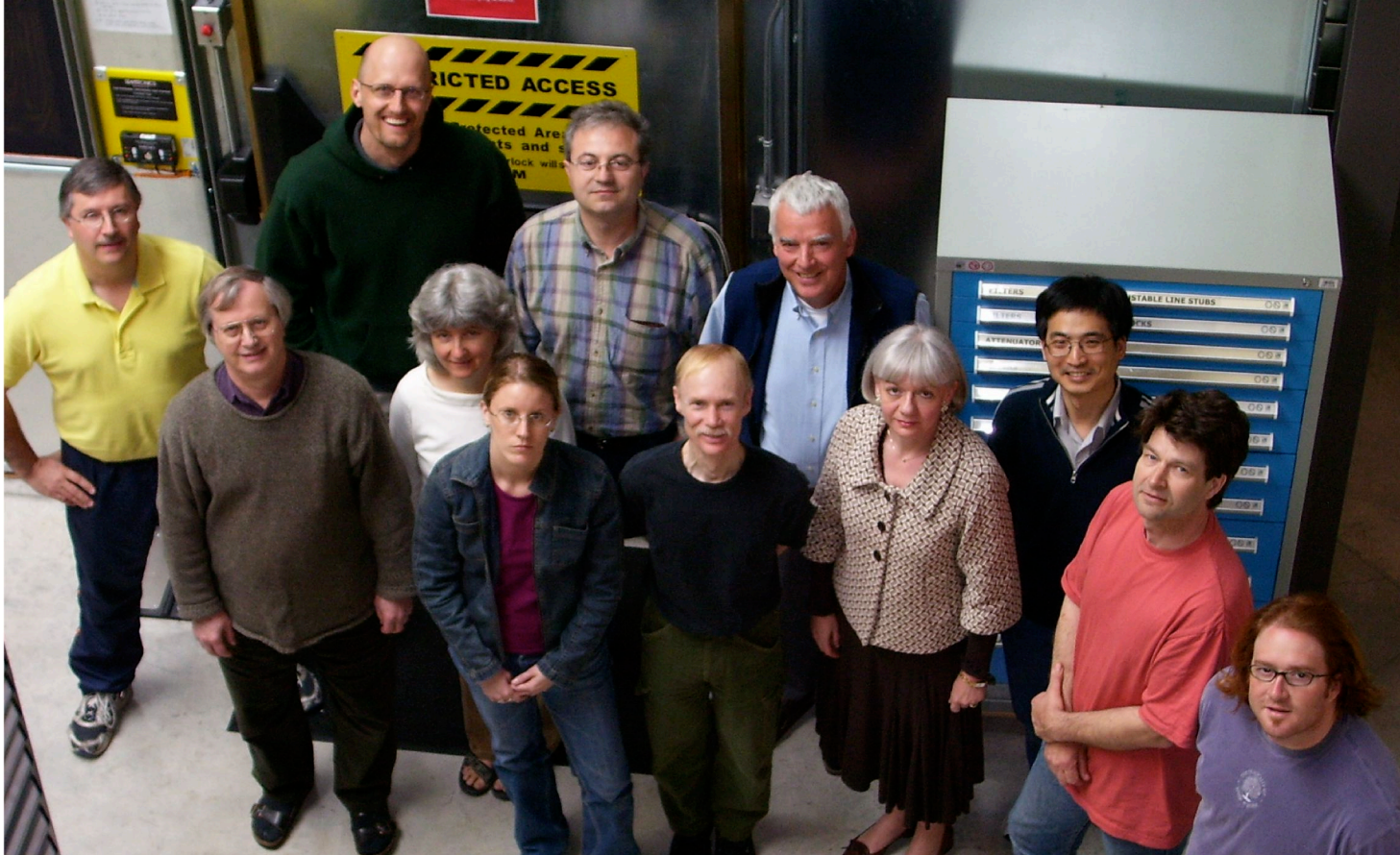


NRAO Crew Views Successful Computer Display Of WIDAR "First Fringes"
Seated, front to back: Barry Clark, Ken Sowinski, Michael Rupen, Kevin Ryan. Standing, front to rear: Mark McKinnon, Rick Perley, Hichem Ben Frej.
CREDIT: Dave Finley, NRAO/IAUI/NSF
Click on image for larger file.



First Fringes August 7, 2008





The people

